A NOVEL HYBRID ENERGY SYSTEM FOR SUPPLYING ISOLATED LOADS WITH FPGA BASED ENERGY MANAGEMENT SCHEME

PROJECT COMPLETION REPORT

SUBMITTED TO
NATIONAL INSTITUTE OF WIND ENERGY, CHENNAI

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Chapter 1

INTRODUCTION

Electrical power has become a vital requirement in this modern world, where every aspect of human activities is ruled by some form of high end technology. It is well known that the per capita power consumption is one of the key indicators of the well-being of a nation. In this context, to meet the ever increasing demand for this electrical power, it has become inevitable to exploit all possible sources of renewable energy. This attempt is not only to overcome the depleting fossil fuels, but also for substantially reducing the environmental pollution and creating an eco-friendly environment in this planet.

There is an ever increasing demand for electrical energy in our country, rapidly advancing in all sectors of development. Apart from the requirement by the varied industries, irrigation of vast agricultural lands and modern household applications in the expanding urbanisation in our country escalates the need for expanding current electrical power capacity. In this context, creating an eco-friendly environment is a prime concern, whereby getting rid of the air pollution, emphasises the need for power from renewable energy sources. This has led to the proposal for going in for all electric vehicles in the next few years, thereby causing an additional demand for electricity. A recent report on 19th Electric Power Survey of India has estimated the peak electricity demand of 162 GW during the year 2016-17, 226 GW for 2021-22 and 299GW for the year 2026-27 [1].

Apart from the increased stress on reducing the environmental pollution, the depleting fossil fuels also has put a compelling need for adopting power generation from renewable energy sources, either to augment the grid power or for supplying certain isolated loads [2]. As a result, global installed capacity of renewable power generation system rose to 921 GW in the year of 2016 [3]. As on 31.12.2016, the total installed generation capacity in India has reached

to 310 GW (as shown in Fig. 1.1) with generation mix of Thermal (69.4%), Hydro (13.9%), Renewable (14.8%) and Nuclear (1.9%) [4]. It is evident that the renewable power has secured 2nd position after Thermal and is spreading its wings rapidly in India. Fig. 1.2 shows the sector-wise Installed Capacity of Renewable Energy in India as on 31.12.2016 in MW [4]. Figs. 1.3 and 1.4 shows the estimated wind and solar potential that can be tapped for power generation [4].

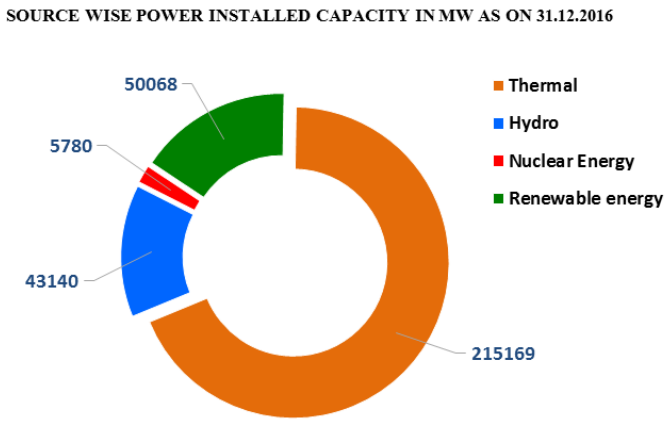


Fig. 1.1 Electrical power installed capacity (MW) in India as on 31.12.2016

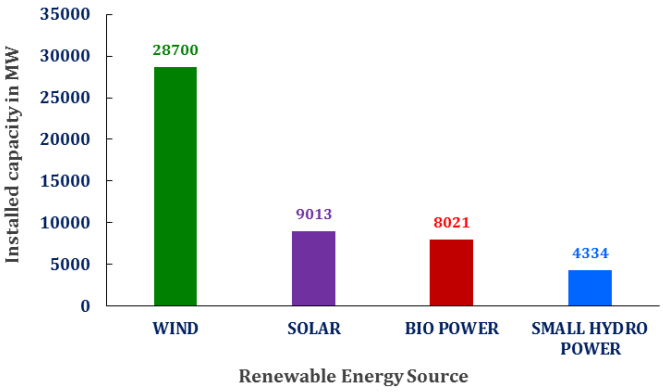


Fig. 1.2 Sector-wise installed capacity(MW) of Renewable Energy in India as on 31.12.2016

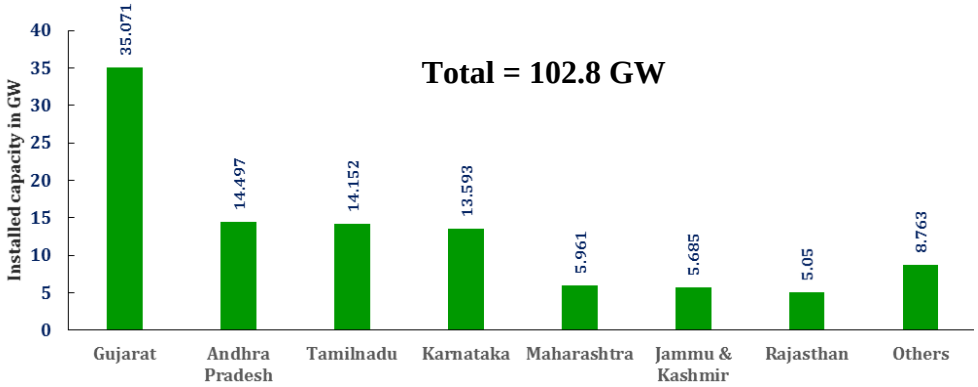


Fig. 1.3 Available Wind potential in India, estimated as on 28-02-2017

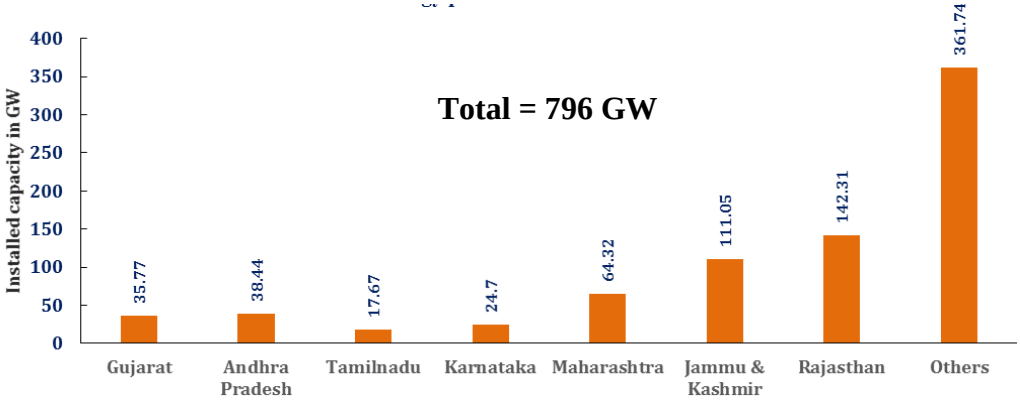


Fig. 1.4 Available Solar potential in India estimated as on 28-02-2017

Across the world, there are remote areas in several countries which cannot be physically or economically connected to an electric power grid. It is reported that over 20 % of the world's population are still without access to electricity [5]. Traditionally, the electricity needs of these remote areas are met by small isolated diesel plants. However, the operating cost of diesel plants at remote locations is huge and there are also few operational difficulties such as fuel transport, equipment maintenance, etc. Electrical energy conversion from renewable energy sources is a prime solution to come out of these difficulties. Efforts have also been made by many countries to provide access to electricity by extending the grid or by installing off-grid power generation systems [3]. Providing access to electricity through central electric grids is found to be uneconomical in many rural areas [6]. Recently, Indian government has launched a scheme 'Deen Dayal Upadhyaya Gram Jyoti Yojana' with an aim to achieve 100 % rural electrification at the end of 2016 [7]. In the progress report of this scheme, it is evident that rural electrification by off-grid systems has been given importance than grid-connected systems.

Owing to technological improvements and significant cost reductions, power generation from wind energy is nearly competitive with conventional sources. So, among various renewable energy sources, wind energy is the leading source as it can be converted into other useful forms of energy at an affordable cost. Further, wind energy electric conversion

systems (WEECS) have been found to be viable in contributing significant amount of electric power, when installed in locations where adequate wind potential is available over most part of the year. So, WEECS plays a vital role for rural electrification to satisfy the electricity needs of the people living in remote locations.

In WEECS, Permanent Magnet Synchronous Generators (PMSGs) or asynchronous generators with Squirrel-Cage Induction Machine (SCIM) / Wound Rotor Induction Machine (WRIM) have largely been employed along with suitable power electronic controllers [8-11]. Many stand-alone WEECS have been developed in the recent past, employing PMSG [10]. Possibility of low speed operation of PMSG eliminates the need for gear arrangement in wind-turbine. Also, the presence of permanent magnet eliminates need for an additional reactive power source and improves the efficiency. Attention had also been given for the development of stand-alone WEECS with SCIM [8-17]. The major advantages of this machine are low cost, robust operation and low maintenance requirement. It is reported that a fixed capacitor and/or power electronic converter provides necessary reactive power for the operation of this machine. In stand-alone WEECS employing PMSG or Squirrel-Cage Induction Generator (SCIG), power electronic converter(s) is required for constant ac voltage magnitude and frequency operation. This power electronic converter(s) should be rated for handling the maximum power delivered by the machine.

For stand-alone power supplies feeding isolated loads, Self-Excited Induction Generators (SEIGs) employing SCIM are being used with WEECS [8-18]. It is known that the output voltage and frequency of SEIGs vary with the driving speed, load and machine parameters. The terminal voltage of the SEIG has been maintained constant by employing variable capacitor configuration such as Static Synchronous Compensators (STATCOM), switched capacitor and static VAR Compensators along with the fixed capacitor [13-14, 19, 20]. A hybrid excitation system consisting of capacitor bank and active power filter for

supplying both ac and dc loads with sinusoidal stator current from SEIGs has also been proposed [14]. It is to be noted that the frequency of SEIG predominately depends on the rotor speed [18, 21-22]. Hence, these configurations fail to maintain stator frequency, if the generator operates with wide rotor speed variation. Later, to achieve constant voltage magnitude and frequency at the stator terminals, inverter assisted induction generators have been proposed in the literature [23] and the inverter along with the battery operates as a virtual grid. The reactive power requirement for the generator and load is being supplied by the Battery-Inverter System (BIS). To reduce the burden on the inverter, a hybrid excited system has been proposed in which fixed capacitor along with the battery-inverter has been used [24]. In such inverter assisted system, the range of generator rotor speed is restricted, since the stator is fed with constant frequency.

Wound Rotor Induction Machine (WRIM) based stand-alone WEECS have also been developed for stand-alone applications [10, 25]. In such WEECS employing WRIM, the stator is connected to isolated loads; whereas, the rotor is connected to an external resistance through a power electronic controller. The slip power is dissipated in the external resistance for the control of stator voltage magnitude and frequency which restricts the potential utilization of wind energy.

Recently, Doubly-Fed Induction Generator (DFIG) based stand-alone WEECS have also reached the commercial market which employs WRIM, though they require maintenance because of the presence of slip-rings and brushes [26]. Reduced power converter rating and wide speed operation of rotor are the major advantages of this system. In this context, several studies on DFIGs for stand-alone applications have also been reported in the literature [26-35]. As the dc-link is common in the case of conventional back-back connected converter configuration of DFIG, control of these two back-back converters is coupled to each other. This dc link voltage has to be maintained on the higher value when transformer is not connected

between the stator side converter and load. This necessitates an additional power converter for interfacing the battery storage systems to provide a continuous power to the isolated load and also for smoothing out the intermittent nature of the wind [35]. In this context, a simple system for the operation of DFIG involving only single Voltage Source Inverter (VSI) has been proposed for supplying isolated loads with battery [32-33]. The advantages of this configuration are i) self-starting ii) simple control strategy with only one inverter at rotor side iii) absorbing the excess power/supplying the deficit power from the wind using battery iv) very low-voltage harmonics and v) possibility of supplying loads even at no wind condition. However, the reactive power requirement of the generator and load has been supplied only by BIS connected at the rotor terminals. So, to take advantage of the enumerated merits, this project aims at employing DFIG with single inverter configuration for wind energy.

Most of the literature available on the operation of stand-alone DFIGs for supplying isolated loads has concentrated on the closed loop control for maintaining constant voltage magnitude and frequency with reduced harmonics [26-34]. Less attention is given on operating the power converter for minimizing the machine loss of such stand-alone systems. In this context, an algorithm for determining the optimal share of reactive power for stator side and rotor side converters of the stand-alone DFIGs has been presented for minimizing the machine and converter losses [30]. So, to minimize the losses, it is proposed to supply the reactive power at the stator terminals also, by connecting the appropriate value of fixed capacitor. The fixed capacitor at the stator terminals can supply a fixed reactive power for the entire operating region and the deficit reactive power is met by BIS. In addition to minimizing the loss in the system, this further reduces the burden on the BIS. It is to be noted that the net reactive power at the stator terminals should be varied dynamically depending upon the reactive power requirement of the load for operating the system with minimum loss. Hence, the capacitor at the stator side should be varied dynamically for operating the system with minimum possible power loss.

Therefore, an attempt is also made in this project for achieving this by employing a DSTATCOM at the stator terminals.

To alleviate the intermittent nature of wind, few authors have suggested the inclusion of various types of energy storage devices with stand-alone WEECS [10, 36]. Owing to wide availability, fast response, simple power converter topologies, ease of control and management, battery storage system is popular with such small scale stand-alone wind-generator systems [10]. The size of batteries should be increased with the increase in power generation capacity, for supplying continuous power to the isolated loads. Further, inclusion of battery increases the cost and also the battery has to be periodically replaced.

A common method of using wind and solar energy in remote areas is to operate the Wind Turbine Generator (WTG) and/or the Photo Voltaic (PV) units in parallel with diesel generators, in order to reduce the average diesel load and hence to save fuel. This mode of operation is particularly suitable for system with relatively small renewable energy penetrations. This system can result in some energy wastage when there is sufficient wind and/or solar energy available, especially at high renewable energy penetrations [37]. Since wind energy and photovoltaic energy are of intermittent nature, these problems can be alleviated to some extent by adding energy storage devices such as batteries to the system. The storage battery banks improve the reliability of these systems because the excess energy is stored in the battery bank, and this energy is delivered to the load when the available energy is not sufficient. Wind energy and photovoltaic energy have complementary characters. Thus, combining wind energy and photovoltaic in one system (hybrid system) increases the reliability of the system and reduces the size of storage batteries [38].

In this project, an SCIG driven by biogas / diesel fuelled IC engine is also proposed to be integrated in the micro grid to operate in grid connected mode. The reactive power

requirement of SCIG can be met with a fixed capacitor and DSTATCOM [39], whose DC side voltage can be maintained with the power available from the solar panel-battery system. Another novel approach in this proposal is that all the control units required for controlling the DSTATCOM, solar battery charger for MPPT and rotor side inverter of WRIG will be implemented digitally employing Field Programmable Gate Array (FPGA) based embedded control system. FPGAs offer significant advantages over microprocessors and DSPs for high performance, low volume applications, particularly for those that can exploit customized bit-widths and massive instruction-level parallelism. The innovative development of FPGAs whose configuration could be re-programmed an unlimited number of times has prompted the invention of a new field in which many different hardware algorithms could execute, in turn, on single device, just as many different software algorithms can run on a conventional processor. This would substantially reduce the cost, size and maintenance of the control units. When comparing the dynamic performance, control capabilities and concurrency in PWM-controlled Power Converters, FPGA based digital techniques are better than DSPs [40, 41].

This project is also timely significant as the Ministry of New and Renewable Energy (MNRE), Government of India has recently launched a programme on "Small Wind Energy and Hybrid System (SWES)" during the 11th Plan i.e., 2010-11 and 2011-12 [42]. So, it is proposed to develop a hybrid stand-alone power system (micro grid) utilizing wind, solar energy and diesel generator shown in Fig. 1.5. The proposed system will have a wind-driven solar excited Wound Rotor Induction Generator (WRIG), Photovoltaic Arrays (PV) and a diesel-fuelled IC engine driven Squirrel-Cage Induction Generator (SCIG). In order to cater to the reactive power requirement of SCIG and loads, a DSTATCOM will be connected in the micro grid.

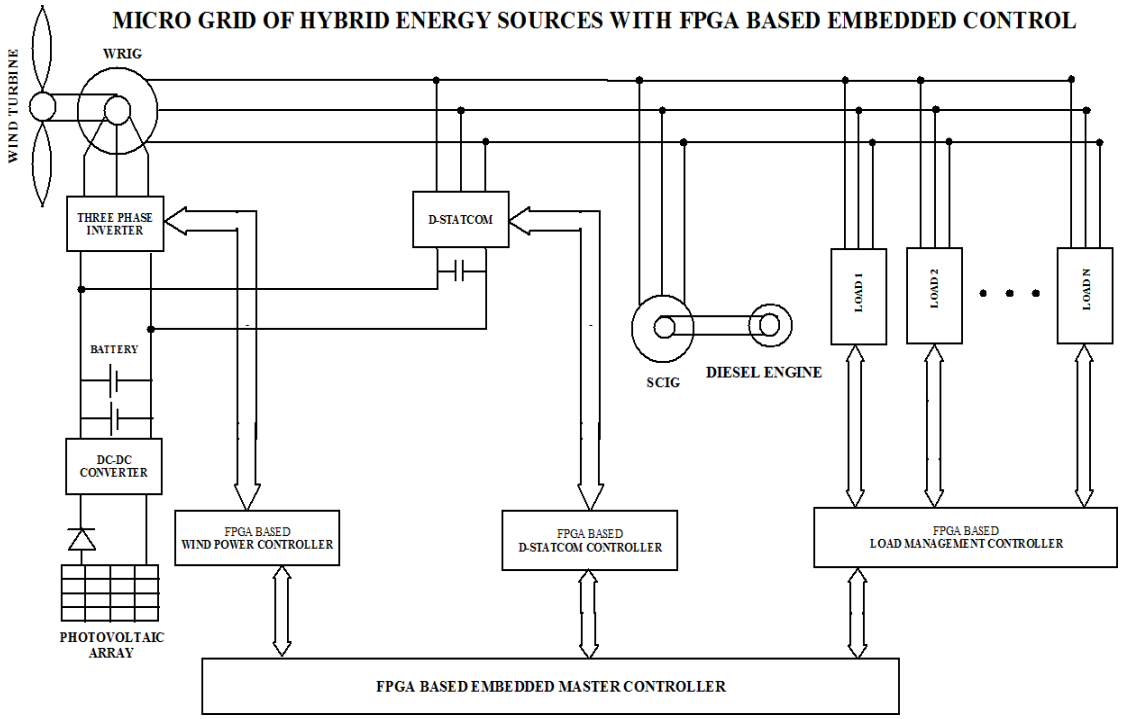


Fig. 1.5 Block diagram of the proposed system

Suitable digital controllers will be developed for controlling the rotor side inverter of WRIG, solar battery charger, DSTATCOM by employing embedded systems based on FPGA. DSTATCOM is also proposed to pump the power from solar PV- Battery system to the common load terminals. The logic for the load and source controller for the successful operation of the proposed system is also devised and furnished in this report. To demonstrate the working of the proposed micro grid system, prototype model has been developed in the laboratory and experimental results are presented in detail in the ensuing chapters.

Chapter 2 presents the working of a hybrid wind-solar system with exhaustive experimental results to demonstrate the working of the same under various operating conditions. These conditions can be a combination of high/low wind speeds, varying insolation levels and/or different load values in kW. A closed loop control strategy has been developed to maintain the terminal voltage and frequency of the WRIG and hence, the output power is

affected by both wind speed and load, while the solar PV panel output varies with incident irradiance and temperature.

Chapter 3 furnishes the parallel operation of the WRIG-SCIG system through experimental results. SCIG is driven by a DC motor (to emulate a bio-gas/diesel engine) at super-synchronous speeds and delivers the real power for the common load.

Chapter 4 presents the development details and working of DSTATCOM. The MATLAB simulation and FPGA based hardware realization are discussed. The synchronous reference frame theory has been utilized to compute the reference current for DSTATCOM. The modular development of synchronous reference frame theory and its realization in FPGA are given in detail. The working of DSTATCOM to compensate reactive power is demonstrated initially at lower voltage level and then at nominal operating voltage. Further, the algorithm for real and reactive power transfer through DSTATCOM has been developed and its working is verified along with WRIG system. The MATLAB simulation and prototype experimentation results showing reactive power transfer alone and subsequently, simultaneous real and reactive power transfer are presented in this chapter.

Chapter 5 presents the details of load controller for power management in the proposed system. The algorithm for power management has been developed and depicted as a flow chart in this chapter. The implementation of load controller in FPGA has been discussed in detail with schematic diagrams, and results are also displayed. Chapter 6 presents the simulation of the proposed hybrid system shown in Fig 1.5 under various operating conditions.

Chapter 2

HYBRID OPERATION OF WIND-DRIVEN WOUND ROTOR INDUCTION GENERATOR (WRIG) – SOLAR PV SYSTEM

2.1 INTRODUCTION

This chapter describes the operation and experimental investigations of the WRIG – solar PV system. The system proposed in this work for the operation of WRIG has only one bi-directional converter which is an SPWM inverter along with the battery at the rotor side. A simple control strategy has been developed for maintaining the set values of voltage and frequency at the stator, so that the consumer loads can be connected at this point. The control strategy proposed in this chapter uses the concept of indirectly controlling the magnitude and frequency of the air-gap emf of the WRIG by adjusting the rotor voltage magnitude and frequency. This does not involve any complex computation such as rotor flux and air-gap emf estimation. Since it depends only on the measured values of stator voltage and rotor speed, it is insensitive to the parameters of the machine i.e., free from parameter variation and so the co-ordinate transformations and rotor position detection, etc. are not required. The development of the closed-loop control for the proposed system has been given in detail and implemented using FPGA (Altium Nanoboard 3000XN.05) board. To assess the successful working of the proposed system, experiments have been conducted on a three-phase, 4 pole, 50 Hz, 3 hp, 415/185 V, 4.7 /7.5 A, Y-connected WRIM and results are presented.

The solar PV panels are connected to the batteries through boost converter. A perturb and observe (P&O) based MPPT algorithm has been developed and implemented for the solar PV system. The developed algorithm requires to monitor only the output current of the boost converter and its detail description has been given in this chapter. Thus, by appropriately operating the boost converter, the charging of the batteries is established employing solar PV panels. The complete experimental set-up has been built in the laboratory, both for WRIG and

solar PV systems. Extensive experimentation has been carried out to demonstrate the working of the proposed hybrid system and developed controllers and the results are furnished in this chapter. Starting from the description of the proposed system, control strategy and experimental investigations are explained in the succeeding sections.

2.2 DESCRIPTION OF THE PROPOSED SYSTEM

Fig. 2.1 shows the schematic of the proposed hybrid system employing wind-driven wound rotor induction generator (WRIG) and solar PV panels together with power electronic controllers. In this system, isolated loads are proposed to connect at the stator terminals of the WRIG. The rotor is fed through SPWM inverter supplied by batteries. The stator voltage magnitude and frequency are maintained constant for any rotor speed and load by appropriately adjusting the rotor voltage magnitude and frequency. The variation in rotor voltage magnitude and frequency is obtained by generating suitable modulation index and modulation frequency of SPWM inverter. The output power from the solar PV panels is aimed for charging the batteries. To enable the maximum power extraction from the solar PV panels, a boost converter is employed between the solar PV panels and batteries.

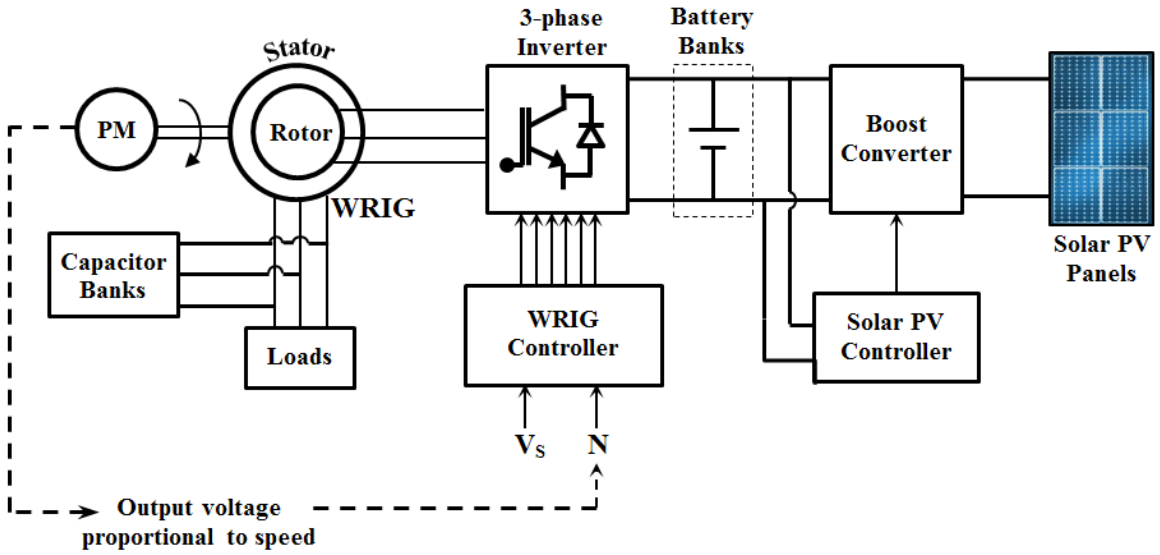


Fig. 2.1 Schematic of the wind-driven WRIG - solar PV system

2.2.1 WRIG CONTROL STRATEGY

Fig. 2.2 shows the closed-loop control strategy adopted for continuously feeding a variable voltage at slip frequency in the rotor terminals of WRIG for maintaining the set value of load voltage magnitude and frequency. The magnitude of the voltage to be injected in the rotor circuit is varied by adjusting the modulation index (m) of the rotor-side three-phase inverter fed through the battery bank powered by solar PV panels.

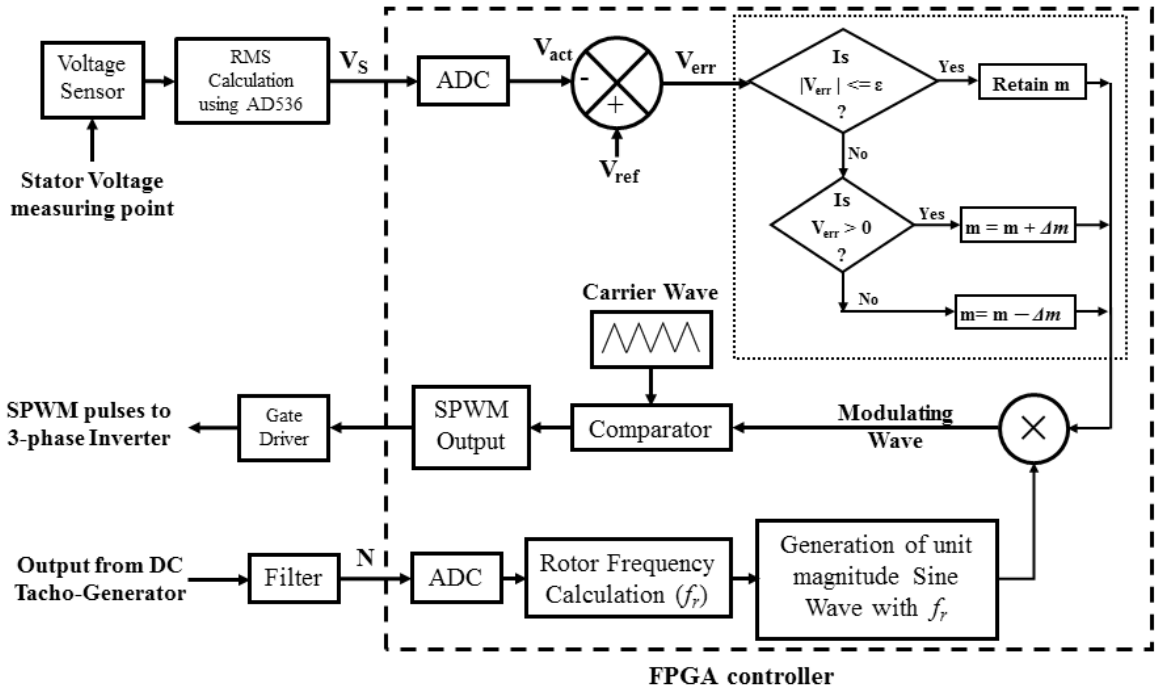


Fig. 2.2 WRIG control strategy

To arrive at the required modulation index value for the current operating point, the stator terminal voltage, V_s is considered as the control parameter. V_s is sensed using a Hall-effect voltage transducer (LV 25-P), and the RMS value of the same is obtained using an RMS-DC converter AD536. This signal is fed to the FPGA controller for evaluating the error in stator terminal voltage, V_{err}. The desired load terminal voltage, 415 V is taken as the reference value V_{ref}. Based on the sign of V_{err}, the magnitude of three-phase rotor winding voltage can be either increased or decreased by adjusting the 'm' of the rotor-side SPWM inverter. If V_{err} is positive,

the indication is that the load voltage is less than V_{ref}, hence magnitude of injected rotor voltage should be increased. Correspondingly, the 'm' of SPWM inverter must be increased to (m+ Δm). Similarly, for a negative value of V_{err}, 'm' of SPWM inverter is decreased to (m $-\Delta m$). The perturbation of MI, Δm is of the order of 0.01. When the stator voltage magnitude is within an acceptable limit, given by (V_{ref} ± 1%) V, the previous m value is retained.

In addition to the voltage magnitude, the frequency of the sinusoidal voltage injected into the rotor terminals must be equal to the slip times the stator frequency ($f_r = s\, f_s$). This can be achieved by setting the frequency of the reference sinusoidal signal for the SPWM inverter equal to f_r. For this, the shaft speed N is measured using a DC tacho-generator, from which f_r is calculated using (2.1).

$$f_r = f_s - (PN/120) \qquad (2.1)$$

where f_s is stator frequency (= 50 Hz), P is the number of poles of WRIG and N is the rotational speed of WRIG in rpm.

At high shaft speeds, the output of DC tacho-generator contains high frequency signals owing to the mechanical vibration of the machine, and the tacho-generator mount. To eliminate the unwanted noise, a second-order filter is employed. The output of the filter is a pure DC signal corresponding to the rotor speed. The magnitude of this signal varies from 0 to 5 V for a speed range of 0 to 3000 rpm. To feed this signal to the FPGA digital controller, an intermediate analog-to-digital converter (ADC) is required. The Altium Nanoboard 3000 has four onboard 8-bit ADC, which gives the equivalent digital value for the tacho-generator output. This 8-bit digital value is then read in the controller program, and shaft speed N is calculated, from which f_r is computed by using (2.1).

For SPWM pulse generation, a high frequency bipolar triangular waveform of unit magnitude is considered as the carrier signal. The magnitude of the modulating sinusoidal

waveform must be equal to the MI value obtained from the controller, and its frequency, f_r. For this purpose, a unit sinusoidal signal is generated at slip frequency, f_r internally, and multiplied with the obtained 'm' value using a multiplier. It is to be noted that the modulating signal consists of three sinusoidal waveforms at slip frequency, displaced by 120^o with each other. On comparing the magnitude of carrier and modulating signals, the SPWM pulses for all six IGBTs are generated, and obtained on the I/O pins of the FPGA controller.

The IGBT module ratings are listed in Table 2, wherein it can be observed that the gate-emitter voltage V_{GE} required for turning the device ON is 3 – 18 V. Although the output voltage of FPGA, 3.3 V is within the specified range, it will not be sufficient to drive the IGBT into saturation region for operating as a switch. Hence, an amplifier cum isolation IC ULN 2003A is employed, which amplifies the gate pulse magnitude to 15 V, as well as provides complete isolation of the triggering circuit and FPGA controller from the power circuit. The SPWM pulses from the gate driver circuit are fed to the corresponding gate-emitter terminals of the 3-phase IGBT inverter. The inverter then injects three-phase sinusoidal waveform of desired magnitude at slip frequency in the rotor terminals of the WRIG. The closed-loop controller thus warrants the virtual grid at the stator terminals by maintaining constant load voltage and frequency for any change in operating point of the system.

2.2.2 SOLAR PV CONTROL STRATEGY

In the proposed wind-solar system shown in Fig. 2.1, the solar PV panels are connected to the battery terminals through boost converter. Now it is of interest to develop a very simple control algorithm for tracking maximum power available in the solar PV panels. The proposed MPPT algorithm requires to monitor only the measured value of dc output current of the boost converter. This has become possible by the inherent stiff dc source of the battery i.e., the voltage at the boost converter output is dictated by the batteries and hence its value is virtually constant. So, for any variation in the PV panel output power will result in variation in the output

current of the boost converter. Therefore, for the solar PV system given in Fig. 2.1, MPPT algorithm has been developed only by sensing the boost converter output current. In addition, the proposed algorithm does not require the information of the solar irradiation and other parameters. Further, employing only one current sensor along with the simple power electronic topology offers the improved reliability in solar PV system for such battery charging application.

The proposed MPPT algorithm for the solar PV system shown in Fig. 2.1 is developed employing Perturb and Observe (P&O) method. As stated earlier, in this method, the controller senses the boost converter output current through a current sensor and compares it with the previous value. The result decides the change (increment or decrement) in the duty ratio of the boost converter. The duty ratio for the boost converter is thus adjusted in order to maintain the maximum output dc current of the boost converter and hence maximum power can be extracted from the solar PV panels. It is to be noted that the solar PV voltage and current are varied for extracting MP available as per its I-V characteristic for any operating conditions by adjusting the duty ratio of the boost converter and continuously monitoring the dc output current alone. The proposed MPPT algorithm has been implemented by using dsPIC30F4011 controller.

2.3. EXPERIMENTAL INVESTIGATIONS

To demonstrate the working and usefulness of the proposed system shown in Fig. 2.1, a prototype system has been designed and built in the laboratory. Table 2.1 gives the complete specifications of the experimental set-up for the system described in Fig. 2.1. A separately excited dc motor was used as a prime mover and suitable number of batteries was connected at the dc side of the inverter. The experiment was conducted for maintaining a constant voltage magnitude of 415 V (within ± 1 %) and frequency of 50 Hz (within ±0.5%) at the stator terminals.

Table 2.1
Specifications of experimental setup for the system shown in Fig. 2.1

Sl. No.	Component	Ratings
1.	Wound Rotor Induction Machine	3-phase, 4-pole, 3 HP; Stator: 415 V and 4.7 A, star-connection; Rotor : 185 V and 7.5 A, , star-connection.
2.	DC motor	220 V, 19 A, 5 HP and 1500 rpm
3.	SPWM Inverter	SEMIKRON make :V_{dc}= 750V, f = 20 kHz, output : 415V and 30A, 6 IGBT(SKM100GB12V) switches
4.	PV panel	P_{max}= 200W, V_{oc} =33V, I_{sc}=8.08A
5.	PV array	10 panels (arranged in 2 parallel paths, 5 panels in each path) P_{max}=2 kW, V_{oc}=165V, I_{sc}=16.16A)
6.	Boost converter	IGBT(IRGTI090U06): V_{CE}=600V, I_C=90 A, V_{CE}(ON)<3.0V & 25 kHz ; Diode (DSEI3006A):$I_{F(AV)}$ = 37A, V_{RRM} = 600V, trr = 35ns, Inductor: 10mH, 20A and Capacitor: 470 µF/450V
7.	Battery bank	17 batteries are connected in series. Each rated for a nominal voltage of 12 V and 100 Ah.

To stabilize the voltage at the input side of the boost converter (which was varying widely because of high frequency switching of IGBT in the boost converter), a 4µF/800V DC capacitor has been used. This value can be increased if significant voltage ripple is found at the boost converter input. The maximum and minimum value of duty ratio for the boost converter can be calculated using (2.2 - 2.3).

$$\delta_{max} = 1 - \frac{V_{PV(min)} \times \eta}{V_0} \quad (2.2)$$

$$\delta_{min} = 1 - \frac{V_{PV(max)}}{V_0} \quad (2.3)$$

where efficiency, $\eta = P_0/P_{PV}$, P_0 and P_{PV} are the output and input powers of the boost converter.

In the present system, boost converter is expected to operate with the minimum input voltage ($V_{PV(min)}$) of 90 V and maximum ($V_{PV(max)}$) of 160V with the nominal output voltage (V_0) of (200 ± 10%) V. Then, using (2.2) and (2.3), the maximum and minimum value of duty ratios are computed as 65% and 28% respectively with the minimum boost converter efficiency

(η) of 85%. The critical values of capacitor and inductor in the boost converter can be calculated using (2.4 - 2.5).

$$C_{cr} = \frac{I_{0(max)} \times \delta_{max}}{f \times \Delta V_0} \quad (2.4)$$

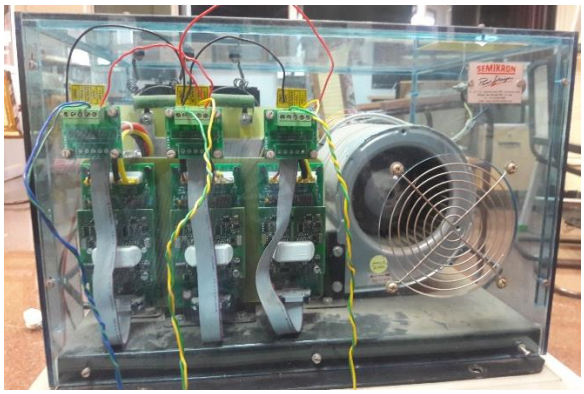
$$L_{cr} = \frac{V_{PV(min)} \times \delta_{max}}{f \times \Delta I_L} \quad (2.5)$$

For estimating the C_{cr} and L_{cr}, following design specifications are considered: the output voltage ripple (ΔV_0) should be less than 5 % and an inductor ripple current (ΔI_L) of less than 1 A for supplying the maximum output current (I_{0max}) equal to 10 A. The switching frequency (f) of the converter is 10 kHz. The critical values obtained with these design specifications are C_{cr} = 59µF and L_{cr} = 5.85mH. The values of capacitor and inductor should be more than C_{cr} and L_{cr} for continuous current mode operation of boost converter. Therefore, 470µF/450V capacitor and 10mH/20A inductor are used for this setup. The LEM make (LA-55-P) current sensor has been suitably designed to sense the output current of the boost converter for implementing the MPPT algorithm as described in the earlier section. The dsPIC30F4011 controller has been programed for the overall control of the solar PV system.

Fig. 2.3 shows the photograph of the various components of the experimental set-up built in the laboratory.

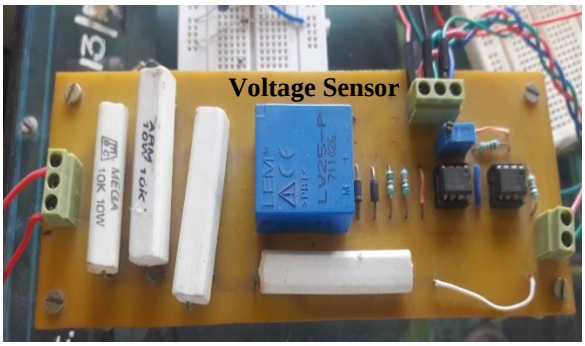
(a) DC motor coupled with WRIG along with the DC Tacho-generator

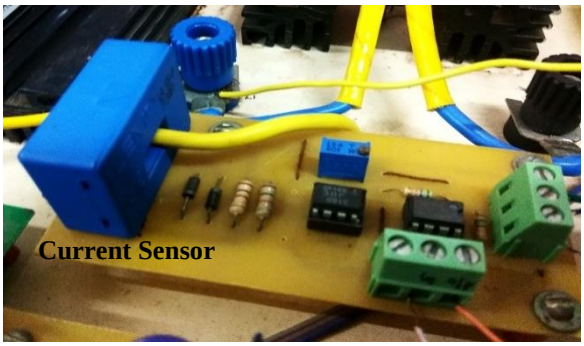
(b) 2 kW Solar PV panels arrangements



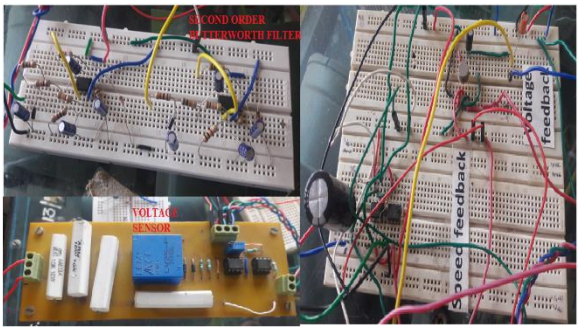
(c) SPWM inverter including gate drivers – side view of terminals, and top view

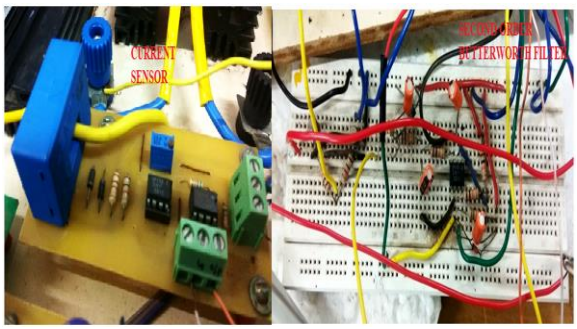
(d) Boost converter along with the controller



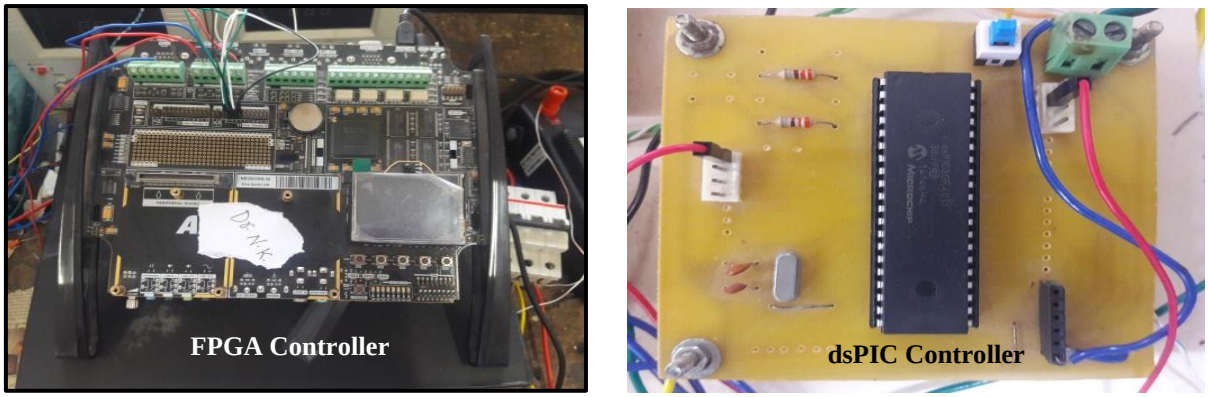


(e) Voltage and current sensor circuits



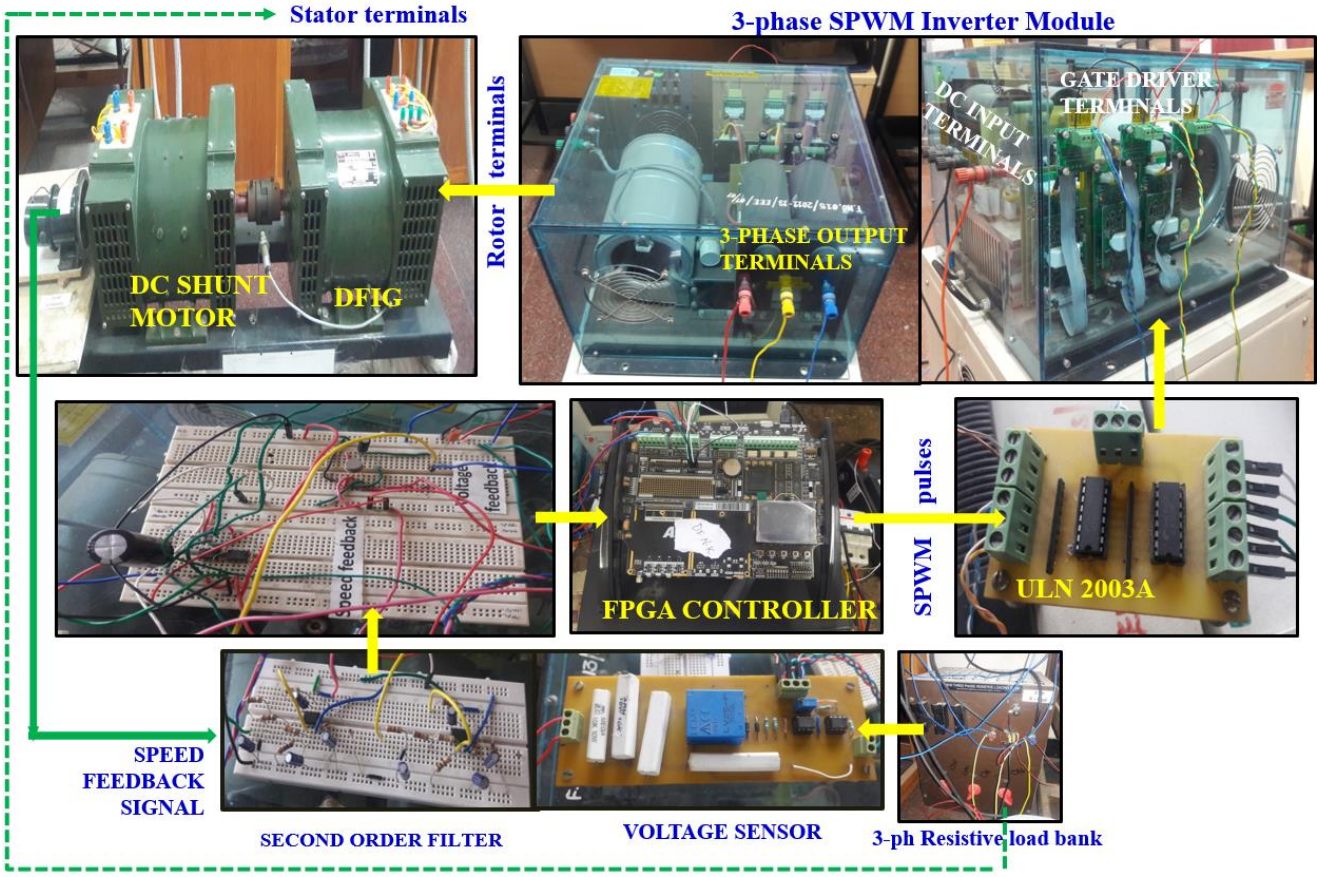


(f) Signal conditioning circuits for feedback signals



(g) FPGA board and dSPIC controller

(h) Electrical connections along with the measuring equipments



(i) Flow of electrical connections corresponding to Fig. 2.3 (h)

Fig. 2.3 Photograph of the experimental set-up

2.4. RESULTS AND DISCUSSIONS

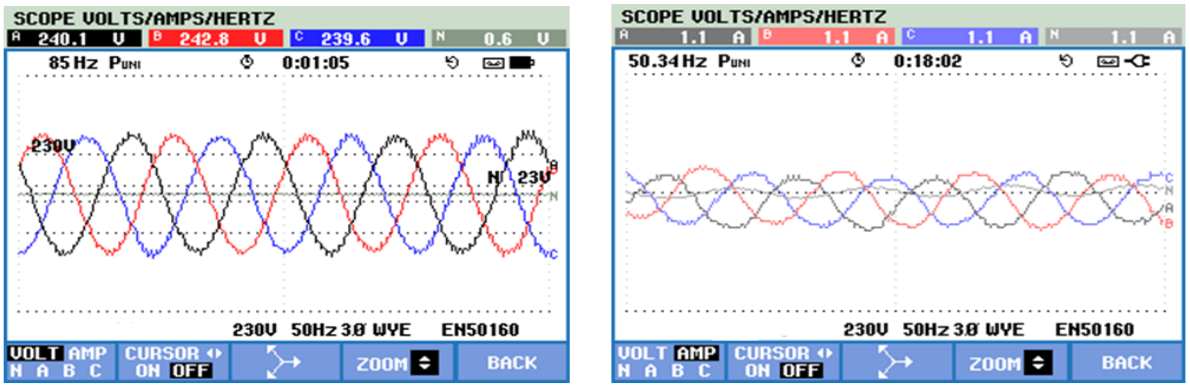
To demonstrate the working and usefulness of the proposed wind-solar hybrid system shown in Fig. 2.1, the prototype system described in the earlier section has been tested for different operating conditions. WRIG has been made to rotate with different speed settings using a separately excited DC motor and tested with different loads. The experimental results thus obtained are given in Table 2.2 for different load and speed settings. Figs. 2.4 to 2.6 shows the waveforms recorded at the various points of the WRIG system for three operating conditions. The details of the electrical quantities recorded are also clearly indicated in the figure. During this experimentation, the batteries shown in Fig. 2.1 were charged using the solar PV panels by appropriately operating the boost converter for extracting the MP available

in the solar PV system. The detailed experimental results obtained on the solar PV system will be described at the end of this sub-section.

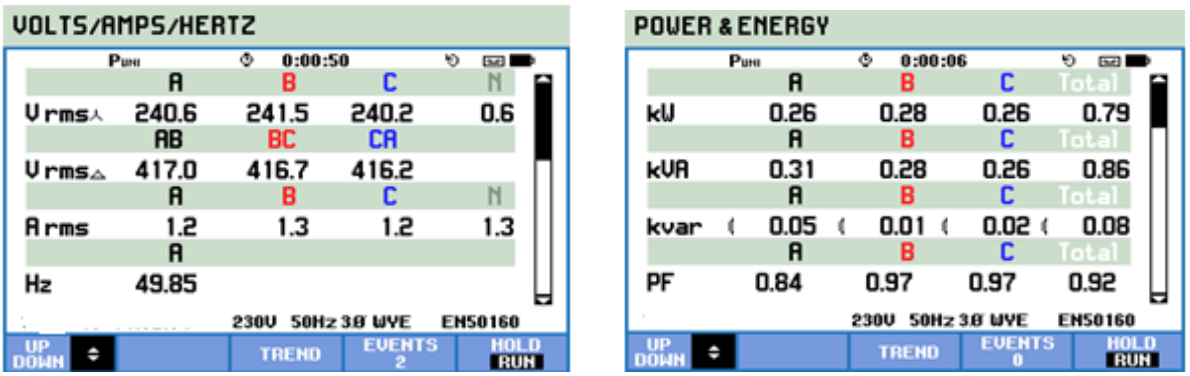
Table 2.2 Experimental results on a WRIG – Solar PV system with different operating conditions (conducted on 05.09.2018)

Load	Speed	DFIG Stator			DFIG Rotor				DC Motor		Battery		PV Panel			Boost Converter			Time
(W)	(rpm)	$V_{s\,L\text{-}L}$ (V)	I_s (A)	$P_{s\,3\text{-}ph}$ (kW)	$V_{r\,L\text{-}L}$ (V)	I_r (A)	$P_{r\,3\text{-}ph}$ (kW)	P.F. (Lag)	V_{DC} (V)	I_{DC} (A)	V_B (V)	I_B (A)	V_{PV} (V)	I_{PV} (A)	P_{PV} (W)	δ (%)	I_0 (A)	P_0 (W)	
750	1260	422.2	1.1	0.82	116.1	3.8	0.44	0.57	184	5.2	210	1.80	105	12.2	1281.0	52.0	5.85	1228.5	14:45
1500	1260	416.1	2.1	1.50	108.1	5.7	0.77	0.69	182	8.3	210	2.90	112	11.4	1276.8	48.0	5.21	1094.1	15:00
2250	1260	413.1	3.1	2.17	107.0	7.4	1.06	0.76	188	12.3	210	4.00	126	7.93	999.2	38.6	4.60	966.0	15:50
750	1360	416.2	1.3	1.81	113.5	3.5	0.40	0.61	196	5.0	210	2.10	130	7.91	1028.3	40.6	4.40	924.0	16:00
1500	1360	418.7	2.0	1.47	109.0	5.2	0.70	0.72	188	8.0	210	3.75	133	5.81	772.7	38.0	3.62	760.2	16:15
2250	1360	417.3	3.3	2.30	107.3	7.6	1.08	0.77	208	11.8	210	4.00	122	7.52	917.4	42.6	4.24	890.4	16:25

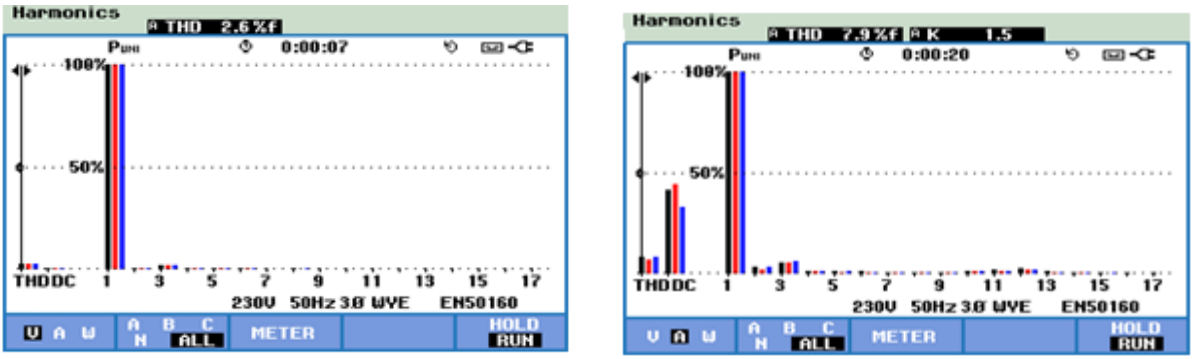
Note : Battery voltage = Boost converter output voltage



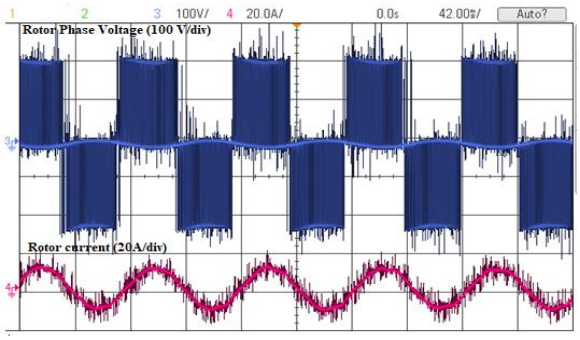
(a) Stator voltage and current



(b) Parameters of stator terminals measured by Power quality analyzer

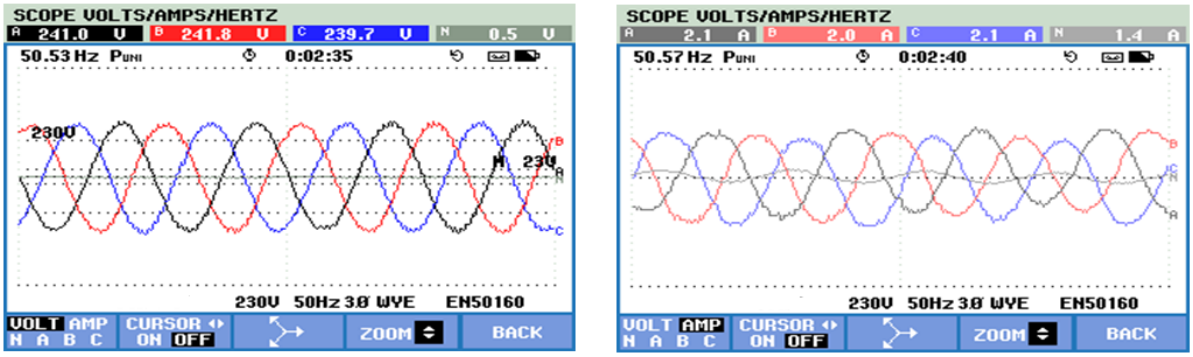


(c) Harmonic spectrum of load voltage and current

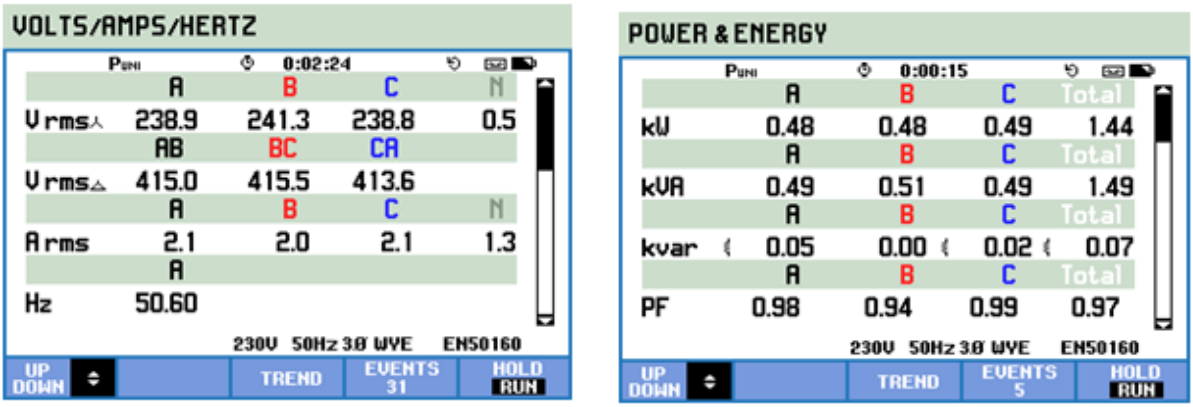


(d) Rotor terminal voltage and current

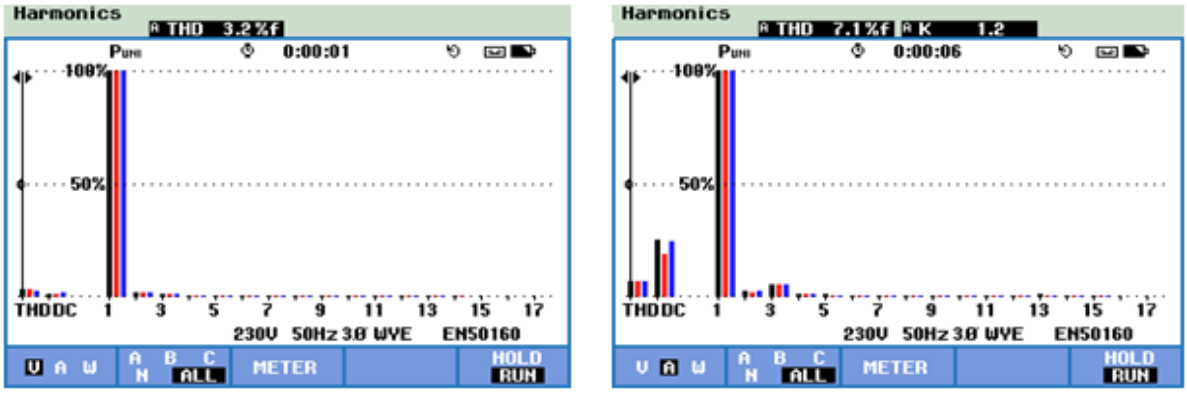
Fig. 2.4 Experimental results obtained on the WRIG system with P_L = 750 W and N=1150 rpm.



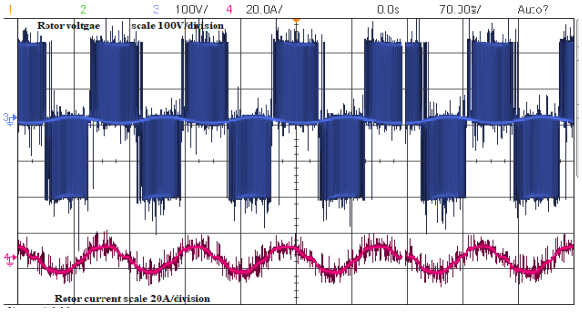
(a) Stator voltage and current



(b) Parameters of stator terminals measured by Power quality analyzer

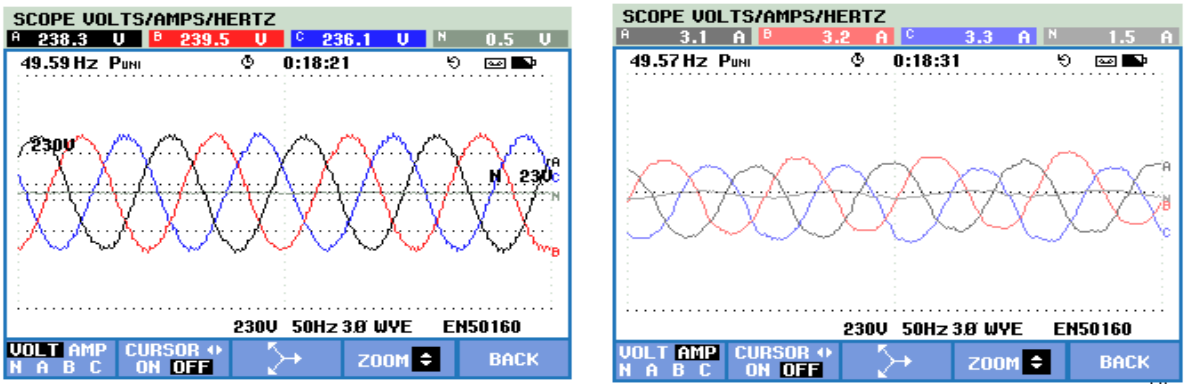


(c) Harmonic spectrum of load voltage and current

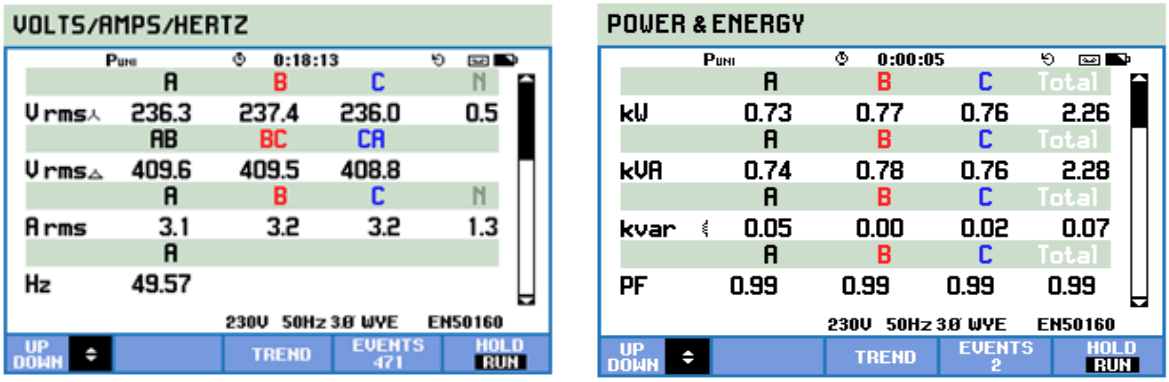


(d) Rotor terminal voltage and current

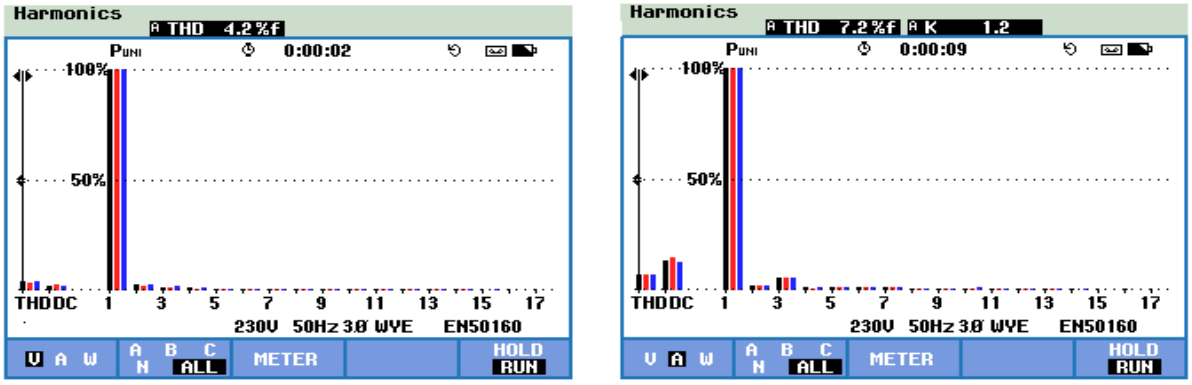
Fig. 2.5 Experimental results obtained on the WRIG system with P_L = 1.5 kW and N=1250 rpm.



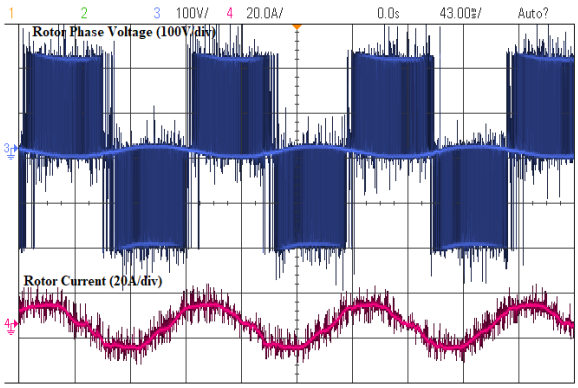
(a) Stator voltage and current



(b) Parameters of stator terminals measured by Power quality analyzer



(c) Harmonic spectrum of load voltage and current



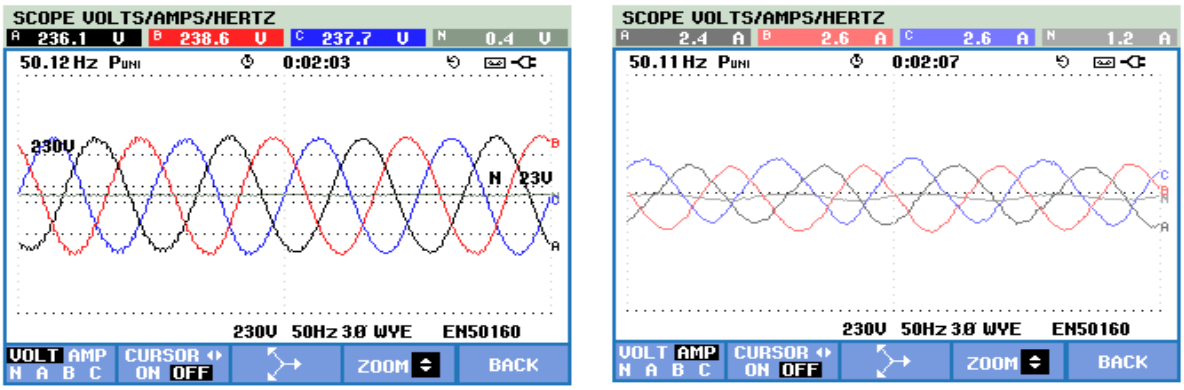
(d) Rotor terminal voltage and current

Fig. 2.6 Experimental results obtained on the WRIG system with P_L = 2.25 kW and N=1250 rpm.

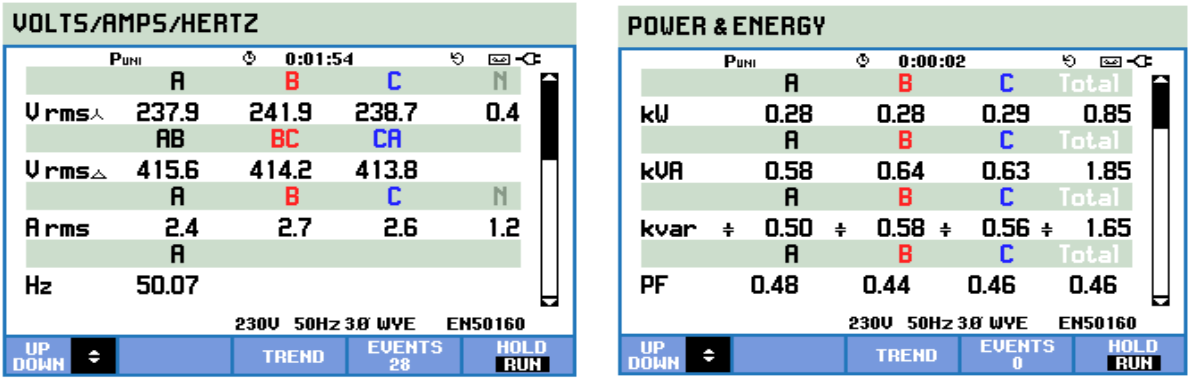
It has been observed from the test results that the WRIG control strategy maintains the stator voltage at 415 V (within the tolerance of ±1%) and frequency of 50 Hz (within the tolerance ±0.5%) for any operating conditions. This authenticates the formation of virtual grid at the stator terminals of WRIG for supplying isolated loads. Further, it can be viewed from Table 2.2 that the power supplied to the rotor increases with increase in load for the same speed. For the same load, rotor power decreases with increase in speed. In this test, the reactive power required to the WRIG has been met only from battery-SPWM inverter system at rotor side. So, to see the effect of supplying reactive power at stator side, testing has also been carried out by connecting a 2 kVAR delta-connected capacitor bank at the stator terminals and results are given in Table 2.3. For the sake of brevity, the waveforms recorded at the various points of the WRIG system for two operating conditions with capacitor at the stator side are given in Figs. 2.7 and 2.8. It can be observed from this Table and Figures that the rotor current decreases for the same speed and load as compared to no reactive power compensation at the stator. This also leads to decrease in the battery current and the value of reactive power from rotor. This indicates that the reactive power needed by the system can be optimally shared at the stator and rotor terminals of WRIG for improved performance.

Table 2.3 Experimental results of WRIG system for different load and speed settings with the addition of 2 kVAR capacitor at the stator side

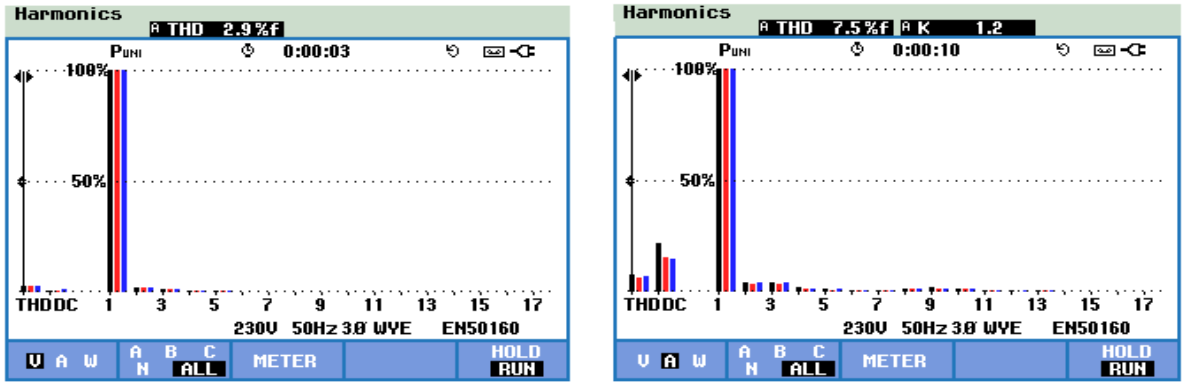
Sl. No.	Load (W)	Speed (rpm)	Stator side of WRIG				Rotor side of WRIG				DC Motor		Battery	
			V_{ph} (V)	I (A)	$P_{3\text{-}ph}$ (kW)	P.F. (Lead)	V_{ph} (V)	I (A)	$P_{3\text{-}ph}$ (kW)	P.F. (Lag)	V_{DC} (V)	I_{DC} (A)	V_B (V)	I_B (A)
1	750	1100	242.1	2.6	0.85	0.47	55.1	2.8	0.32	0.71	150	7.6	210	1.4
2	750	1150	240.4	2.6	0.85	0.47	48.0	3.0	0.25	0.66	156	7.6	212	1.4
3	750	1250	238.7	2.6	0.87	0.46	41.6	2.7	0.2	0.61	172	7.2	210	1.1
4	750	1350	242.2	2.6	0.81	0.45	37.2	2.7	0.13	0.54	194	6.8	211	0.8
5	750	1400	240.8	2.6	0.83	0.46	30.0	2.6	0.10	0.47	208	6.8	210	0.6
6	1500	1100	238.4	3.2	1.54	0.69	55.2	5.2	0.57	0.71	158	11.8	212	2.5
7	1500	1150	243.9	3.3	1.56	0.68	53.2	5.4	0.52	0.69	166	12.2	209	2.4
8	1500	1250	239.8	3.2	1.64	0.68	41.4	4.5	0.42	0.64	185	11.8	210	2.3
9	1500	1350	238.5	3.1	1.47	0.67	35.2	4.6	0.25	0.57	206	10.6	215	1.5
10	1500	1400	237.3	3.2	1.51	0.67	34.9	4.3	0.23	0.52	212	10.6	210	1.4
11	2250	1150	239.7	4.1	2.59	0.82	53.6	7.6	0.98	0.71	184	18.2	210	4.5
12	2250	1250	239.7	4.1	2.24	0.81	47.2	7.2	0.64	0.67	202	15.6	211	3.2
13	2250	1350	242.4	4.1	2.30	0.80	42.5	7.2	0.55	0.62	214	16.0	212	2.9
14	2250	1400	238.4	4.1	1.78	0.81	36.2	6.8	0.34	0.54	216	13.0	210	1.9



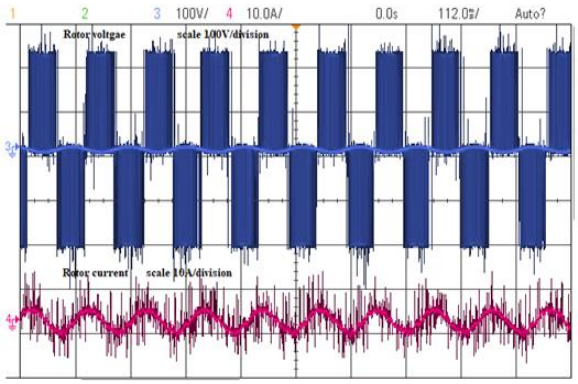
(a) Stator voltage and current



(b) Parameters of stator terminals measured by Power quality analyzer

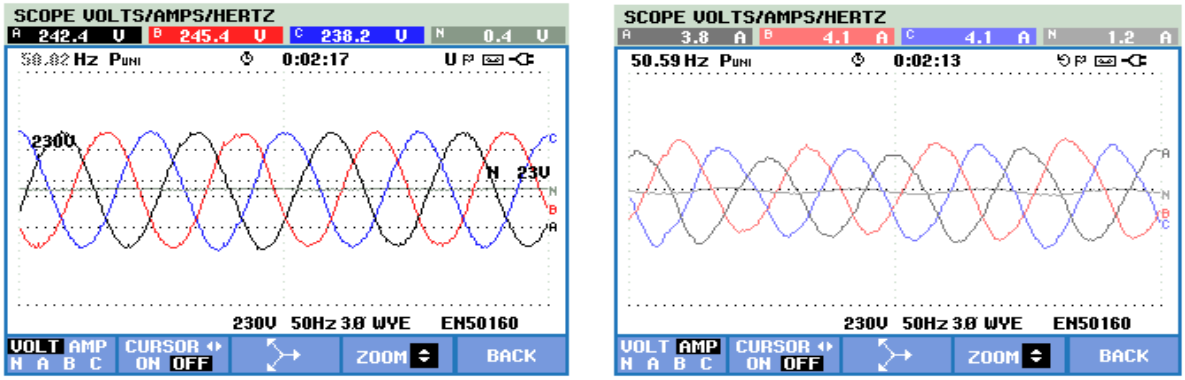


(c) Harmonic spectrum of load voltage and current

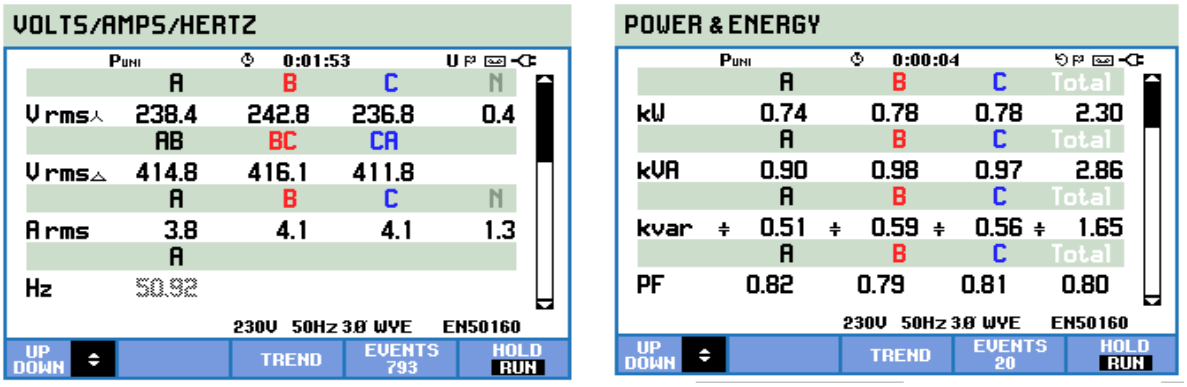


(d) Rotor terminal voltage and current

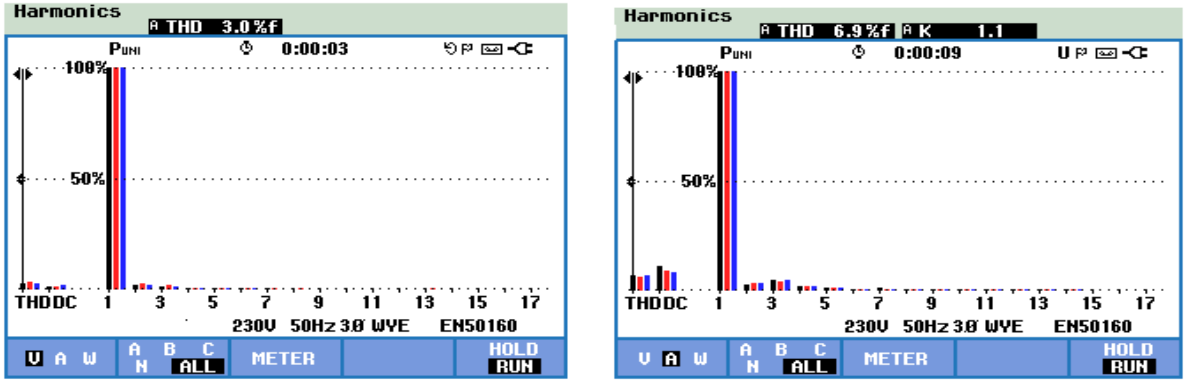
Fig. 2.7 Experimental results obtained on the WRIG system with P_L = 750 W and N=1250 rpm, with 2 kVAR capacitor bank (delta-connected).



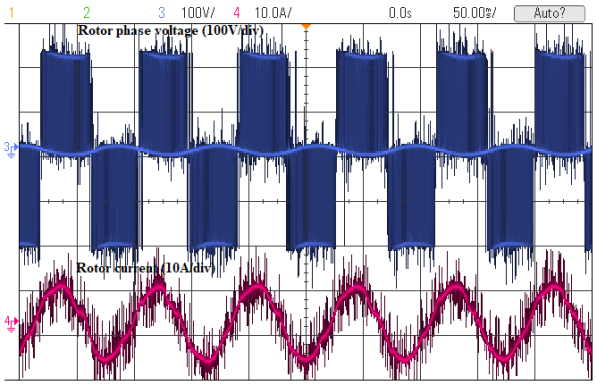
(a) Stator voltage and current



(b) Parameters of stator terminals measured by Power quality analyzer



(c) Harmonic spectrum of load voltage and current



(d) Rotor terminal voltage and current

Fig. 2.8 Experimental results obtained on the WRIG system with P_L = 2.25.kW and N=1350 rpm, with 2 kVAR capacitor bank (delta-connected).

To substantiate the satisfactory dynamic performance of the proposed system, the controller has been tested with (i) step change in load and (ii) step change in speed. Figs. 2.9 and 2.10 gives the experimental results obtained with such testing conditions, one for step change in load and the other for step change in speed. The results shown in Fig. 2.9 correspond to a running speed of 1300 rpm. It can be observed that the battery bank current changes from 1.9 A to 1.5 A when load changes from 0.75kW to no-load and 1.5 A to 2.1 A when load changes from no-load to 1.5 kW. Also, the stator terminal voltage reaches the set steady-state value. Fig. 2.10 shows the dynamic response of the system feeding a load of 1.5 kW.

The experimental results given in Figs. 2.4 to 2.10 and Tables 2.2 and 2.3, validate the successful working of the WRIG control strategy developed in this paper for supplying isolated loads.

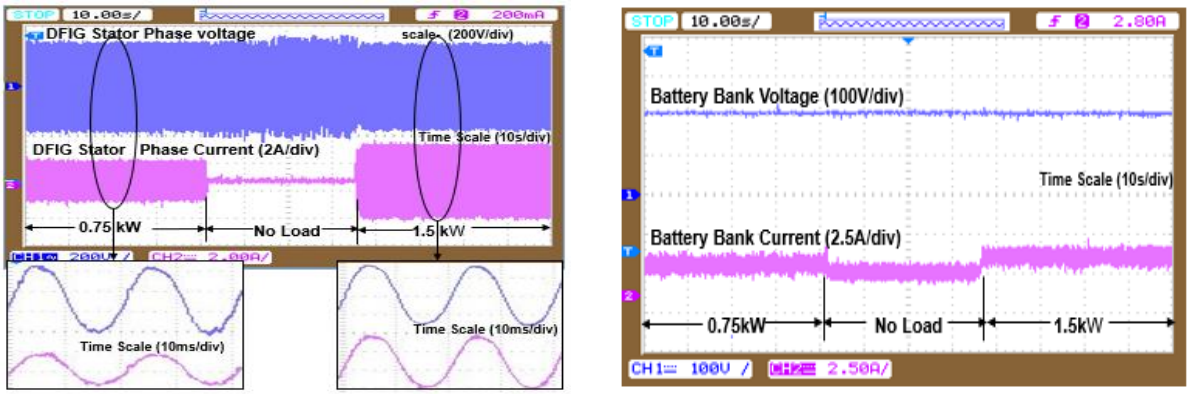


Fig. 2.9 Step change in load

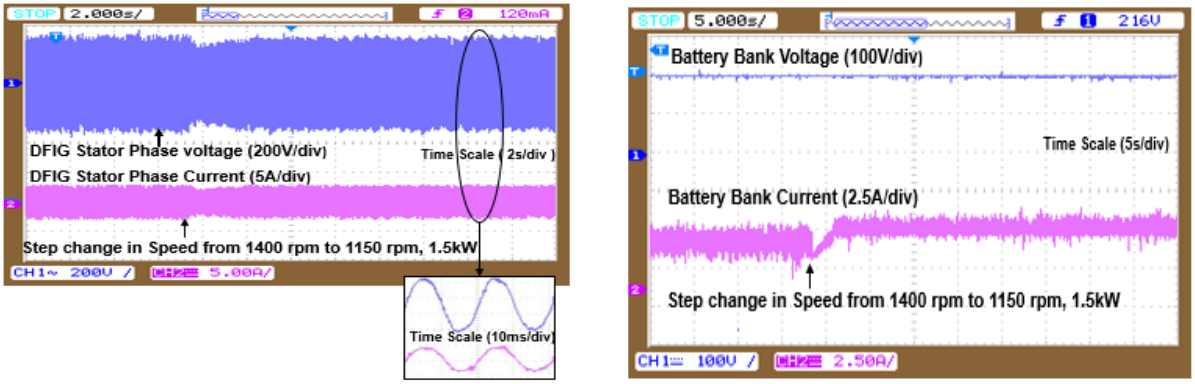
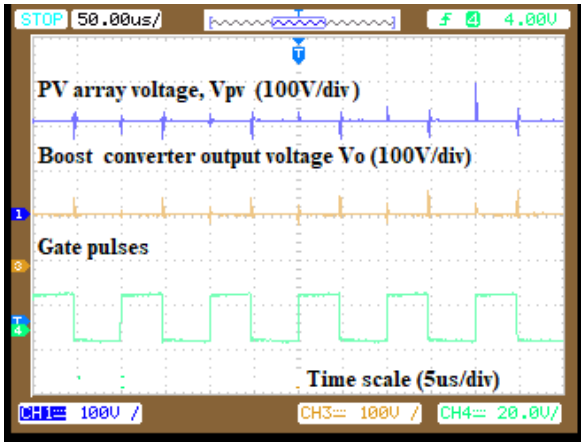
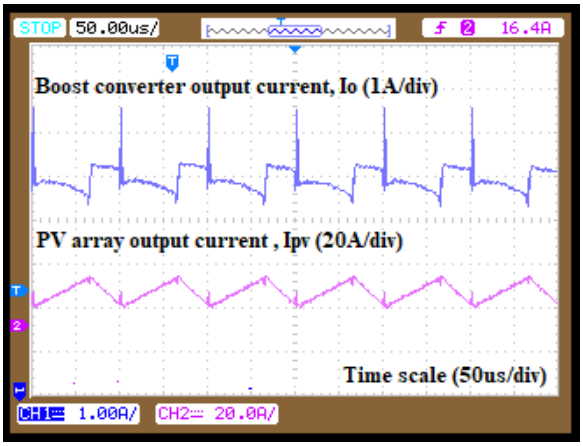


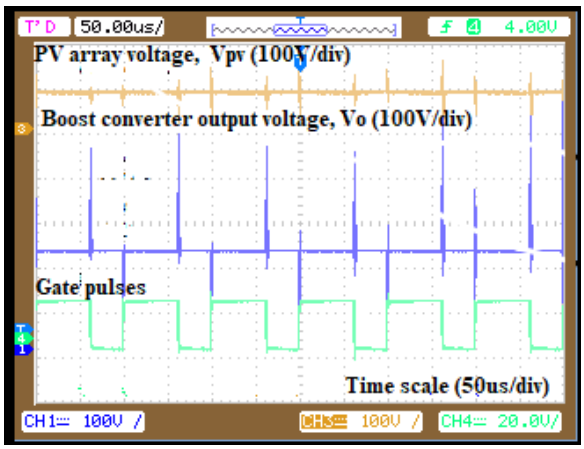
Fig. 2.10 Step change in speed

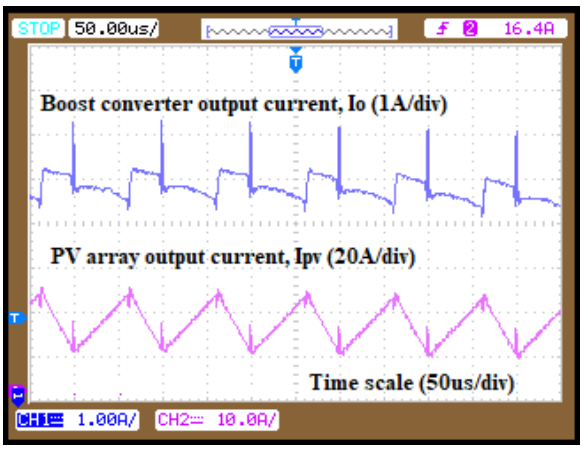
As stated earlier, testing of the WRIG system has been carried out in the laboratory along with solar-PV system feeds power to the batteries. The testing of the solar PV system has been carried out in the actual operating condition on 20.9.2017. Fig. 2.11 shows one set of waveforms captured at the input and output side of the boost converter along with the gating pulses. Table 2.4 shows the steady-state test results of the solar-PV system. This table gives the variation of duty ratio of the boost converter, the output power from the solar PV panels and power supplied to the battery at MPPT condition. This table also gives the corresponding variations of voltage and current at the input and output side of the Boost converter. Here the boost converter output voltage is almost constant at 220 V. Hence, the output current of boost converter is varied between the minimum of 2.4 A to a maximum of 5.6 A for achieving the MPPT condition. Solar PV voltage varies from 95 V to 133 V with the corresponding current variation of 15 A and 4.6 A, respectively. Thus, Table 2.4 and Fig. 2.11 demonstrate that the developed MPPT algorithm, which adjusts the duty ratio of the converter in a closed-loop to extract the maximum power from the solar PV panels. Table 2.4 also indicate the efficiency of the boost converter, which is always more than 85 %. This validates the design procedure described in the report for boost converter.



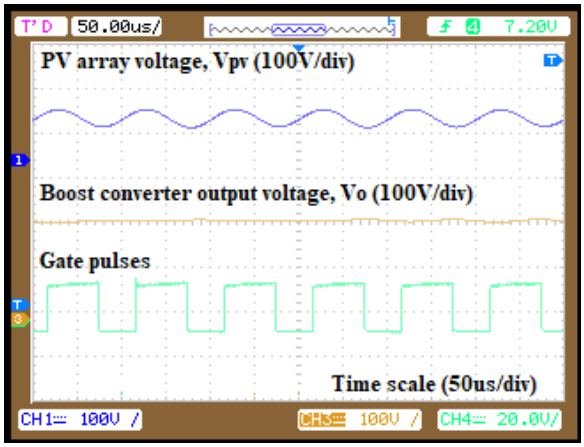


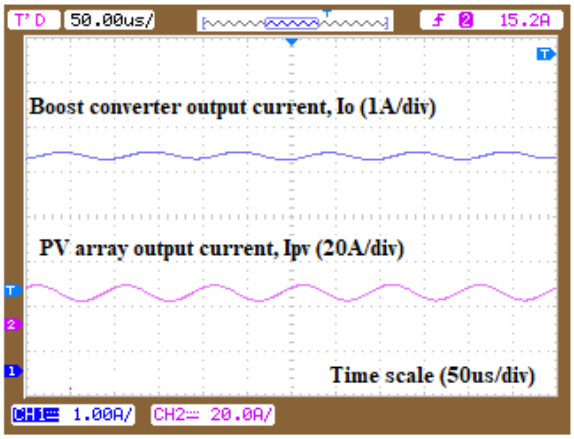
(a) Voltage and current waveforms captured on 20.09.2017 at 10:50 am



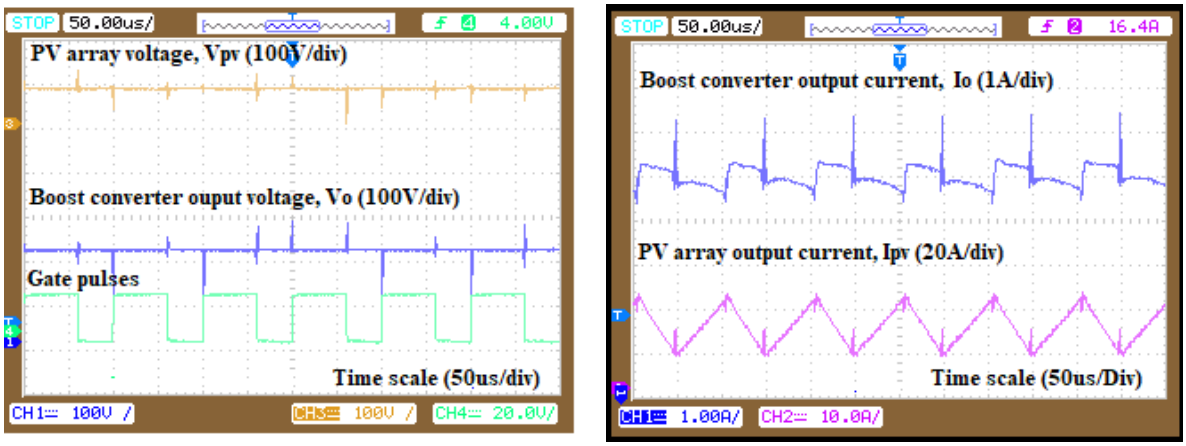


(b) Voltage and current waveforms captured on 20.09.2017 at 10:50 am

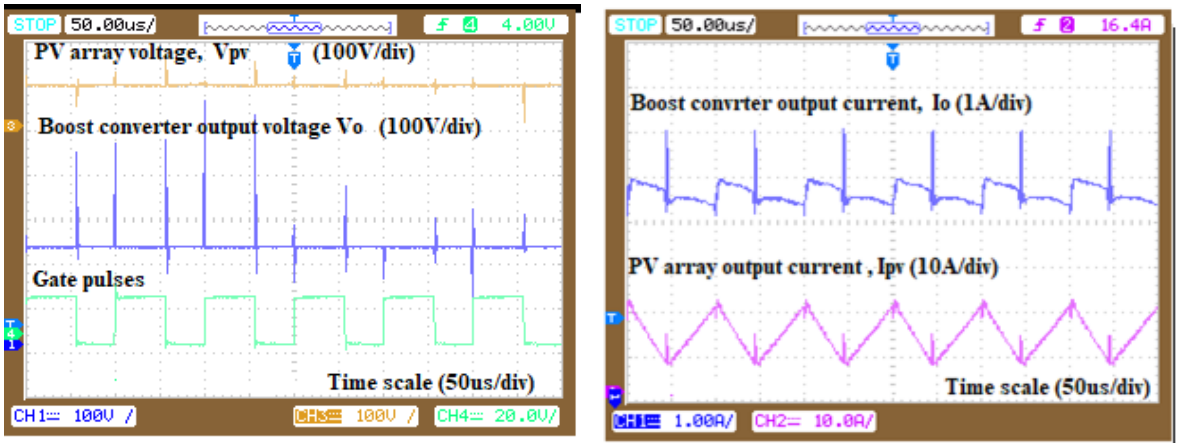




(c) Voltage and current waveforms captured on 20.09.2017 at 12:35 pm (Experimental waveforms recorded using DSO with digital low pass filter enabled)



(d) Voltage and current waveforms captured on 20.09.2017 at 01:30 pm



(e) Voltage and current waveforms captured on 20.09.2017 at 03:00 pm

Fig. 2.11 Experimental results obtained from the solar-PV system

Table 2.4 Experimental readings for solar PV system (Taken on 20-09-2017)

Sl. No.	Time	PV Panel			Boost Converter				Total losses (W)	Conduction loss in inductor (W)	Efficiency (%η)
		Voltage V_{PV} (V)	Current I_{PV} (A)	Power P_{PV} (W)	δ (%)	Voltage V_0 (V)	Current I_0 (A)	Power P_0 (W)			
1	09:50	109	10.8	1177.2	53.0	216	4.7	1015.2	162.0	69.98	86.24
2	10:15	108	11.6	1252.8	53.5	220	4.9	1078.0	174.8	80.74	86.05
3	10:25	106	12.0	1272.0	54.5	220	5.0	1100.0	172.0	86.40	86.48
4	10:40	105	12.8	1344.0	55.0	220	5.1	1122.0	222.0	98.30	83.48
5	10:50	103	13.2	1359.6	57.0	220	5.2	1144.0	215.6	104.54	84.14
6	11:05	100	14.0	1400.0	58.0	220	5.5	1210.0	190.0	117.60	86.43
7	11:20	98	14.6	1430.8	60.0	220	5.6	1232.0	198.8	127.90	86.11
8	11:45	97	14.8	1435.6	62.5	220	5.5	1210.0	225.6	131.42	84.29
9	12:10	95	15.0	1425.0	63.0	220	5.5	1210.0	215.0	135.00	84.91
10	12:35	102	13.8	1407.6	56.0	220	5.2	1144.0	263.6	114.26	81.27
11	12:50	101	14.0	1414.0	57.0	220	5.3	1166.0	248.0	117.60	82.46
12	13:30	97	14.4	1396.8	61.0	220	5.6	1232.0	164.8	124.42	88.20
13	14:15	100	14.6	1460.0	58.0	220	5.7	1254.0	206.0	127.90	85.89
14	14:30	103	12.8	1318.4	56.5	220	5.0	1100.0	218.4	98.30	83.43
15	15:00	106	11.8	1250.8	54.0	220	4.7	1034.0	216.8	83.54	82.67
16	15:10	111	10.2	1132.2	52.5	220	4.4	968.0	164.2	62.42	85.50
17	15:25	117	9.0	1053.0	49.0	220	4.1	902.0	151.0	48.60	85.66
18	15:45	121	8.0	968.0	48.0	218	3.7	806.6	161.4	38.40	83.33
19	15:55	125	6.8	850.0	46.0	217	3.4	737.8	112.2	27.74	86.80
20	16:15	133	4.6	611.8	41.0	214	2.4	513.6	98.2	12.70	83.95

Note: (1) Output power from solar PV panels = Input power at the boost converter,

(2) Battery power = Output power of boost converter,

(3) PV panel voltage = Boost converter input voltage,

(4) Battery voltage = Boost converter output voltage,

(5) PV panel current = Boost converter input current and

(6) Battery current = Boost converter output current

2.5. SUMMARY

This chapter has described the operation of proposed hybrid wind-solar system employing WRIG and solar PV system. The closed-loop controller for the operation of WRIG and solar PV MPPT have been developed and implemented using digital controllers. Extensive experimentation has been carried out and the results obtained on the proposed hybrid wind-

solar system together with the developed controllers demonstrate their successful working and viability of the proposed system for feeding isolated loads.

To develop the operation of WRIG and associated controllers, initially, detailed study has been carried out with the machine available in the laboratory, and the outcome of these studies as part of this project are published in the following research journals and conferences:

1. K. A. Nikhil, P. Bharath Chandra, M. R. Jawahar, S. Moorthi, M. P. Selvan and N. Kumaresan, "FPGA-based closed-loop monitoring and control of doubly fed induction generator with single inverter and battery for wind energy conversion", Australian Journal of Electrical and Electronics Engineering, Vol. 15, Issue. 4, 2018, pp. 175–183. (Print ISSN: 1448-837X Online ISSN: 2205-362X)

2. K. Navin Sam, N. Kumaresan, N. Ammasai Gounden and Rajesh Katyal, "Analysis and control of wind-driven stand-alone doubly-fed induction generator with reactive power support from stator and rotor side" *International journal of Wind Engineering*, Vol.39, No.1, 2015, pp.97-112. (ISSN: 0309-524X).

3. K. Vijayakumar, N. Kumaresan and N. Ammasaigounden, "Operation of inverter assisted wind-driven slip-ring induction generator for stand-alone power supplies", *IET Electr. Power Appl.*, Vol.7, Issue. 4, 2013, pp.256-269. (SCIE indexed: ISSN: 1751-8660).

4. K. Vijayakumar, N. Kumaresan and N. Ammasaigounden, "Operation and closed-loop control of wind-driven stand-alone WRIGs using single inverter-battery system", *IET Electr. Power Appl.*, Vol. 6, Issue. 3, 2012, pp. 162-171. (SCIE indexed: ISSN: 1751-8660).

5. N. Sekhar, P. Lakshmana Rao, N. Kumaresan, and M. P. Selvan, "Experimental Investigation on Operation of Stand-alone Wind-driven WRIG-Solar PV System" Proceedings of Thirty-third National Convention of Electrical Engineers 2017 (NCEE 2017) & National Conference on "Hybrid AC/DC Power Systems for Effective Utilization of Renewable Energy" organized by IE(India), held on 24th and 25th November 2017, at National Institute of Technology, Tiruchirappalli, pp.182-186. – (secured **best paper award**).

6. M.S. Suhanya, A. Tirumalendra Reddy and N. Kumaresan, "Analysis and Simulation of Standalone WRIG Employing a Battery Single Inverter Scheme" Proceedings of Thirty-third National Convention of Electrical Engineers 2017 (NCEE 2017) & National Conference on "Hybrid AC/DC Power Systems for Effective Utilization of Renewable Energy" organized by IE(India), held on 24th and 25th November 2017, at National Institute of Technology, Tiruchirappalli, pp. 91-95.

The next chapter describes the experimental investigations of the present system operated in parallel with bio-mass/diesel driven squirrel-cage induction generator.

Chapter 3

PARALLEL OPERATION OF WRIG AND SQUIRREL-CAGE INDUCTION GENERATOR (SCIG) ALONG WITH SOLAR PV SYSTEM

3.1 INTRODUCTION

This chapter describes the experimental investigations on the parallel operation of wind-driven Wound Rotor Induction Generator (WRIG) and bio-mass/diesel engine driven Squirrel-Cage Induction Generator (SCIG) along with the solar PV system for supplying isolated loads. The WRIG control strategy developed in this work (described in Chapter 2) has been used for maintaining the set values of voltage and frequency at the stator terminals of WRIG, so that the consumer loads and SCIG can be connected at this point. SCIG is proposed to operate only when the wind and solar energies are not sufficient to meet the consumer demand. A prototype system has been developed in the laboratory for demonstrating the successful working of the proposed system. Experimental results obtained on the prototype system in the laboratory for various operating conditions are furnished in this chapter.

3.2 DESCRIPTION OF THE PROPOSED SYSTEM

Fig. 3.1 shows the block diagram of the parallel operation of SCIG with Hybrid wind-solar system described in Fig. 2.1. This system consists of (i) wind-driven WRIG with an SPWM inverter-battery bank connected at the rotor terminals, (ii) solar PV system with MPPT controller, (iii) SCIG coupled with diesel engine/ bio-mass driven engine, and (iv) isolated ac loads. The excitation of the rotor of the wind-driven WRIG is established using a single inverter which is a Sinusoidal Pulse Width Modulation (SPWM) inverter supplied through set of batteries. The stator terminals of both machines (WRIG and SCIG) and isolated ac loads are connected together, which forms the Point of Common Coupling (PCC). At PCC, the voltage

magnitude and frequency are maintained constant for any operating conditions by employing the WRIG control strategy described in the previous chapter. It is to be noted that the SCIG is directly connected to the PCC (without out any power electronic controller) and hence it has to be rotated more than its synchronous speed for operating as a generator. So, based on the rotational speed, the SCIG will supply the real power at PCC and takes reactive power for its operation.

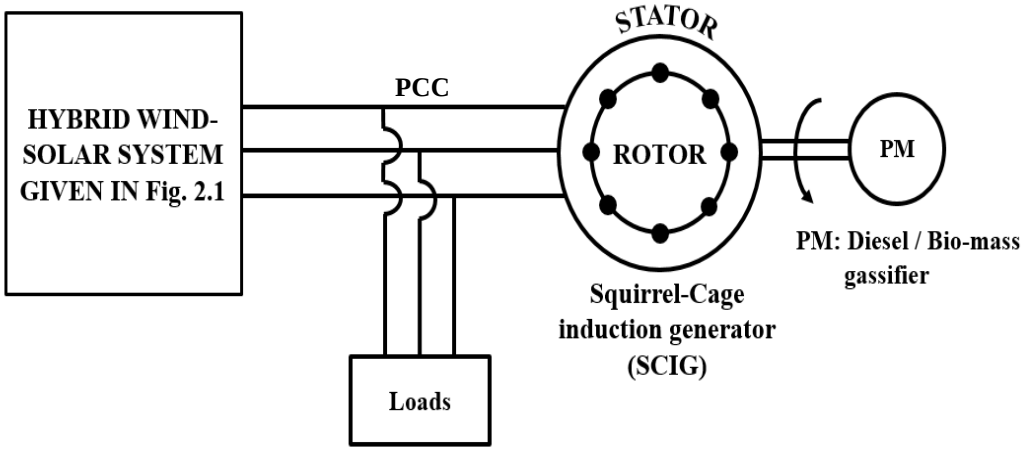


Fig. 3.1 Block diagram of parallel operation of SCIG with Hybrid wind-solar system given in Fig. 2.1.

3.3 RESULTS AND DISCUSSIONS

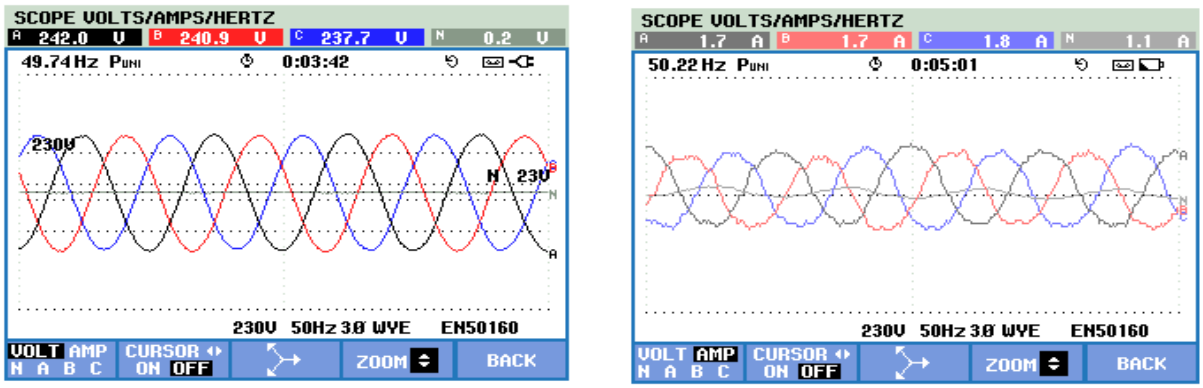
To illustrate the working of the proposed system shown in Fig. 3.1, experiments have been conducted on the prototype system developed in the laboratory. The technical specifications for the WRIG and solar PV system are given in Chapter 2. A 3-phase, 4-pole, 415 V, 50 Hz, 3 hp, star-connected stator has been considered for SCIG. As stated earlier, a separately excited DC motor was used as the prime mover to drive WRIG. Similarly, SCIG has been coupled with a separately excited DC machine for the emulation of Diesel engine.

Experiment was conducted for different loads at the PCC and operating the WRIG and SCIG at different speeds. The experimental results thus obtained are given in Table 3.1 for two load settings at PCC. However, apart from this, the WRIG and SCIG were operated with different speeds. Throughout the experiment, 415 V, 50 Hz has been maintained at the PCC by WRIG control strategy described in the previous chapter. It can be observed from the Table 3.1 that the total load at the PCC has been shared by WRIG and SCIG. Further, the power supplied by the SCIG is increasing with its rotational speed. To have the power balance, the power supplied by the WRIG decreases even if it is operating at a constant speed. The voltage and currents waveforms were also recorded and recorded values for three operating conditions are given in Figs. 3.2 to 3.4. The details of the electrical quantities recorded are also clearly indicated.

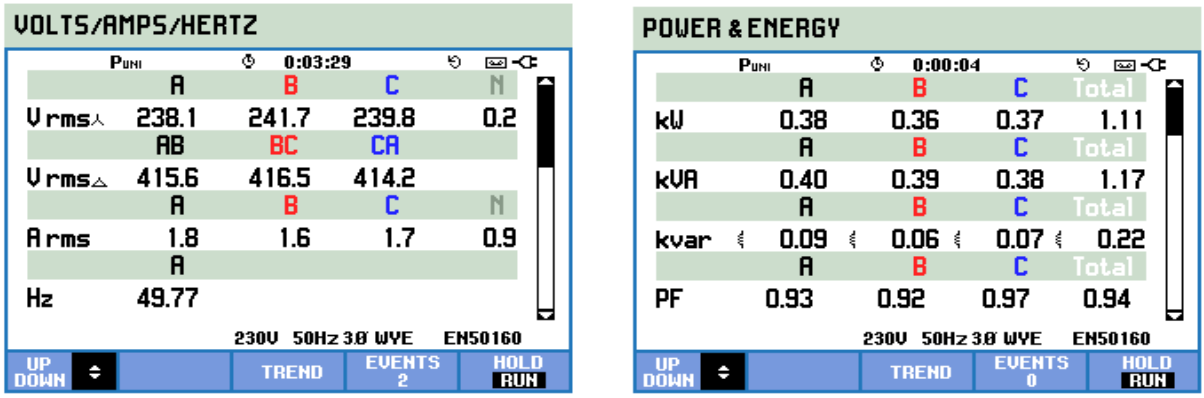
In the proposed scheme, SCIG is to take load only if wind/solar generation is not sufficient to meet the load. To emulate such situation, wherein load is fully supplied by WRIG plus PV, and SCIG just floating across the microgrid drawing reactive power alone. So, to show the operation of the proposed system, under this condition, experiments have been conducted, and results are given in Table 3.2 and Figs. 3.5 and 3.6. For this experiment, SCIG was rotated at synchronous speed (i.e., at 1500 rpm) by the prime mover. SCIG currents were measured for the generator convention. It is to be noted from the results that SCIG takes a small amount of power for compensating the iron loss of the machine. To clearly show that SCIG is just floating and drawing reactive power, (i.e., the phase angle difference between the voltage and current is 90 degree), the enlarged version of the stator voltage and current is also shown with this result.

Table 3.1 Experimental results of parallel operation of WRIG sand SCIG

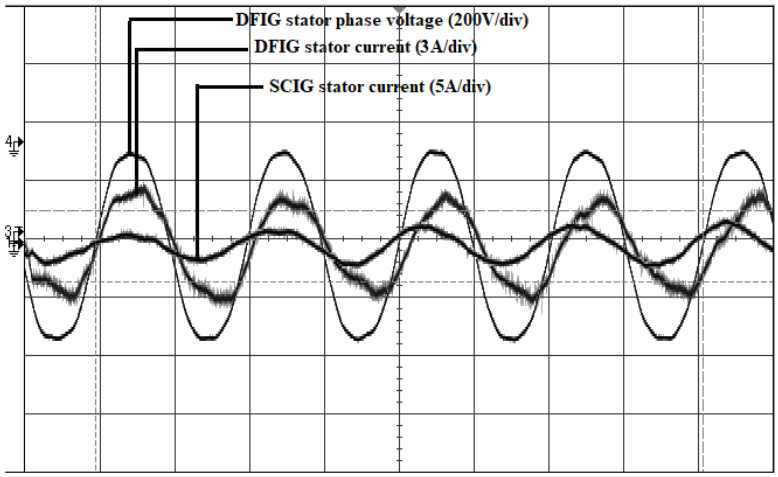
Load (W)	DFIG											SCIG							Battery	
	Speed (rpm)	DC Motor		Stator				Rotor				Speed (rpm)	V_{L-L} (V)	I (A)	P.F. (Lag)	P_{3-ph} (W)	DC Motor		V_B (V)	I_B (A)
		V_{DC} (V)	I_{DC} (A)	V_{L-L} (V)	I (A)	P_{3-ph} (kW)	P.F. (Lag)	V_{L-L} (V)	I (A)	P_{3-ph} (kW)	P.F. (Lag)						V_{DC} (V)	I_{DC} (A)		
750	1300	190	4.8	411.6	0.8	0.45	0.81	62	8	0.39	0.48	1520	411.6	2.5	0.2	356.45	220	5.2	205	1.8
750	1300	190	7.4	421.4	0.7	0.27	0.64	64.8	7.9	0.36	0.45	1540	421.4	2.8	0.28	572.23	215	6.4	204	1.6
750	1300	184	5.6	418.8	0.8	0.1	0.23	66.1	7.2	0.41	0.46	1550	418.8	3	0.36	783.41	215	7.9	205	1.5
1500	1250	184	8.4	415.6	1.8	1.11	0.94	77.7	9.1	0.69	0.56	1515	415.6	2.5	0.2	359.92	218	5.2	205	2.8
1500	1250	180	6.4	414.9	1.3	0.78	0.89	74.8	8.7	0.61	0.52	1530	414.8	2.8	0.35	704.08	215	7.2	205	2.8
1500	1250	178	4.8	413.4	1.0	0.48	0.61	77.3	8.3	0.56	0.5	1550	413.4	3.2	0.46	1053.99	212	9.2	205	2.4
1500	1250	174	3.4	414.8	1.0	0.21	0.34	73.3	9.0	0.59	0.49	1570	414.8	3.6	0.53	1370	212	12	205	2.2



(a) WRIG Stator phase voltage and current, respectively

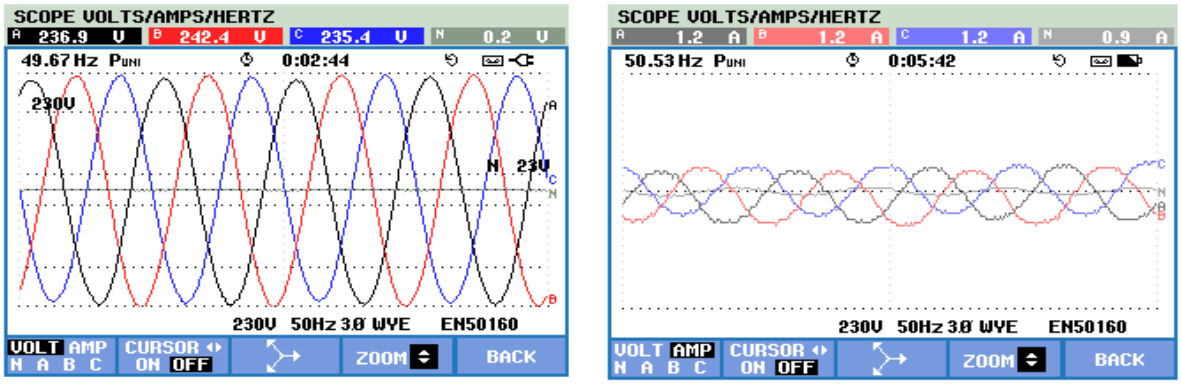


(b) Power quality analyzer displaying parameters at WRIG stator terminals

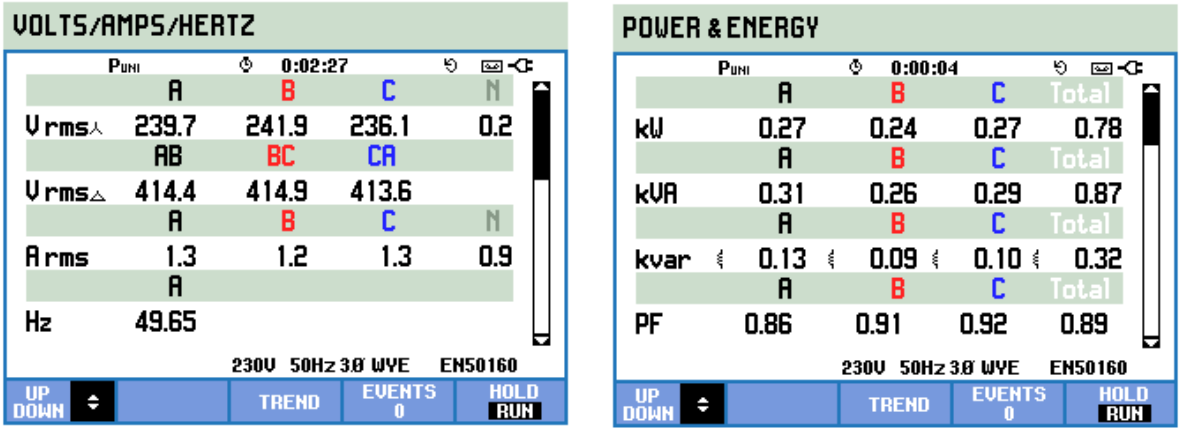


(c) WRIG and SCIG waveforms

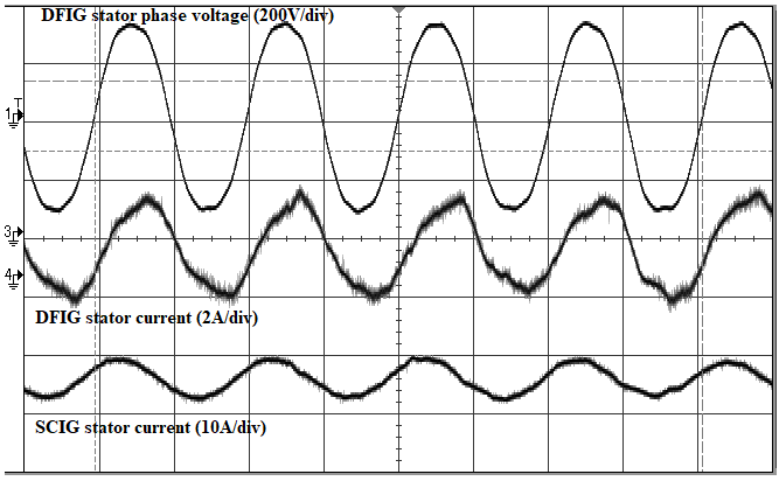
Fig. 3.2 Test results obtyained from the proposed WRIG-SCIG system for a load of 1.5 kW and at a speed of 1250 rpm (SCIG speed 1515 rpm)



(a) WRIG Stator phase voltage and current, respectively

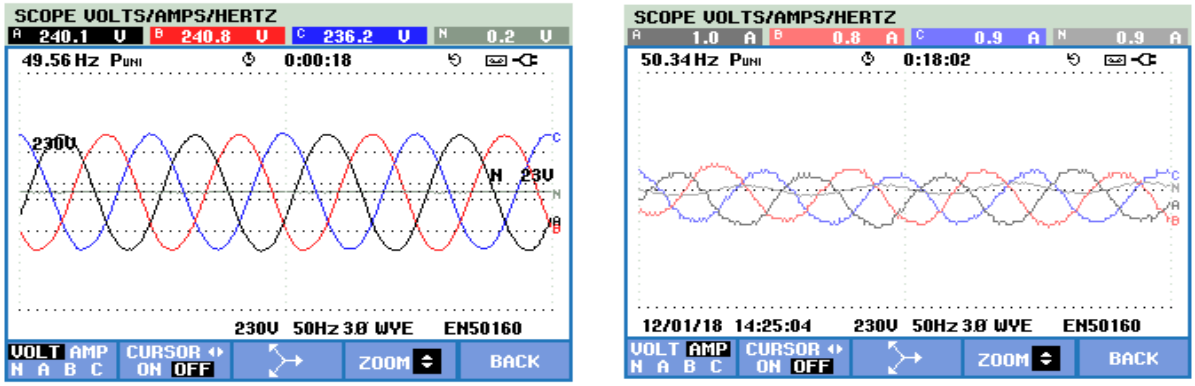


(b) Power quality analyzer displaying parameters at WRIG stator terminals

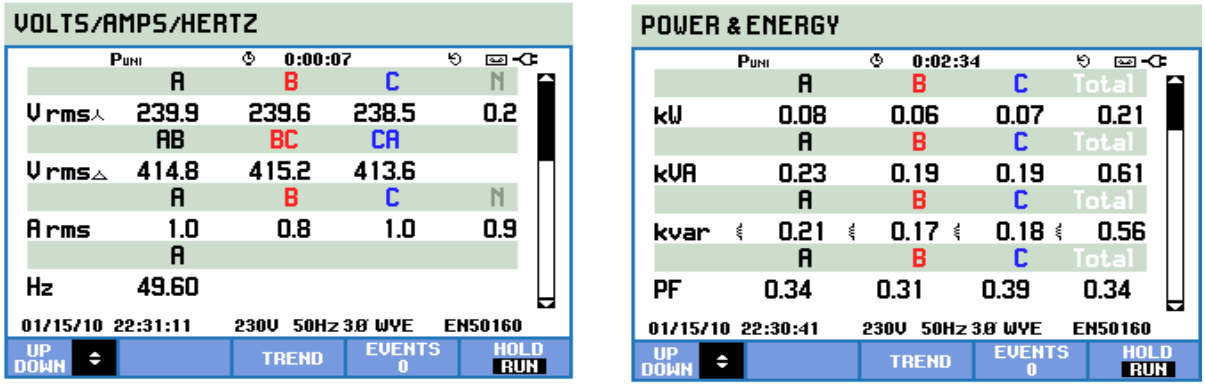


(c) WRIG and SCIG waveforms

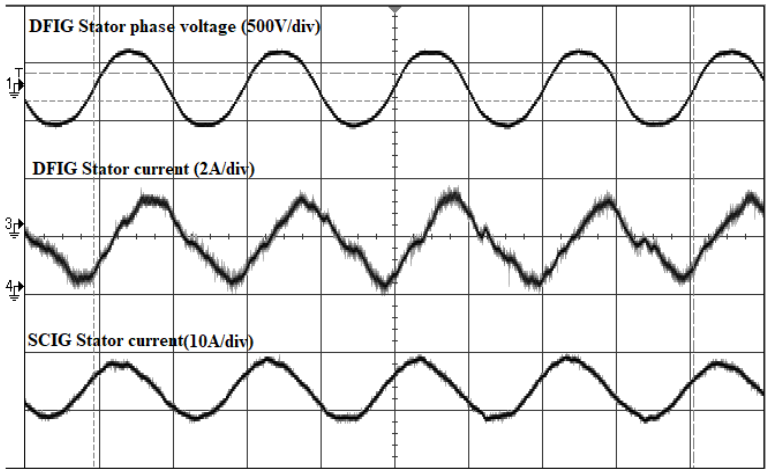
Fig. 3.3 Test results obtained from the proposed WRIG-SCIG system for a load of 1.5 kW and at a speed of 1250 rpm (SCIG speed 1530 rpm)



(a) WRIG Stator phase voltage and current, respectively

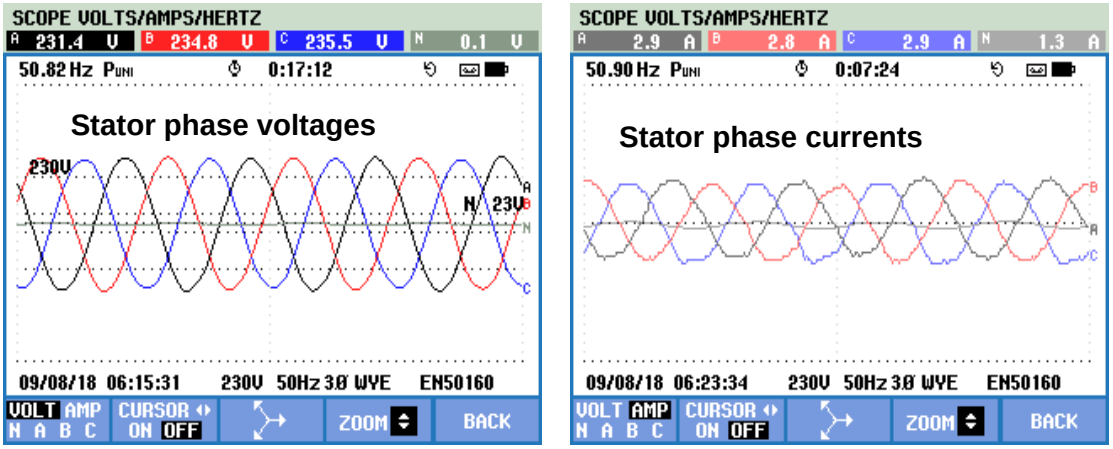


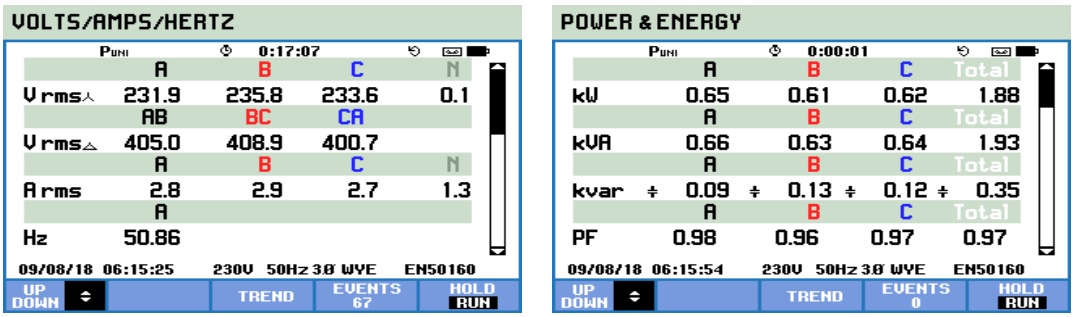
(b) Power quality analyzer displaying parameters at WRIG stator terminals



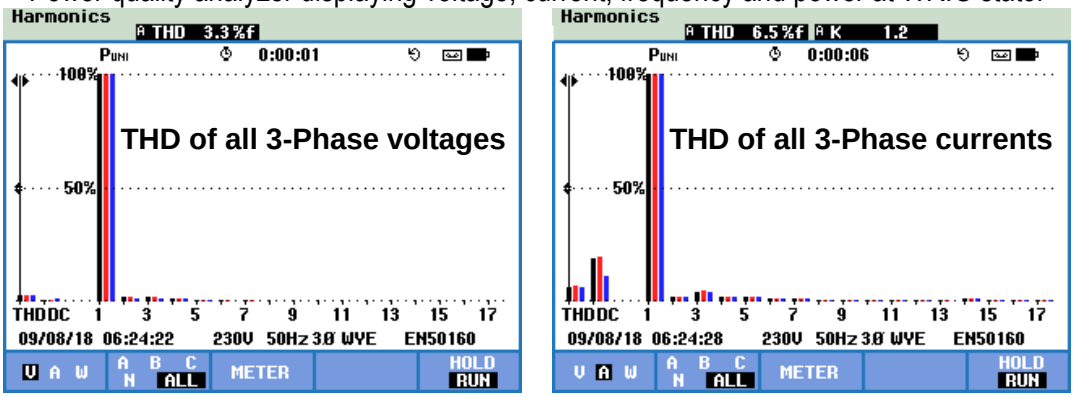
(c) WRIG and SCIG waveforms

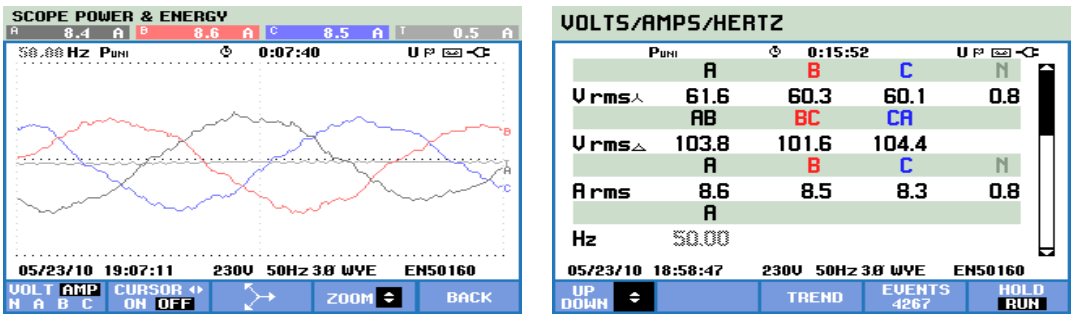
Fig. 3.4 Test results obtained from the proposed WRIG-SCIG system for a load of 1.5 kW and at a speed of 1250 rpm (SCIG speed 1570 rpm)





Power quality analyzer displaying voltage, current, frequency and power at WRIG stator

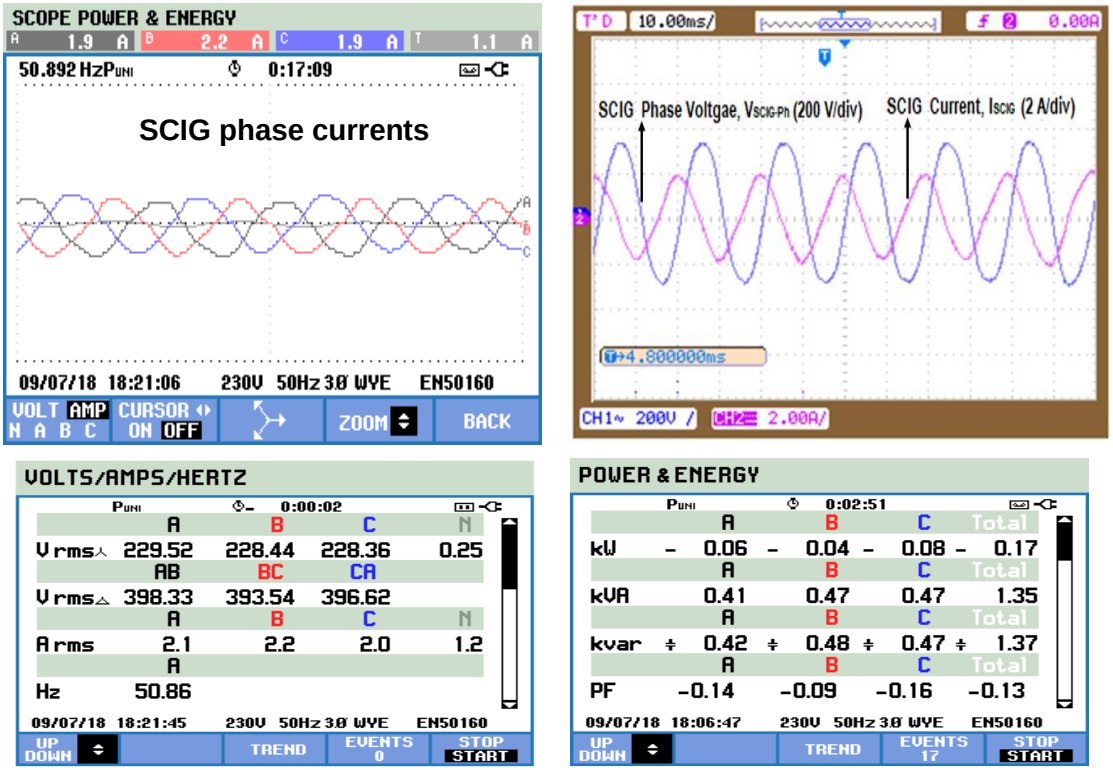




Rotor current waveforms

Voltage and current values at the rotor side

Fig. 3.5 Test results obtained from WRIG-SCIG parallel operation for a load of 1.5 kW and at a speed of 1050 rpm



Power quality analyzer displaying voltage, current,frequency and power at SCIG terminals

Fig. 3.6 Test results obtained from WRIG- SCIG parallel operation for a load of 1.5 kW and at a speed of 1050 rpm (SCIG speed = 1500)

Table 3.2

WRIG- SCIG parallel operation for floating condition

Load (kW)	Speed (rpm)	DFIG Stator			DFIG Rotor				Battery		PV Panel		Boost Converter			SCIG			
		$V_{s\,L\text{-}L}$ (V)	I_s (A)	$P_{s\,3\text{-}ph}$ (kW)	$V_{r\,L\text{-}L}$ (V)	I_r (A)	$P_{r\,3\text{-}ph}$ (kW)	P.F. (Lag)	V_B (V)	I_B (A)	V_{PV} (V)	I_{PV} (A)	δ (%)	V_O (V)	I_O (A)	Speed (rpm)	I_{SCIG} (A)	P (kW)	Q (kVAR)
1.5	1050	405	2.8	0.82	102	8.5	1.06	0.73	210	4.0	122	5.7	43	210	3.4	1500	2.1	0.17	1.37

3.4 SUMMARY

This chapter has described the parallel operation of WRIG and SCIG system. SCIG is envisaged to operate only when the power is deficit both from the wind and solar energies to meet out the required consumer demand. Experimental results given in this chapter demonstrates the successful working of the proposed system shown in Fig. 3.1. Depending upon the availability of wind and solar energy and battery capacity, the proposed system shown in Fig. 3.1 will operate in different modes for supplying the continuous power to the isolated loads. All such possible operating modes of the proposed system are taken in to consideration for effectively managing the proposed system. Details of such source and load controller are given in Chapter 5. Detailed steady-state analysis of the WRIG-SCIG-Battery system has also been carried out and the outcome of the analysis, operating modes, experimental validations, as part of this project are published in the following research paper:

1. K. Navin Sam, N. Kumaresan, and N. Ammasai Gounden, "Wind-driven Stand-alone DFIG with Battery and Pumped Hydro Storage System" Sadhana - Academy Proceedings in Engineering Science, Vol.42, Issue.2, February 2017, pp.173-185. (SCIE indexed: ISSN: 0256-2499).

The next chapter describes the operation and experimental investigations of the DSTATCOM and its integration with the proposed micro-grid system.

CHAPTER 4

DSTATCOM AND ITS INTEGRATED OPERATION WITH WRIG

4.1 Introduction

In the present project, it is proposed to employ DSTATCOM for catering the demand of reactive loads in the micro-grid and the dynamic reactive power requirement of squirrel cage induction generator (SCIG). This chapter presents the development details and working of DSTATCOM. The MATLAB simulation and FPGA based hardware realization are discussed. The synchronous reference frame theory has been utilized to compute the reference current for DSTATCOM. The modular development of synchronous reference frame theory and realization in FPGA are given in detail. The working of DSTATCOM to compensate reactive power is demonstrated initially at lower voltage level and then at nominal operating voltage. Further, the algorithm for real and reactive power transfer through DSTATCOM has been developed and its working has been verified along with WRIG system. The MATLAB simulation and prototype experimentation results showing reactive power transfer alone and then, simultaneous real and reactive power transfer are presented in this chapter.

4.2 Principle of working of DSTATCOM

The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) fed from a DC capacitor, for injecting current at the PCC through the interface inductor as shown in Fig. 4.1. It injects reactive and harmonic components of load current at the point of common coupling (PCC) such that the unbalanced, reactive, and harmonic loads are converted into equivalent balanced linear resistive load, and the source supplies only three-phase balanced fundamental

positive sequence component of load current. The VSI should be controlled such that desired current is injected into the system. The DC link voltage of the VSI is maintained almost constant by means of a large DC storage capacitor. Suitable adjustment of the phase and magnitude of DSTATCOM output voltage allows effective control on active and reactive power output from DSTATCOM.

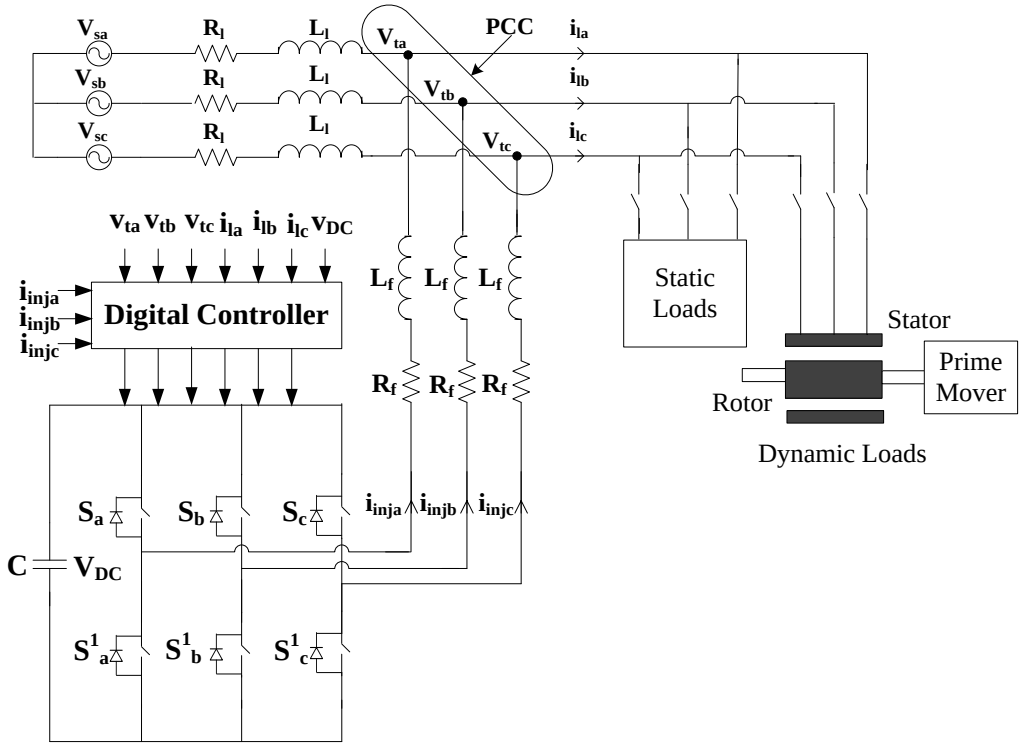


Fig. 4.1 Schematic of DSTATCOM connected system

The performance of DSTATCOM depends on the control algorithm used for extraction of reference current components. For this purpose, many control schemes such as instantaneous reactive power (IRP) theory, instantaneous symmetrical components theory, synchronous reference frame (SRF) theory, current compensation using DC bus regulation and neural network technique are reported in literature. Among the aforementioned control schemes, IRP and SRF theories are widely used for reference signal generation.

In the current technological scenario, microprocessors, digital signal processors (DSPs) and field-programmable gate arrays (FPGAs) are emerging as the preferred options for digital implementation of the control strategies for power converters. FPGA is becoming more expedient due to high degree of parallelism and input and output (I/O) capabilities. Their computational throughput is higher than that of typical DSPs at a much lower cost, as their hardware resources are configured to conform to the demands of each specific application.

In this project, an attempt is made to incorporate DSTATCOM to cater the reactive power requirements of loads. The capability of DSTATCOM to provide dynamic reactive power support is also explored. The present implementation utilizes synchronous reference frame (SRF) theory based transformation for reference current generation as it offers higher accuracy than stationary frame-based techniques. Further, a hysteresis controller is employed for the generation of pulses for the control of output voltage of VSI. The control scheme is implemented in FPGA controller without a dedicated personal computer (PC), which is mandatory for realising a similar control scheme in DSPACE controller. FPGA controller board used for this purpose incorporates a Xilinx Spartan 3AN -XC3S1400AN device.

4.3 Reference Current Generation by SRF Theory

SRF theory is based on the transformation of electrical quantities from stationary reference frame into synchronously rotating dq reference frame. The basic building blocks of SRF theory are shown in Fig. 4.2, where the three-phase PCC voltage (v_{ta}, v_{tb}, and v_{tc}) and load current (i_{la}, i_{lb} and i_{lc}) are fed as inputs to the controller.

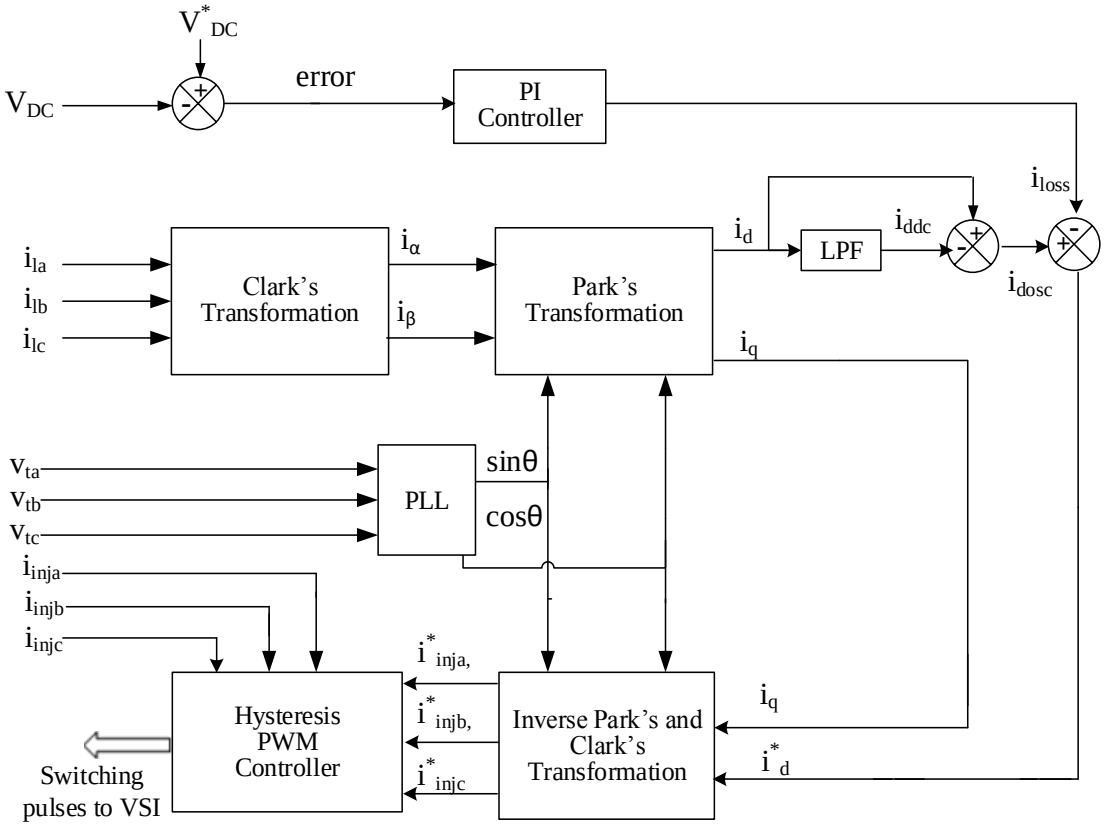


Fig. 4.2 Block diagram of reference current generation by SRF theory

The voltage signals are processed by a phase-locked loop (PLL) to generate unit voltage templates, (sine and cosine signals) so that the three-phase voltage at the converter output is synchronised with PCC voltage. Load current signals are transformed to dq frame, where these signals are filtered to extract the harmonic and reactive components of the load current. Then the extracted signals are translated back to abc frame (i^*_{inja}, i^*_{injb}, and i^*_{injc}), which are fed to a hysteresis-based PWM signal generator to generate switching pulses for VSI. Equations corresponding to the complete transformation are given below:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \quad (4.1)$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (4.2)$$

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} i^*_d \\ i_q \end{bmatrix} \quad (4.3)$$

$$\begin{bmatrix} i^*_{inja} \\ i^*_{injb} \\ i^*_{injc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 1 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_0 \\ i^*_\alpha \\ i^*_\beta \end{bmatrix} \quad (4.4)$$

The real and reactive components of the load current (i_d and i_q) attained from eq. (4.2) will have a DC component and an oscillating component. DSTATCOM is operated in such a way that it has to supply the oscillating part of real component and complete reactive component of the load current. A low pass filter (LPF) capable of extracting only i_{ddc} is used and then it is subtracted from i_d, so that DSTATCOM supplies only oscillating component (i_{dosc}) of the real power. No filtering is done on i_q as the complete reactive component required by the load has to be supplied by the DSTATCOM.

In the operation of DSTATCOM connected system, either the AC sources connected in the system or the DC source connected across the DC capacitor is expected to supply the real power required by the load and losses (switching losses of devices, losses in reactor, and dielectric losses of DC bus capacitor) in the DSTATCOM. So, the injected current reference that decides the

switching of DSTATCOM has two components: one is the oscillating component of the load current and another corresponding to the losses in DSTATCOM. The loss component is estimated by comparing the reference DC bus voltage (V^*_{DC}) with the sensed DC capacitor voltage (V_{DC}) and processing it through PI controller. The output of PI controller accounts for the losses in DSTATCOM, which is considered as the loss component of the current, and is combined with the d-axis component of the load current. This loss component helps in maintaining the DC link voltage (V_{DC}) at a predefined reference value (V^*_{DC}) by drawing balanced current from the source.

The reference current i_{ref} (i^*_{inja}, i^*_{injb}, and i^*_{injc}) obtained from eq. (4.4) and the sensed DSTATCOM injected current i_{act} (i_{inja}, i_{injb} and i_{injc}) are fed to a hysteresis-based PWM current controller to control the DSTATCOM such that the injected current always follows the reference current.

4.4 FPGA Implementation of SRF Theory

FPGA is a hardware array of configurable logic resources with interconnections that are fully programmable by the end user to build specific hardware architectures. FPGA devices can target nearly any application due to their general architecture, which permits the designer to tailor specific tasks by programming the functionality and connectivity of the device using electronic design automation (EDA) tools. In industrial applications, DSP and FPGA based controllers are powerful competitors in many aspects. However, FPGA is better suited to operate with high-frequency applications where it is desired to drive several modules as a multi-module system or to add functions to improve the final performance taking advantage of its speed and parallelism.

Hardware Description Languages (HDL) such as Very high speed integrated circuits Hardware Description Language (VHDL) and Verilog HDL support the growth of intricate designs

on FPGAs utilising a hierarchical and modular approach defined at different abstraction levels employing a top-down design style methodology. Thus, complicated applications require defining the problem in a modular structure suitable to be translated into HDL code. Although FPGA devices are an attractive solution to implement digital controllers, they do demand an additional exertion in the programming phase. Nevertheless, with improved tool support, structured design techniques and available intellectual property (IP) core, the design time can be shortened.

In the event of power electronic control application, the execution needs the definition of a modular structure that ought to be easily translated into HDL code. As a first measure, the main modules required in the control strategy should be recognised, making particular emphasis to the module inputs, outputs and main variables/signals involved in its performance. Likewise, for complex modules, decomposition into sub-modules is required. Ideally, the modules designed should be easily exportable to different applications. In time, over different projects, these modules can be used to establish a library that can greatly reduce design time in future tasks. The second measure is to create a register transfer level (RTL) description of the internal information flow. As a third step, all the defined structures are translated into HDL code to be synthesized and loaded into an FPGA using Design Suite. It is significant to note that each module can be designed independently, reused and likewise has a physical significance, as it performs specific tasks.

In this work, a modular implementation of SRF control strategy of a DSTATCOM using FPGA is carried out, and the control performance is also presented. The control strategy has been completely implemented on a Spartan-3AN FPGA. The general schematic shown in Fig. 4.3(a) designates that the modular design of the control strategy requires four modules to implement all

the controller functions (A/D conversion and positive sequence extractor module, synchronization, reference signal generation and PWM module). Schematic of the modular design in Altium design suite is presented in Fig. 4.3(b).

***1) A/D conversion module*:** This module executes the A/D conversion by receiving serial bits from the external ADC channel. It deals with the synchronization of the external analog to digital converter (ADC) with the FPGA and sends the acquired 8-bit data to the subsequent module. The inputs signals to the external ADC channel are from current and voltage transducers, in the range of (0-3.3) V. The A/D conversion module performs ten conversions which include the three-phase PCC voltage, three-phase load current, three-phase injected current and the DC voltage. The module operates with a 3.2 MHz clock due to the 50 kSps imposed on ADC. The ADC084S021 is utilised in this work.

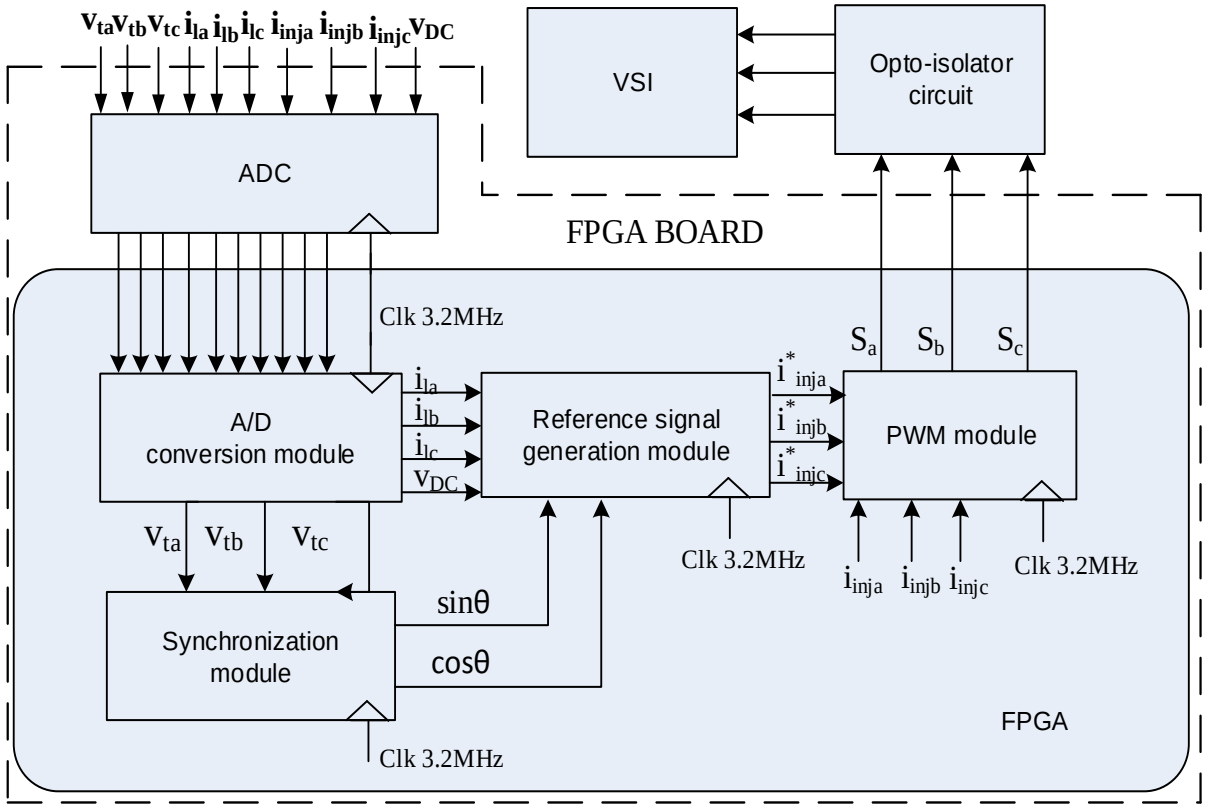
***2) Synchronization module*:** Three-phase positive sequence component of PCC voltage is fed to this module, which obtains the synchronizing angle from the input voltages. The three-phase voltages (v^{+}_{ta}, v^{+}_{tb}, and v^{+}_{tc}) are converted into two-phase voltages (v_{α} and v_{β}) by using the eq. (4.5) and the synchronizing angles sinθ and cosθ are obtained from eq. 4.6 and 4.7.

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \\ v_{0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \quad (4.5)$$

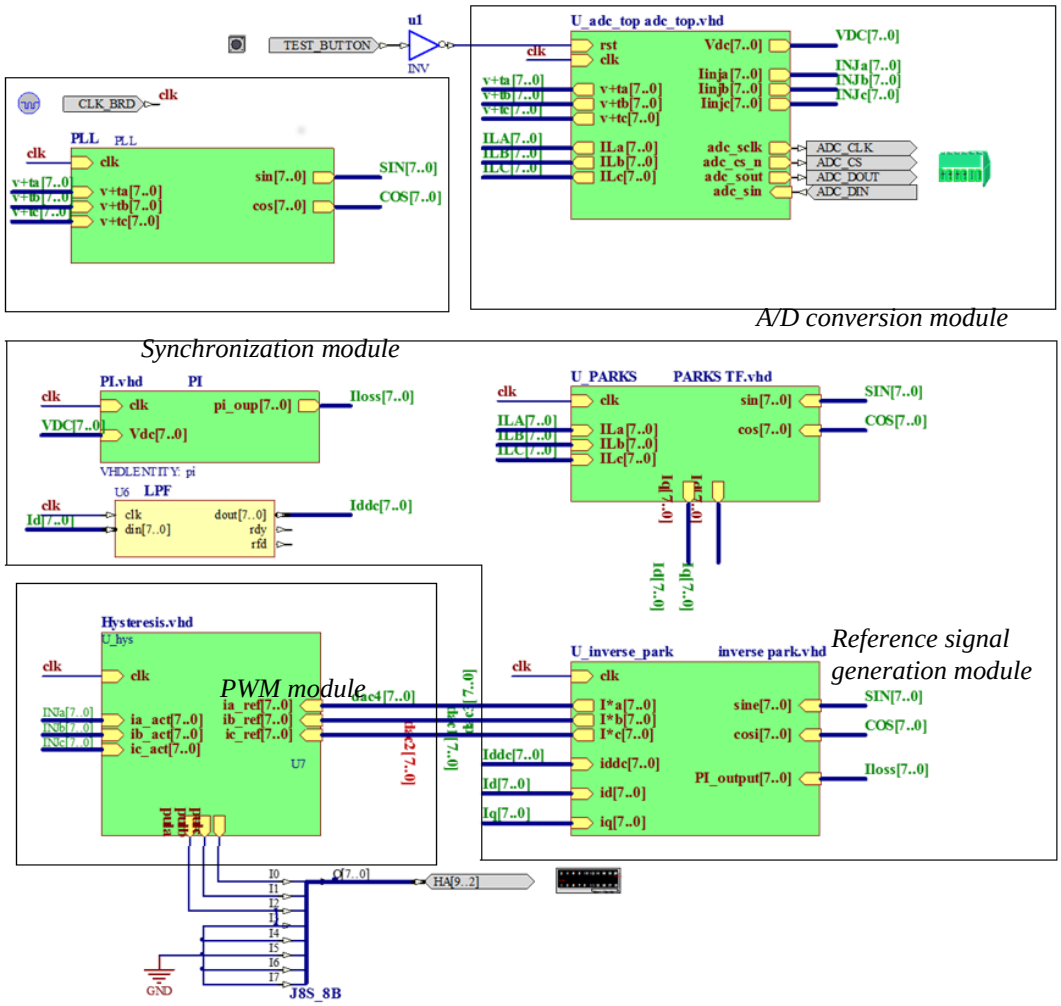
$$\sin\theta = \frac{v_\alpha}{\sqrt{v_\alpha^2 + v_\beta^2}} \qquad (4.6)$$

$$\cos\theta = \frac{v_\beta}{\sqrt{v_\alpha^2 + v_\beta^2}} \qquad (4.7)$$

***3) Reference signal generation module*:** This module takes load current (i_{la}, i_{lb} and i_{lc}) and synchronisation angles as inputs and computes the reference signal for DSTATCOM. As seen from Fig. 4.3(b) this module contains *abc-dq* block, LPF, PI controller and *dq-abc* block.



(a) Modular design of control strategy



(b) Schematic of the modular design in Altium design Suite.

Results Summary

Device Resources - Usage Summary	
4-Input LUTs - Logic	1,803 / 22,528 8%
Average Fan/Non-Clock Nets	2.06
BUFGMUXs	2 / 24 8%
I/O Pins	40 / 502 8%
MULT18X18SIOs	18 / 32 56%
over-mapped for a non-slice resource or if Placemen	
Slice Flip Flops	1,650 / 22,528 7%
Slices with only related logic	1,753 / 1,753 100%
Slices with unrelated logic	0 / 1,753 0%
Slices	1,753 / 11,264 15%
Total 4-Input LUTs - Logic	1,822 / 22,528 8%
Design Statistics - Timing Summary	
No timing constraints.	

(c) Resource utilisation of the proposed FPGA implementation of SRF theory based DSTATCOM control scheme.

Fig. 4.3 FPGA implementation of the control scheme.

The *abc-dq* block gives i_d and i_q as output, i_d is further processed through a digital (LPF) to obtain dc component (i_{ddc}). The coefficients (0.104, 0.626, 0.626 and 0.104) for LPF are obtained using MATLAB toolbox. Further, the actual DC voltage is compared with its reference and resulting error is processed through a discrete PI controller which uses several registers to store the previous values. The PI output is appended to the oscillating component of i_d, which in conjunction with i_q are fed to the *dq-abc* block to obtain the reference signals in *abc* frame. The module input rate is 50 kHz and the output generation is also at 50 kHz.

***4) PWM module*:** Three-phase reference current and injected current are fed as inputs to this block as shown in Fig. 4.3(b). Switching signals generated by PWM module controls the injected current close to the reference current. The following logic has been used for generating switching signals, where *hb* is the hysteresis band around the reference current i_{ref}.

1) If (i_{act}) $\geq$ (i_{ref} + *hb/2*), the upper switch of the leg is OFF, and the lower switch is ON.

2) If (i_{act}) $\leq$ (i_{ref} – *hb/2*), the upper switch of the leg is ON, and the lower switch is OFF.

3) If (i_{ref} – *hb/2*) $\leq$ (i_{act}) $\leq$ (i_{ref} + *hb/2*), no change in the switching pulses.

The resource usage summary generated by the Altium design suite is shown in Fig. 4.3(c).

4.5 Testing of DSTATCOM by Laboratory Experiment

A prototype built in the laboratory to examine the performance of DSTATCOM for load compensation is shown in Fig. 4.4. The three-phase load current (i_{la}, i_{lb} and i_{lc}) and DSTATCOM injected current (i_{inja} i_{injb} and i_{injc}) are sensed using Hall effect current sensor (LA-55P). Four voltage sensors (LV-20P) are used to sense three-phase PCC voltage and DC link voltage. These quantities are fed to the FPGA through ADC available on-board. The control theory is totally

programmed in VHDL, synthesized using Altium Design suite and finally loaded into the SPARTAN 3AN FPGA. Waveforms are recorded using digital storage oscilloscope (DSO-X3034A) and power quality clamp meter (Fluke 345).

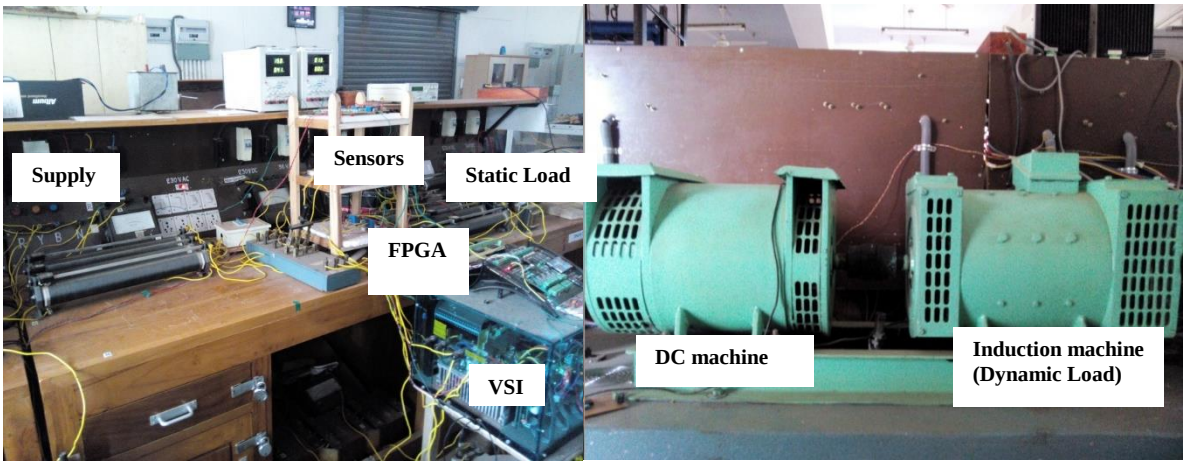


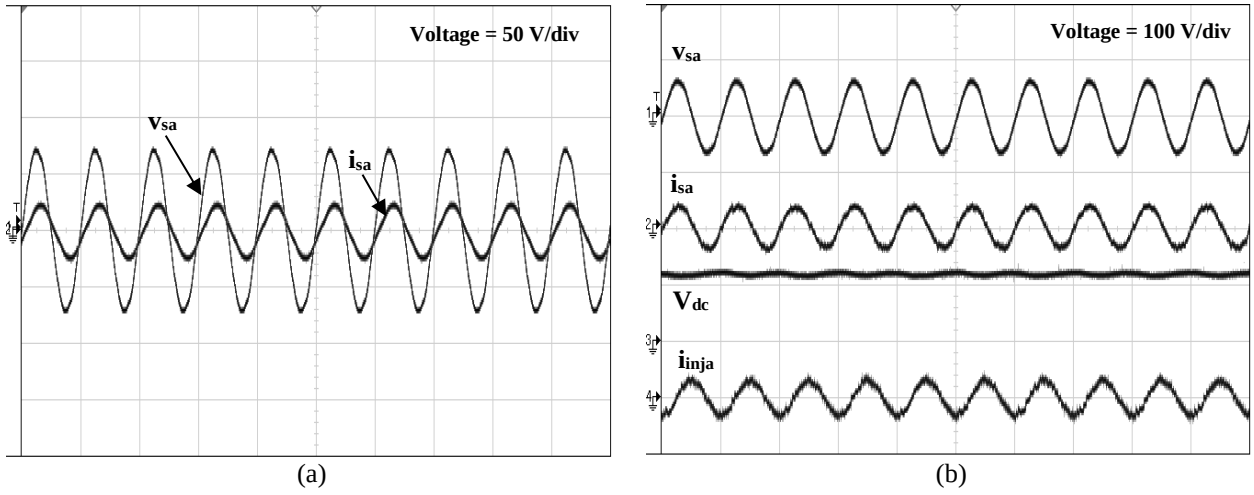
Fig. 4.4 Photograph of the experimental setup used in the laboratory.

A. Performance of DSTATCOM under Static Loading

In order to check the effectiveness of the algorithm implemented in FPGA for the control of DSTATCOM, various test cases are executed. The test cases comprise of different loading conditions such as only linear load, only nonlinear load, linear and nonlinear loads connected in parallel and unbalanced loads. The linear load considered in this case study is a star connected balanced three-phase R-L load and the nonlinear load is a diode bridge rectifier followed by R-L load.

1) Reactive power Compensation: The source voltage and uncompensated source current are shown in Fig. 4.5(a). Based on the reference current obtained using eq. (4.4), the VSI is operated in hysteresis current control mode to synthesis actual compensator current. Accordingly,

the switching commands are issued to control IGBT switches through proper interfacing circuits. The maximum switching frequency attained for hysteresis controller is 5 kHz, which is well below the maximum switching frequency of the IGBT switches i.e. 20 kHz. The steady state waveforms of source voltage, source current, DC link voltage and injected current when DSTATCOM is connected to the system are presented in Fig. 4.5(b). It is evident that the source current is in phase with the source voltage and the DC link voltage is maintained at 115 V with a PI controller. Thus the reactive power compensation is achieved using DSTATCOM with a self-supporting DC bus.



(a) (b)

Fig. 4.5 Waveforms under reactive power compensation of static loads (phase-a).
(current axis = 4A/ div and time = 20 ms/div)
(a) Source voltage and current without DSTATCOM.
(b) Source voltage, source current, DC voltage and injected current with DSTATCOM.

2) Harmonic Compensation: The performance of DSTATCOM with nonlinear load is presented in Fig. 4.6. The source voltage and uncompensated source current are shown in Fig. 4.6(a). It can be inferred that the source current consists of harmonics and has a total harmonic distortion (THD) of 17.4 % which is shown in Fig. 4.6(c). The steady state waveforms of source voltage and current, DC voltage and injected current with DSTATCOM are shown in Fig. 4.6(b). Further, it can be inferred from Fig. 4.6(c), %THD of the compensated source current is 3.6 %. Thus, the harmonic and reactive power required by the load is provided by DSTATCOM.

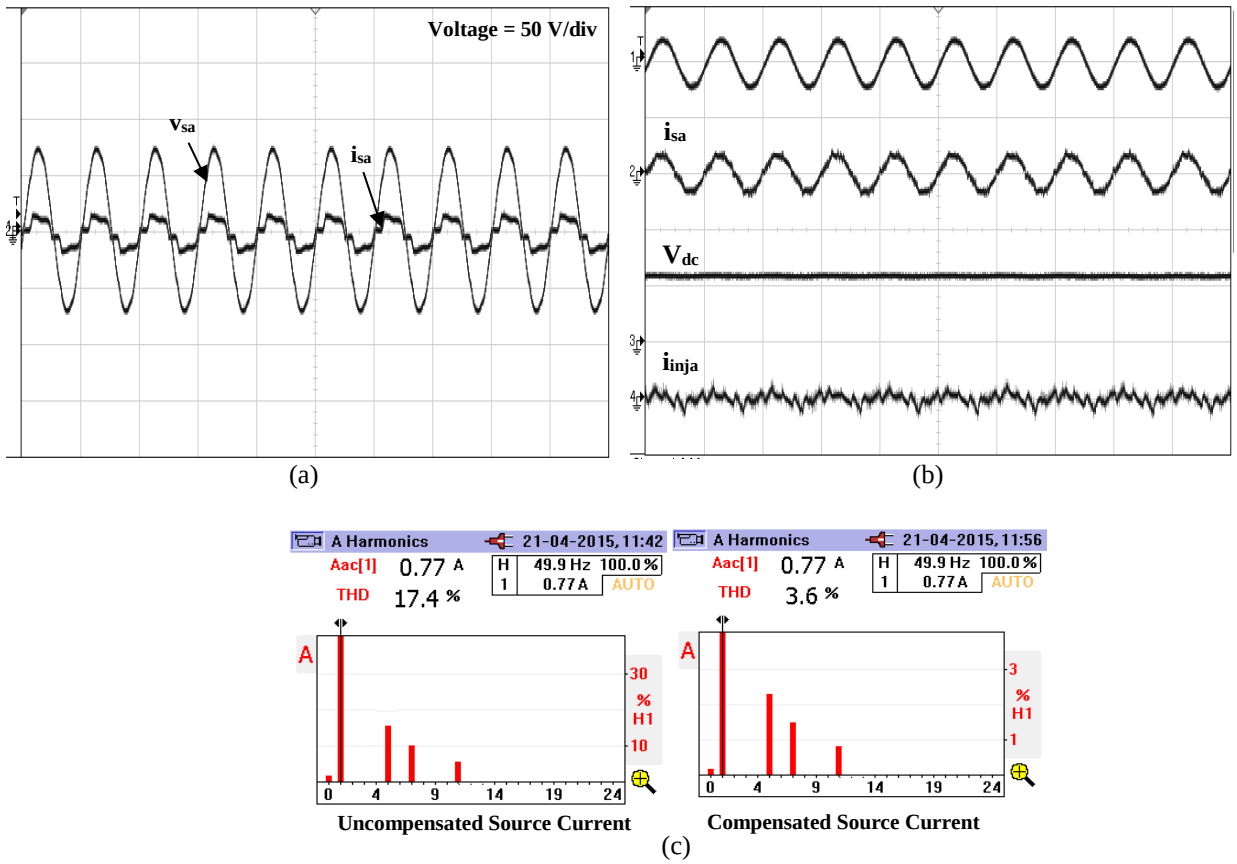


Fig. 4.6 ***Waveforms under harmonic compensation of static loads (phase-a).***
(current axis = 3A/ div and time = 20 ms/div).

(a) Source voltage and current without DSTATCOM.
(b) Source voltage, source current, DC voltage and injected current with DSTATCOM.
(c) % THD of uncompensated and compensated source current.

3) Reactive Power and Harmonic compensation: In this case, both linear and nonlinear loads are connected in parallel and the performance of DSTATCOM is observed. The recorded waveforms are presented in Fig. 4.7. Fig. 4.7(a) demonstrates the recorded waveforms of source voltage and current before compensation. Fig. 4.7(b) presents the waveforms of source voltage, source current, DC voltage (115 V) and injected current. The waveforms of reference current observed through DAC and injected current are shown in Fig. 4.7(c). It is apparent that DSTATCOM with proposed scheme tracks reference current incisively and provides harmonic and reactive power compensation of the load. Further it can be ascertained from Fig. 4.7(d) that %THD of the source current is reduced to 2.6 % from 7.2 %.

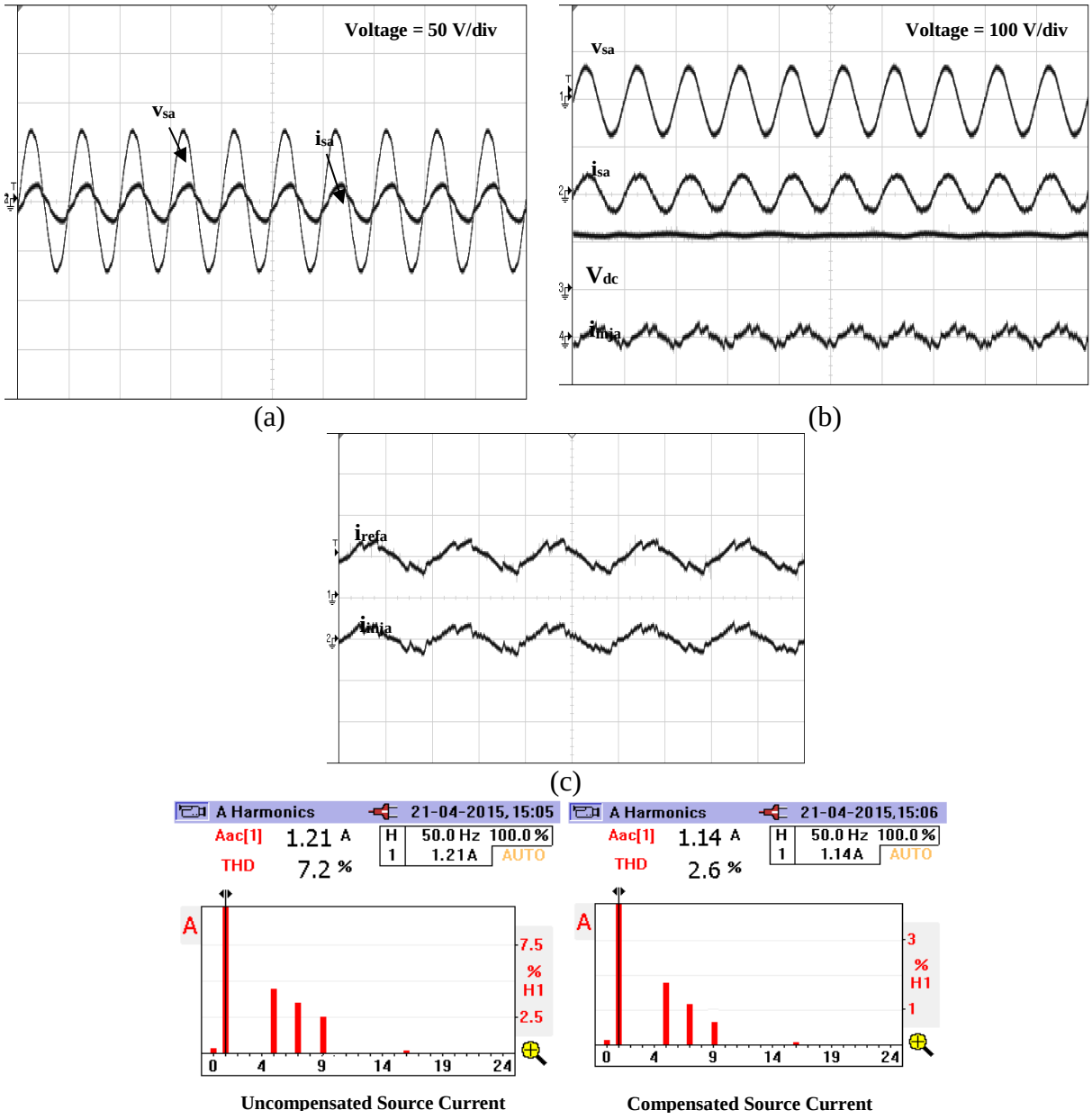
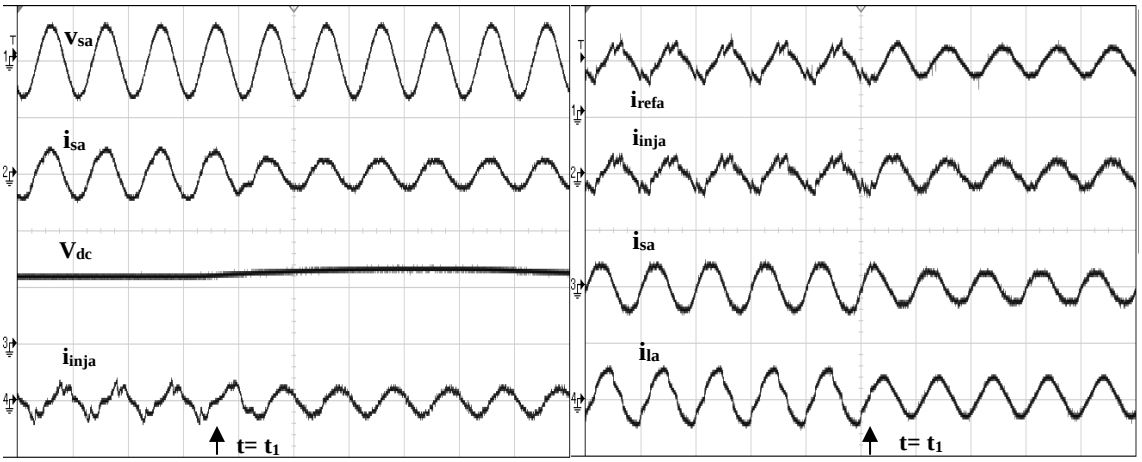


Fig. 4.7 ***Waveforms under reactive power and harmonic compensation of static loads(phase-a)*** **(current axis = 4A/ div and time = 20 ms/div)**

(a) Source voltage and current without DSTATCOM.
(b) Source voltage, source current, DC voltage and injected current with DSTATCOM.
(c) Reference current and injected current. (d) % THD of uncompensated and compensated source current.



(a) (b)

Fig. 4.8 Waveforms under dynamic compensation (phase-a).
(voltage axis = 100V/div, current axis = 4A/ div and time = 20 ms/div)

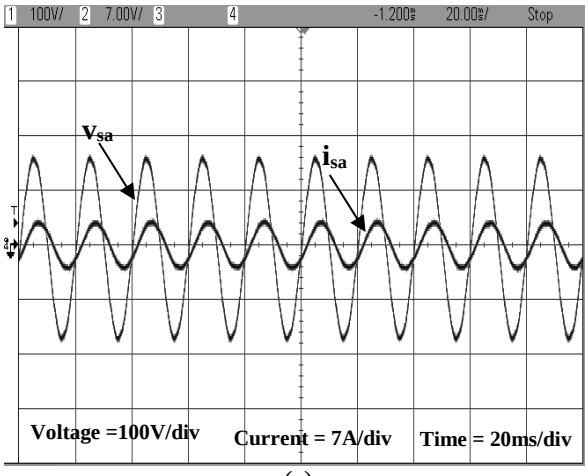
(a) Source voltage, source current, DC voltage and injected current.
(b) Reference current, injected current, source current and load current.

Further, the performance of proposed scheme during dynamic condition is shown in Fig. 4.8, wherein a disturbance is introduced at time t = t_1 s by disconnecting the nonlinear load. Fig. 4.8(a) displays the waveforms of phase-a source voltage (v_{sa}), source current (i_{sa}), DC voltage (V_{dc}) and phase-a injected current (i_{inja}). The waveforms of phase-a reference current (i_{refa}), injected current (i_{inja}), source current (i_{sa}) and load current (i_{la}) The injected current tracks reference current effectively even under transient conditions.

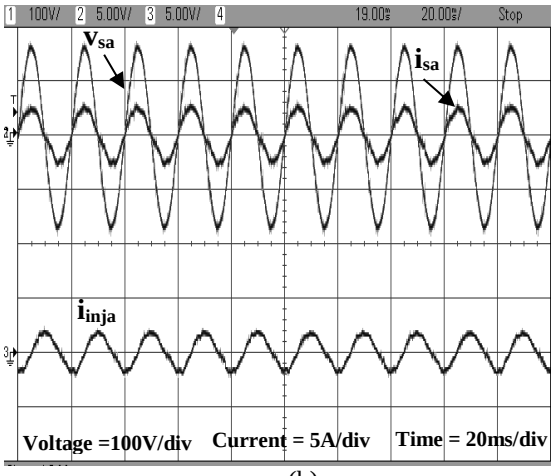
B. Performance of DSTATCOM under Dynamic Loading

***1) Reactive power compensation for an Induction Motor*:** In order to validate the feasibility of the implemented control scheme of DSTATCOM for dynamic reactive power compensation, the algorithm is tested with induction motor (IM), under different loading conditions. The IM used in the laboratory prototype during experimentation is a 4 pole 50 Hz machine and is fed at 200 V (L-L). Fig. 4.9(a) shows the waveforms of the source voltage and current of phase-a before compensation. It is observed that the current is lagging the voltage, which indicates that the

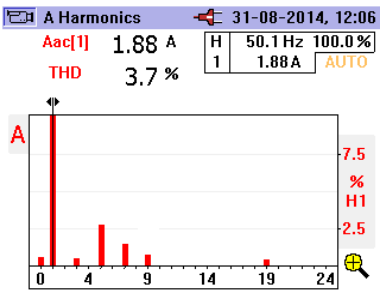
machine is drawing reactive power from the source. The waveforms recorded after the connection of DSTATCOM to the system are shown in Fig. 4.9(b). It can be noticed that the reactive power required by the motor is supplied by DSTATCOM so that almost unity power factor (UPF) operation is attained at the source. Further, Fig. 4.9(c) evinces % THD of the compensated source current which is 3.5%. The real and reactive power absorbed from the supply without and with DSTATCOM at a load current of 2.08 A is exhibited in Fig. 4.9(d). It can be depicted that the power factor at the source side is improved from 0.783 to 0.990. Further, there is an increase of 25W in real power, when DSTATCOM is switched ON, indicating that the losses in the inverter are supplied by the source. The DC capacitor is maintained at 420 V by using PI controller. Fig. 4.9(e) demonstrates the graph depicting the dynamic reactive power compensation capability of DSTATCOM under different loading conditions. It can be inferred that the increment in real power corresponds to the losses in the inverter, which is nearly constant in all the loading conditions.



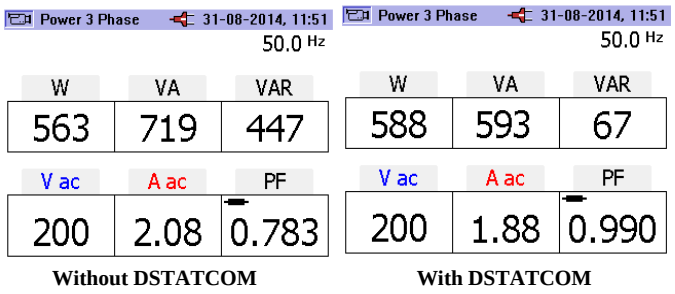
(a)



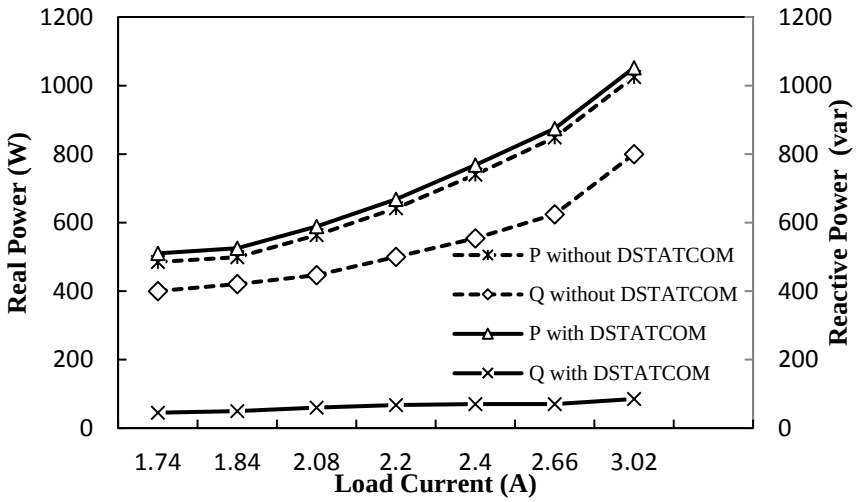
(b)



(c)



(d)



(e)

Fig.4.9 Reactive power compensation of induction motor.

(a) Source voltage and current without DSTATCOM (phase -a).
(b) Steady state waveforms of source voltage, source current and injected current (phase-a).
(c) % THD of compensated source current.
(d) Real and reactive power absorbed from the supply without and with DSTATCOM.
(e) Real and reactive power absorbed from the supply with and without DSTATCOM under dynamic loading.

2) Reactive power compensation for SCIG

The capability of DSTATCOM to provide dynamic reactive power compensation for SCIG is also tested. Super synchronous speed operation is accomplished through field control of dc shunt motor acting as a prime mover. Fig. 4.10(a) shows the phasor relationship between supply voltage (v_{sa}) and current (i_{sa}) in phase-a without DSTATCOM, which uncovers that the reactive power is drawn from the supply. The direction of the current is reversed which indicates that induction

machine is acting as induction generator (IG). The results are provided for a rotor speed of 1545 rpm. Steady state waveforms of v_{sa}, i_{sa} and i_{inja} are illustrated in Fig. 4.10(b), in which there is nearly 180^0 phasor relationship between voltage and current indicating that the reactive power is supplied by the DSTATCOM. Fig. 4.10(c) displays the %THD of source current with DSTATCOM which is only 2.9 % and within IEEE 519 limit. The DC voltage is regulated around 420 V using PI controller. The real power delivered to the supply and reactive power drawn from the supply without and with DSTATCOM is shown in Fig. 4.10(d). It can be inferred that the power factor is improved from 0.701 to 0.991 lagging. Negative power factor indicates the 180^0 phase difference between voltage and current. The reduction in real power fed to the supply corresponds to the losses in inverter which are supplied by IG. Fig. 4.10(e) shows the graph of real and reactive power absorbed from the supply without and with DSTATCOM at various rotor speeds. It can be noticed that the reactive power absorbed from the supply is reduced, which affirms the efficacy of the controller.

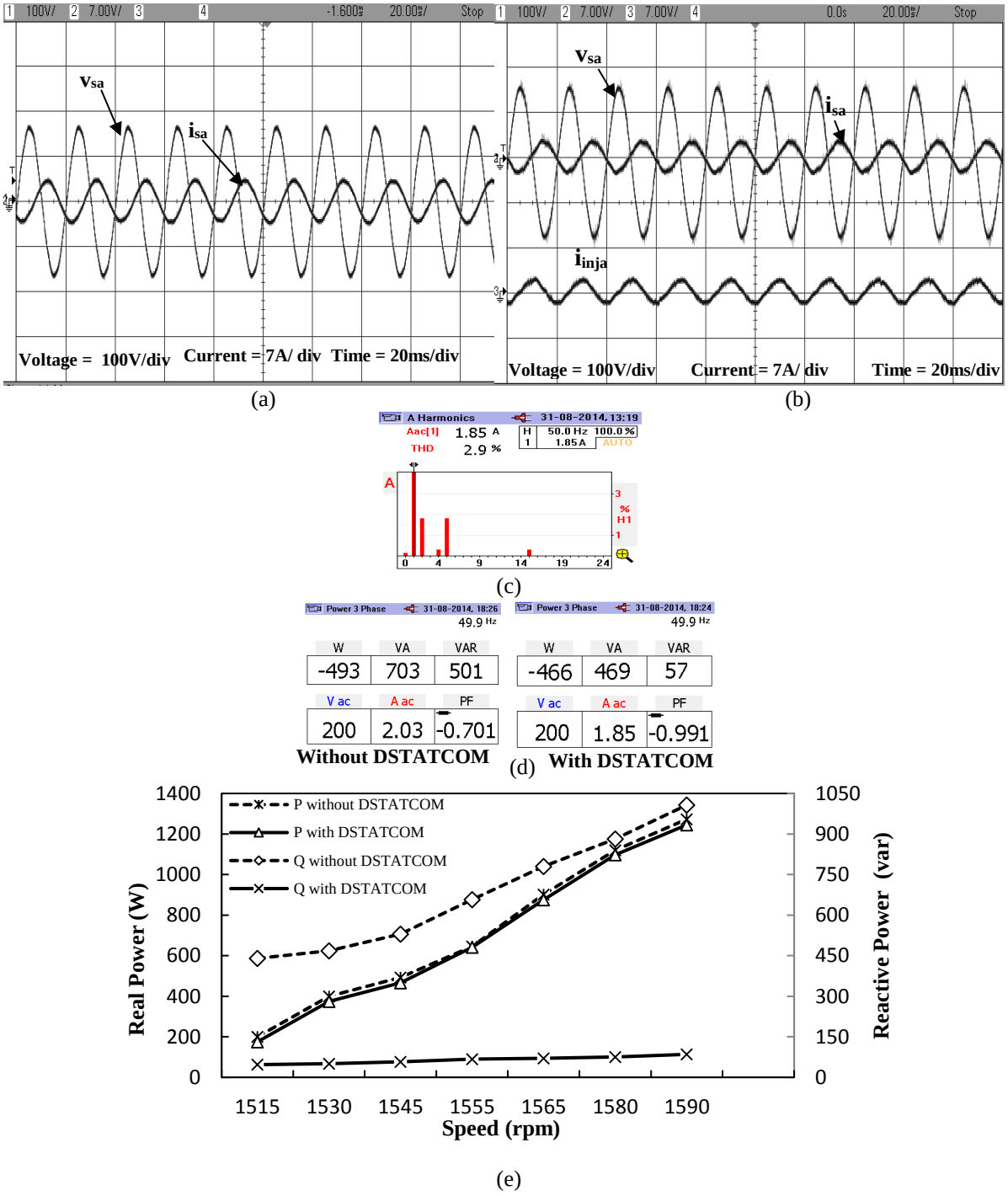


Fig. 4. 10 Reactive power compensation of induction generator.

(a) Source voltage and current without DSTATCOM (phase -a). **(b)** Steady state waveforms of source voltage, source current and injected current (phase-a). **(c)** % THD of compensated source current. **(d)** Real and reactive power absorbed from the supply without and with DSTATCOM**.** **(e)** Real power fed to and reactive power absorbed from the supply with and without DSTATCOM under assorted rotor speed conditions.

4.6 Testing of DSTATCOM at Nominal Operating Voltage

The DSTATCOM is tested with the nominal operating voltage of three-phase, 415 V, 50 Hz. Initially its functionality is evaluated with an isolated load of R=50 Ω and L = 50mH (per phase).The DC link voltage is maintained at 600 V. The power flow and voltage magnitudes recorded at the load terminal, DSTATCOM terminal and supply terminal are tabulated in Table -4.1 and displayed in Fig. 4.11 and 4.12, when DSATCOM is used for compensating load reactive power alone. Similarly, the power flow and voltage magnitudes recorded at the load terminal, DSTATCOM terminal and supply terminal are tabulated in Table -4.2 and displayed in Fig. 4.13 and 4.14, when DSATCOM is used for compensating load reactive power and fraction of the load real power.

Case : 1 Transfer of only reactive power by DSTATCOM

Table 4.1 Power Flow and Voltage details (transfer of only reactive power by DSTATCOM)

Measuring Point	Before Compensation				After Compensation			
	V_{ph} (V)	I_{ph} (A)	$P_{3\emptyset}$ (W)	$Q_{3\emptyset}$ (Var)	V_{ph} (V)	I_{ph} (A)	$P_{3\emptyset}$ (W)	$Q_{3\emptyset}$ (Var)
Supply	240	4.58	3156	991	240	4.41	3186	20.86
Load	240	4.58	3156	991	240	4.58	3154	994
STATCOM	240	0	0	0	240	1.38	36	995

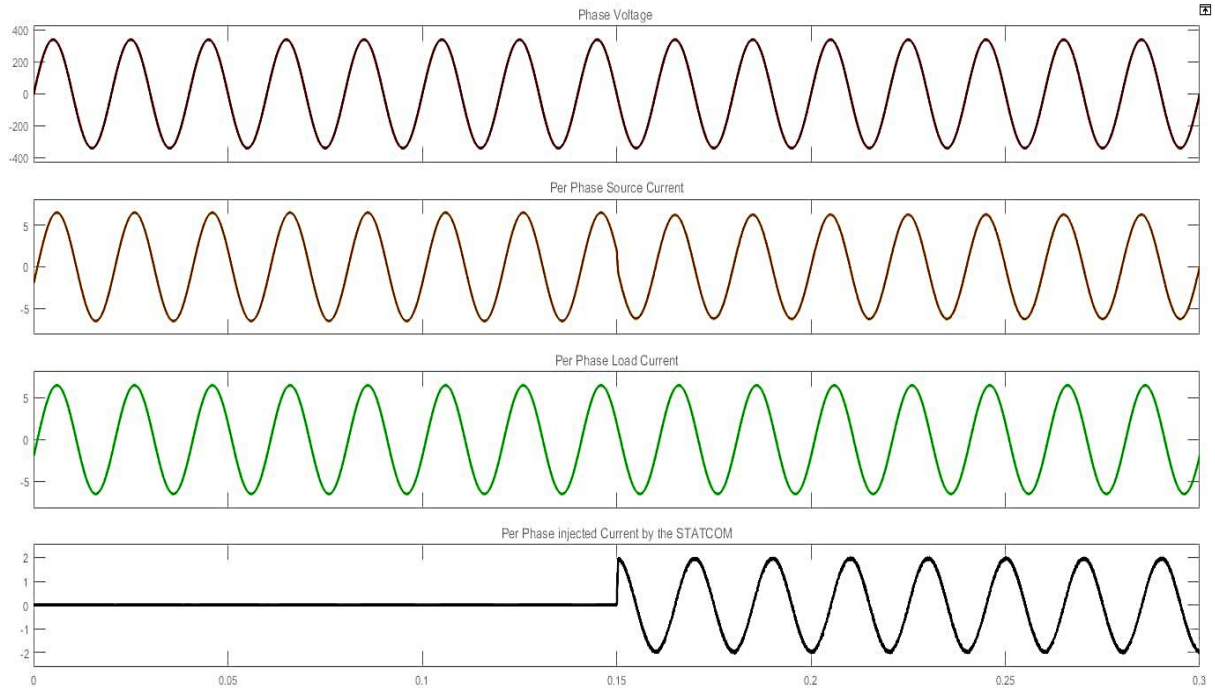


Fig. 4.11 Phase Voltage, Per Phase supply current, Per Phase Load Current, Per Phase DSTATCOM Current

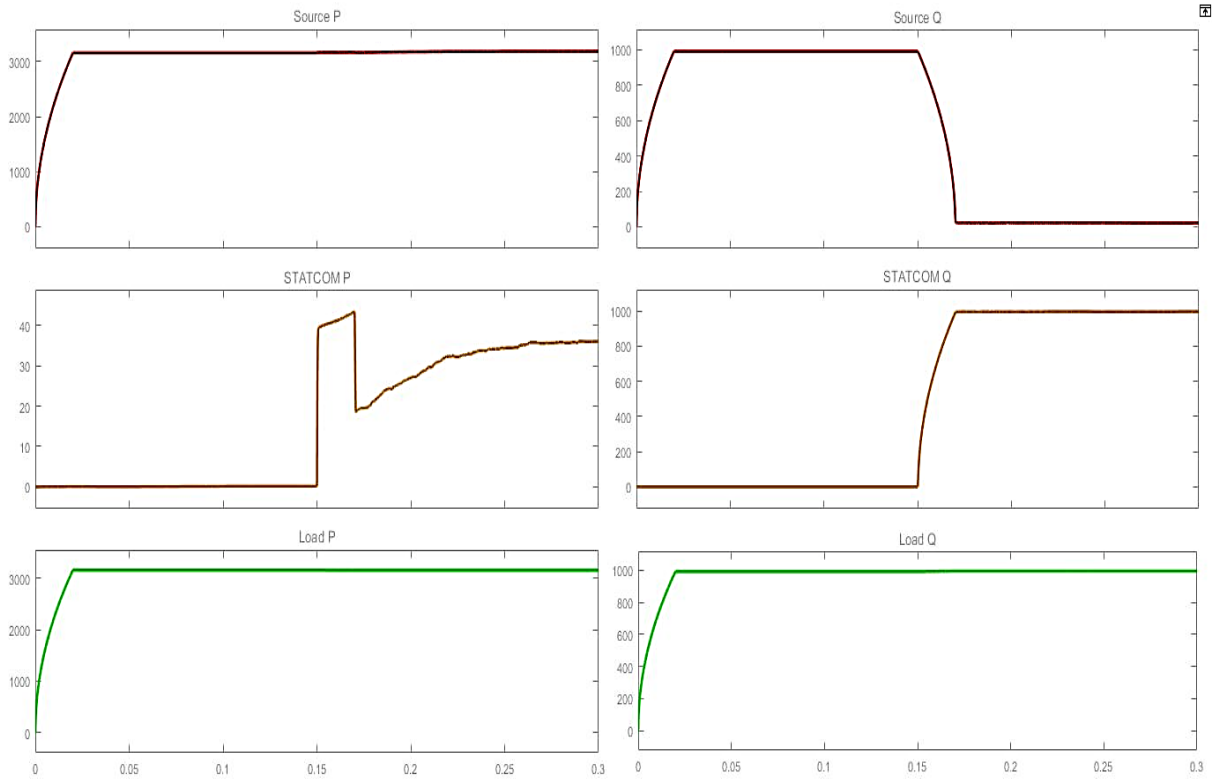


Fig. 4.12 Real and reactive power measured at supply, DSATCOM and Load terminals

Case : 2 Transfer of reactive power and 50% of real power

Table 4.2 Power Flow and Voltage details

Measuring Point	Before Compensation				After Compensation			
	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)
Supply	240	4.58	3156	991	240	2.23	1608	21.92
Load	240	4.58	3156	991	240	4.58	3154	994
STATCOM	240	0	0	0	240	2.55	1546	1002

(transfer of reactive power and 50% of real power by DSTATCOM)

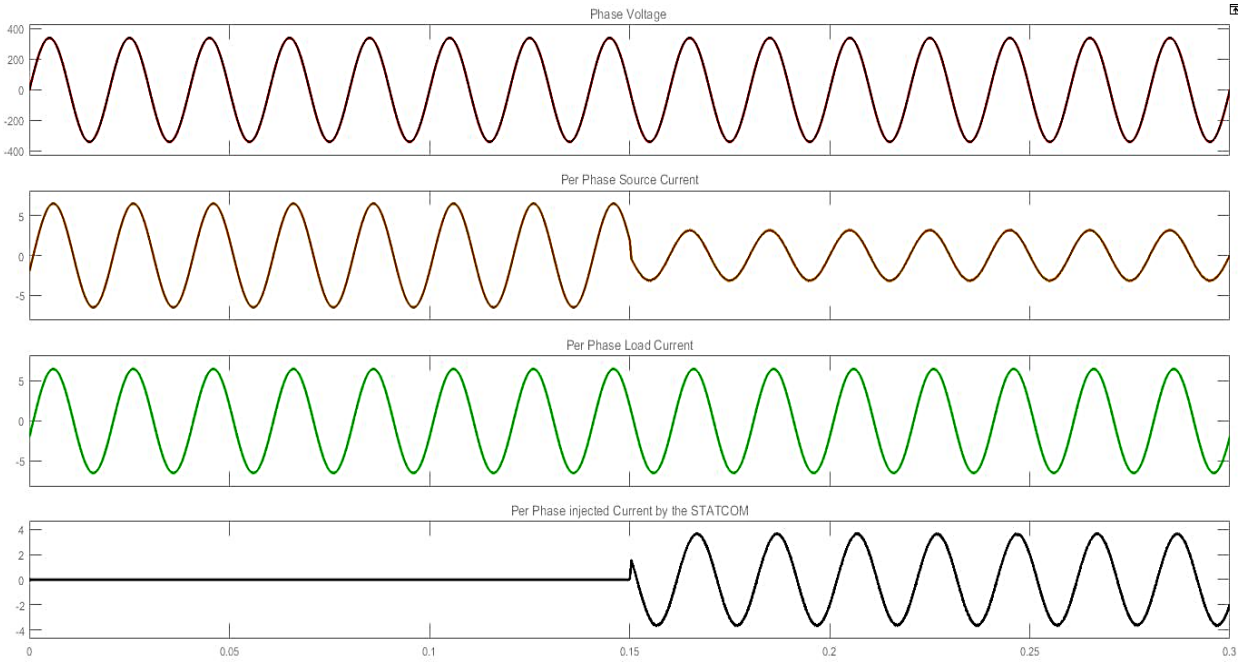


Fig. 4.13 Phase Voltage, Per Phase supply current, per phase load current, per phase DSTATCOM Current

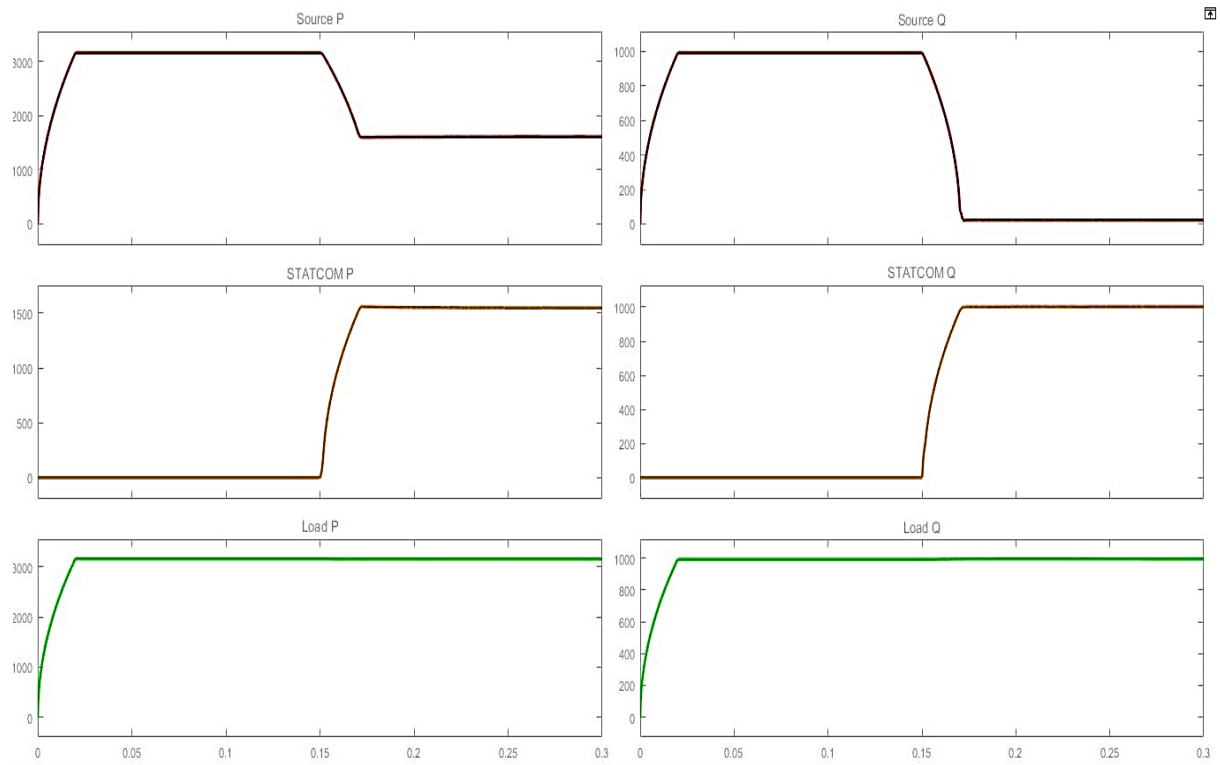


Fig. 4.14 Real and reactive power measured at supply, DSATCOM and load terminals

4.7 Testing of DSTATCOM with WRIG System

In this section, the performance of DSTATCOM along with wind driven WRIG system is tested with the nominal operating voltage of three-phase, 415 V, 50 Hz. The rotor speed of WRIG is set at 1350 rpm. Rotor side inverter DC voltage is maintained at 200 V. Initially its functionality is evaluated with an isolated load of R=50 Ω and L = 50mH (per phase).The DC link voltage is maintained at 600 V. The total load in the set-up is R = 200 Ω and L=0.5H. The simulation environment of DSTATCOM with WRIG is shown in Fig. 4.15. The power flow and voltage magnitudes recorded at the load terminal, DSTATCOM terminal and supply terminal are tabulated in Table -4.3 and displayed in Fig. 4.16 and 4.17, when DSATCOM is used for compensating load reactive power alone. Similarly, the power flow and voltage magnitudes recorded at the load

terminal, DSTATCOM terminal and supply terminal are tabulated in Table -4.4 and displayed in Fig. 4.18 and 4.19, when DSATCOM is used for compensating load reactive power and supplying fraction of the load real power.

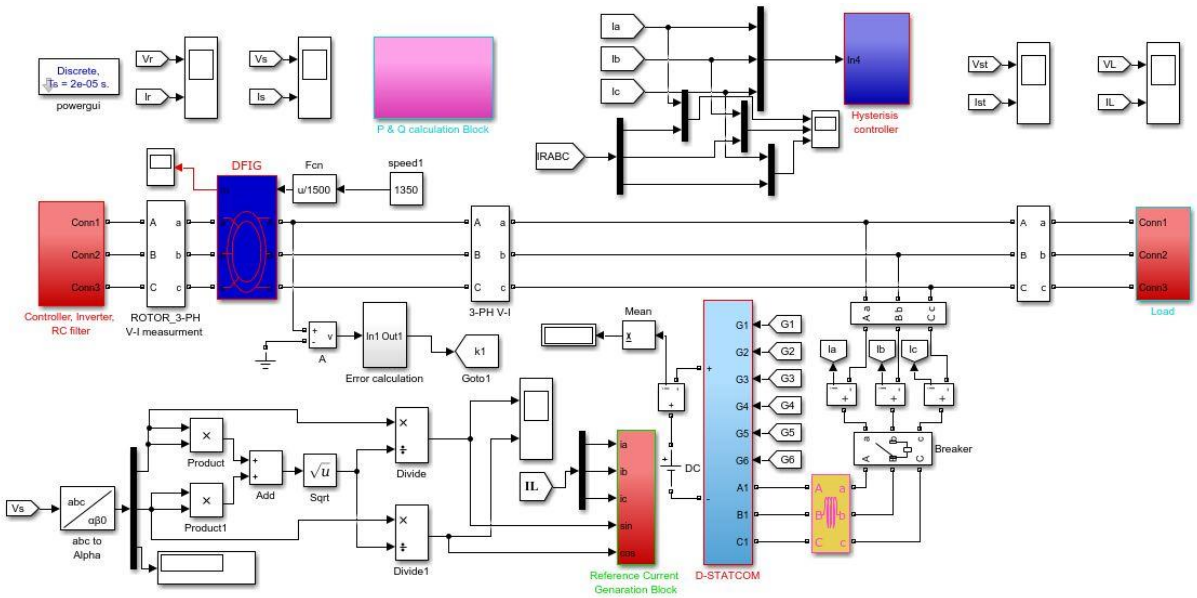


Fig. 4.15 Simulation of DSTATCOM integrated with WRIG

Case : 1 Transfer of only reactive power by DSTATCOM

Table 4.1 Power Flow and Voltage details (transfer of only reactive power by DSTATCOM)

Measuring Points	Before Compensation				After Compensation			
	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)
WRIG	240	1.94	2247	897.9	240	1.87	2346	94.52
Load	240	1.94	2247	897.9	240	1.95	2292	889.8
STATCOM	240	0	0	0	240	0.79	154.1	951.1

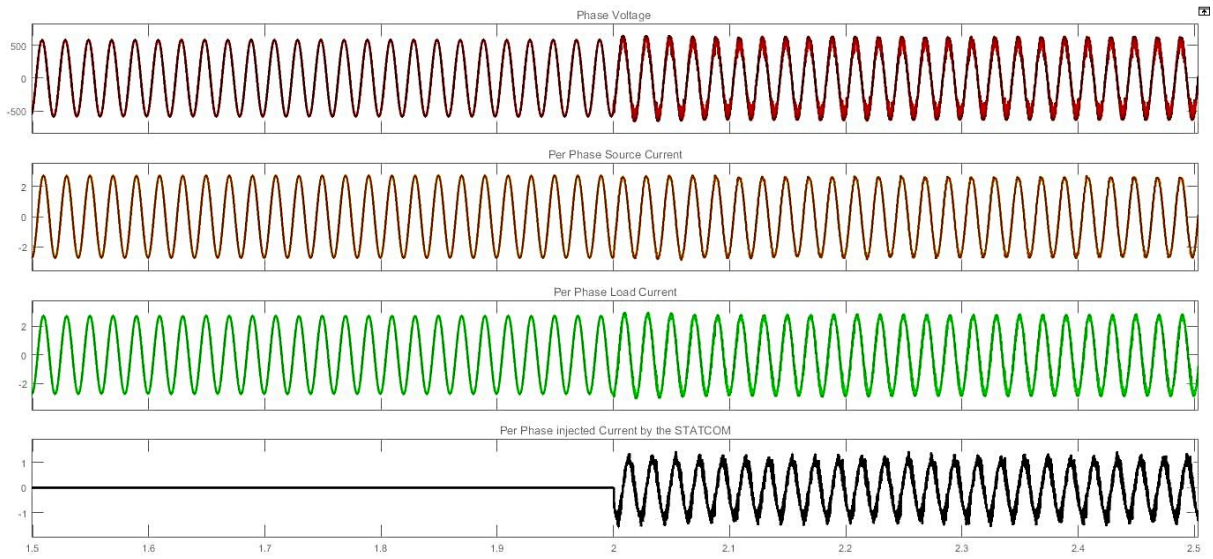


Fig. 4.16 Phase Voltage of WRIG, Per Phase WRIG current, per phase load current, per phase DSTATCOM Current

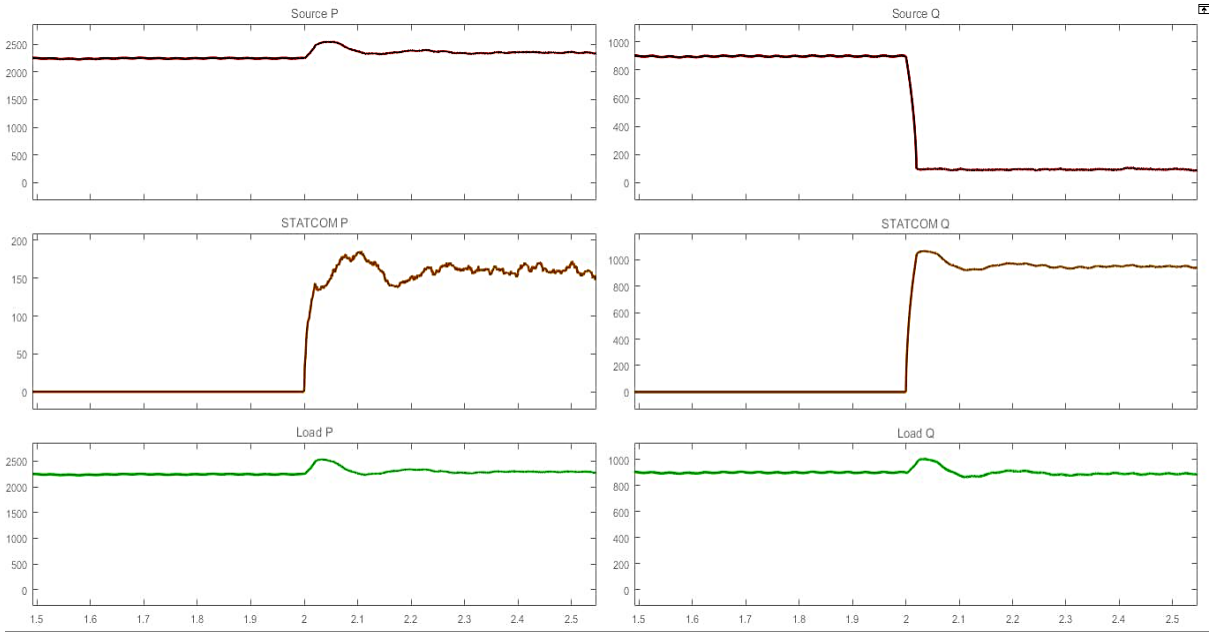


Fig. 4.17 Real and reactive power measured at WRIG, DSTATCOM and load terminals

Case : 2 Transfer of reactive power and 50% of real power

Table 4.4 Power Flow and Voltage details
(transfer of reactive power and 50% of real power by DSTATCOM)

Measuring Points	Before Compensation				After Compensation			
	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)	V_{ph} (V)	I_{ph} (A)	$P_{3Ø}$ (W)	$Q_{3Ø}$ (Var)
WRIG	240	1.94	2247	897.9	240	0.97	1228	86.86
Load	240	1.94	2247	897.9	240	1.95	2304	894.7
STATCOM	240	0	0	0	240	1.14	1084	956.8

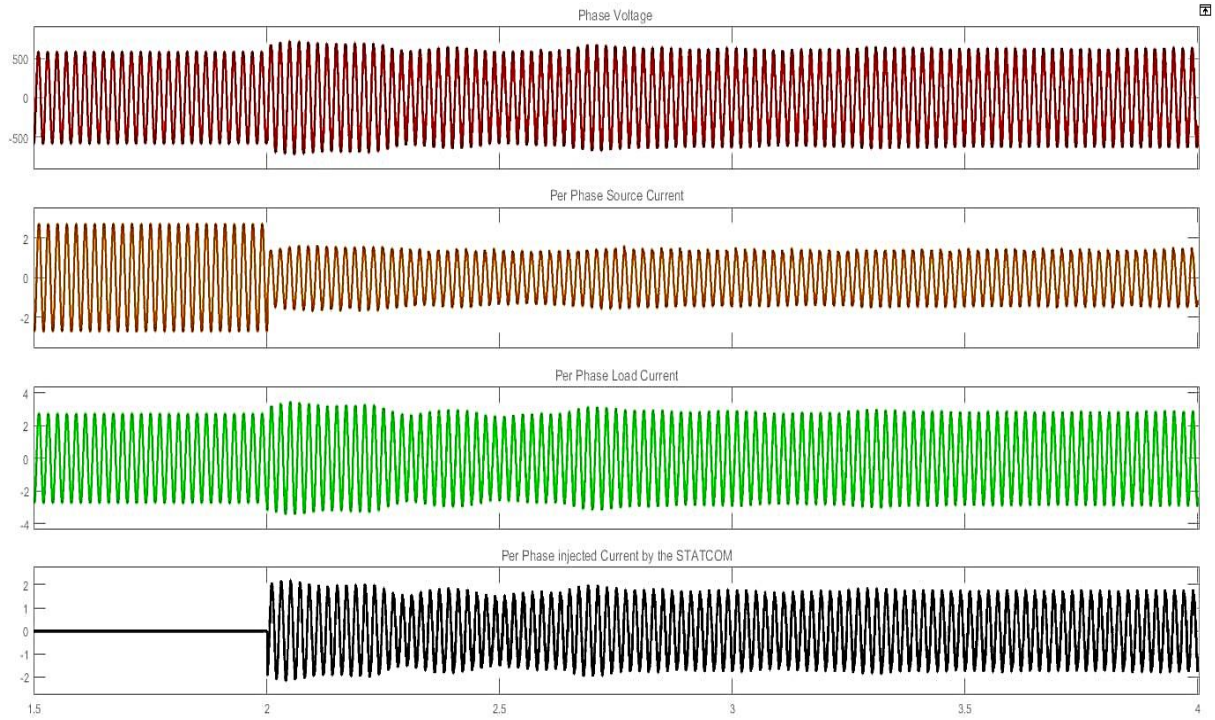


Fig. 4.18 Phase Voltage of WRIG, per phase WRIG current, per phase load current, per phase DSTATCOM current

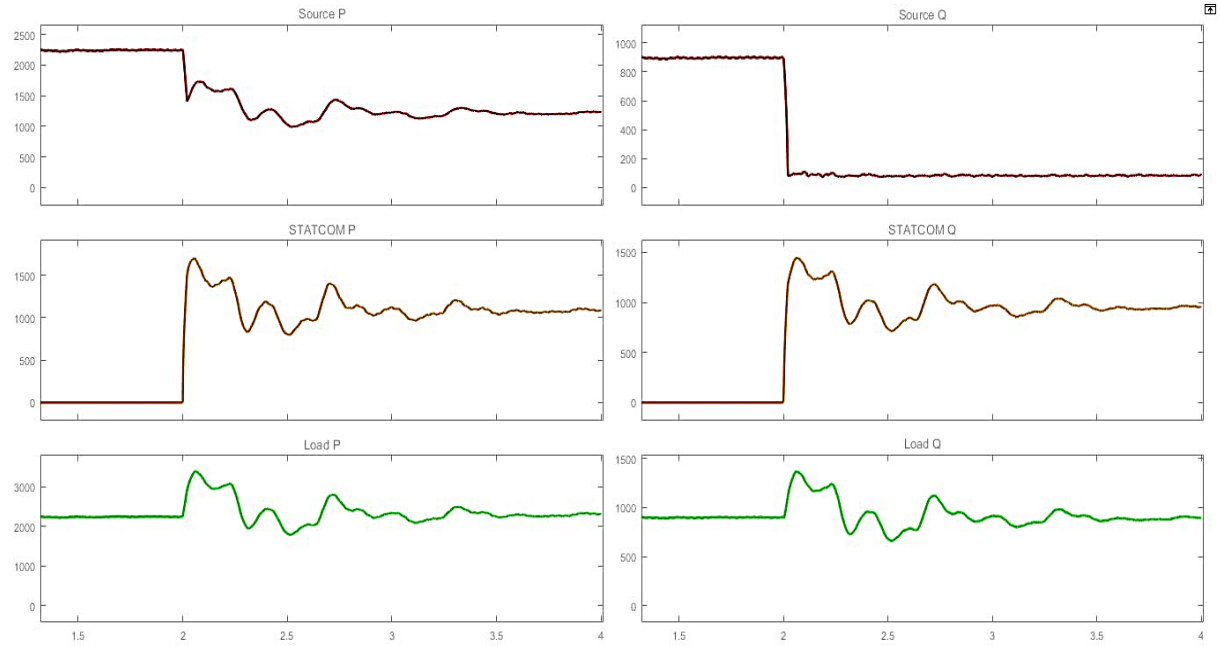


Fig. 4.19 Real and reactive power measured at WRIG, DSTATCOM and load terminals

4.8 Experimental demonstration of DSTATCOM integrated with WRIG

The DSTATCOM developed and tested in the laboratory is connected in parallel with the WRIG experimental setup. Initially the laboratory prototype is tested for reactive power compensation alone and then for transfer of real power along with reactive power compensation.

Case 1: Reactive power compensation alone

The DSTATCOM is controlled in such a way that the reactive power demanded by the load connected at the WRIG terminals is compensated by providing reactive power. Fig. 4.20 (a) shows the WRIG terminal voltage and line current, which is lagging the voltage thus indicating the supply of reactive power. The Fluke meter readings indicating the flow of power at WRIG stator without DSTATCOM is depicted in Fig. 4.20 (b). Fig. 21 (a) presents the WRIG stator voltage and current waveforms with DSTATCOM connected at its terminals. The reference current for DSTATCOM generated by the control algorithm implemented in FPGA is shown in Fig. 21 (b).

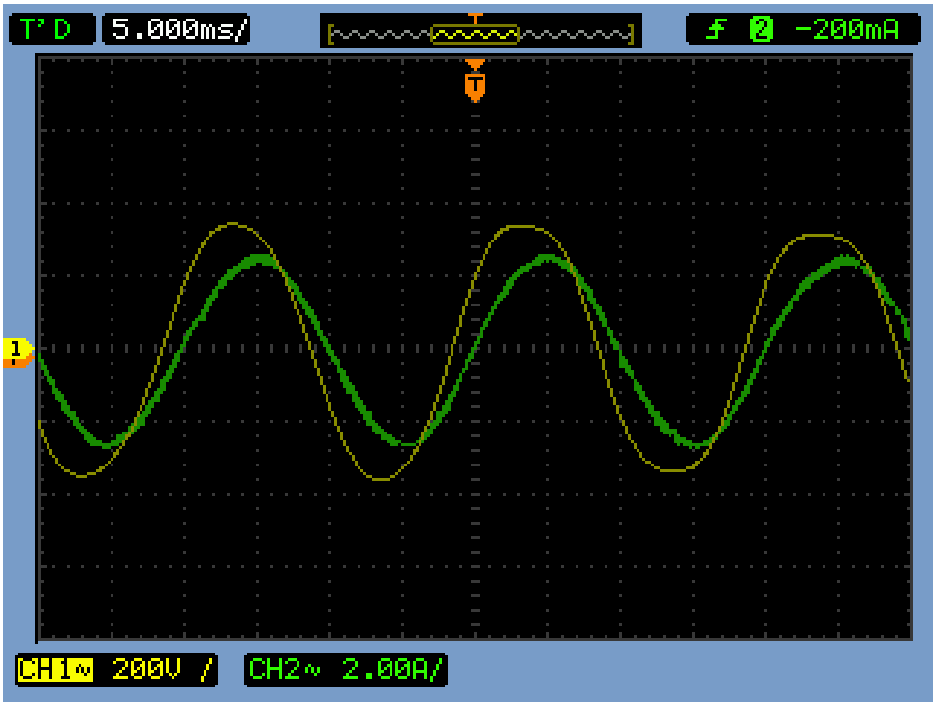


Fig. 4.20 (a) Per phase voltage (Yellow) and current (Green) of WRIG (Without DStatcom)

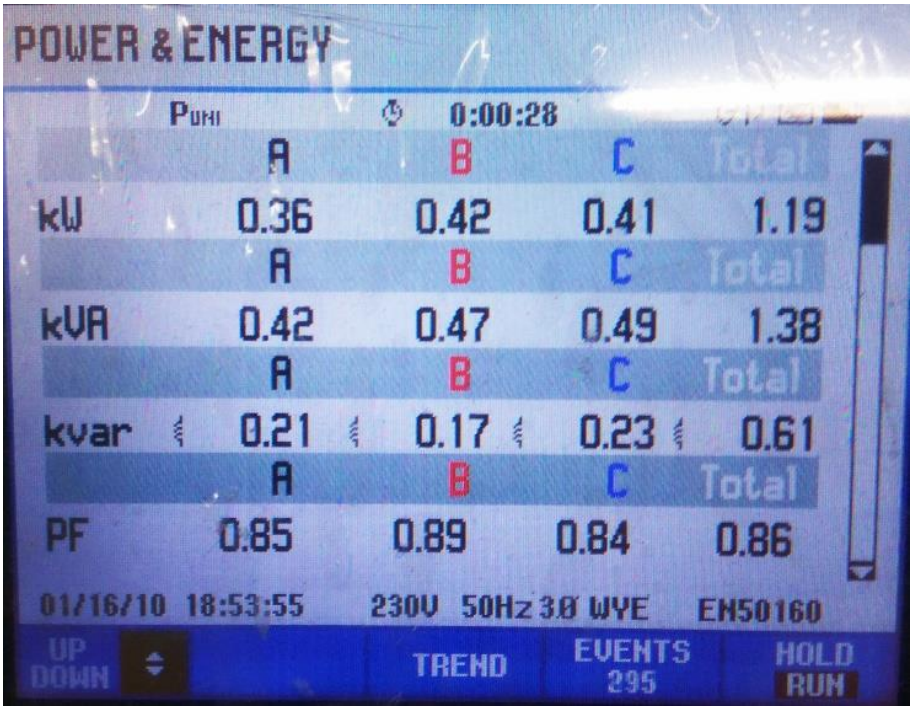


Fig. 4.20 (b) Real and reactive power flow from WRIG (Without DStatcom)

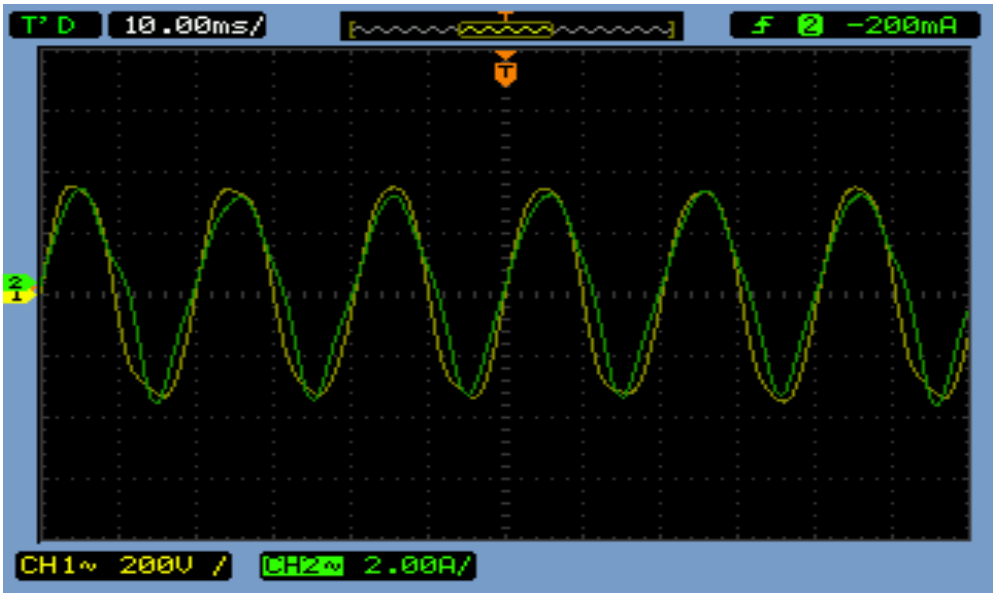


Fig. 4.21 (a) Per phase voltage (Yellow) and current (Green) of WRIG (With DStatcom)

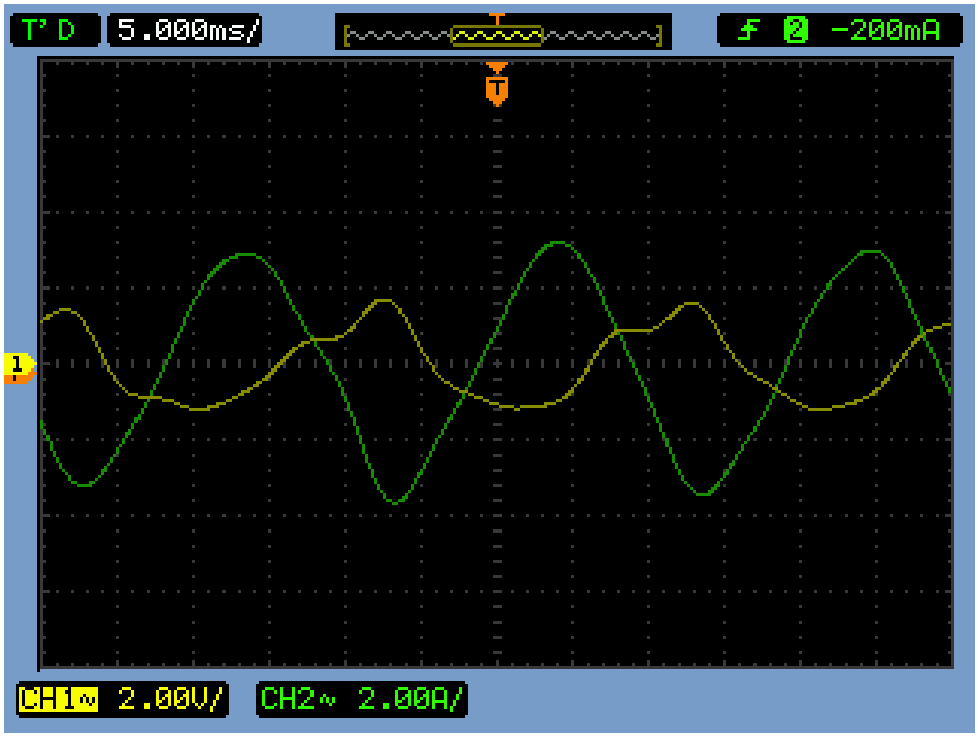


Fig. 4.21 (b) Per phase load current (Yellow) and reference current for DSTATCOM (Green) (With DStatcom)

(Waveforms plotted from DAC output of FPGA)

Fig. 4.21 (c) depicts the real and reactive power flow from WRIG with DSTATCOM connected at its terminals. It can be noted from Fig. 4.20 (b) that the power factor at WRIG terminals is 0.86 lagging and which has been improved to 0.95 lagging using DSATACOM as indicated in Fig. 4.21(c).

Fig. 4.21 (c) Real and reactive power flow from WRIG (With DStatcom)

Case 2: Reactive power compensation along with transfer of real power

The DSTATCOM is controlled to transfer 20% of the total real power demanded by the load. Remaining 80% is met by the WRIG. Fig. 4.22 indicates the Fluke meter readings recorded at the WRIG terminals, DSTATCOM terminals and the load terminals. In the experimental setup, WRIG supplies 1.35 kW of power and DSTATCOM supplies 0.24 kW of real power, while DSTATCOM operates in the capacitive mode and compensates part of the stator magnetizing current requirement of WRIG. This experimentation proves the conceptual working of DSTATCOM to transfer portion of the real power demanded in addition to the reactive power compensation.

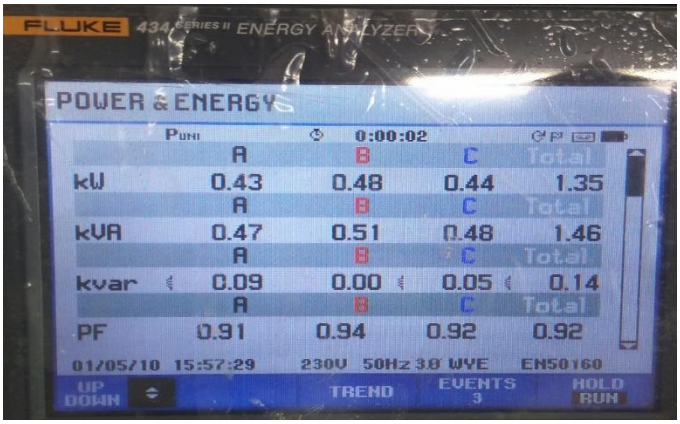


Fig. 4.22 (a) Power flow recorded at the WRIG terminals

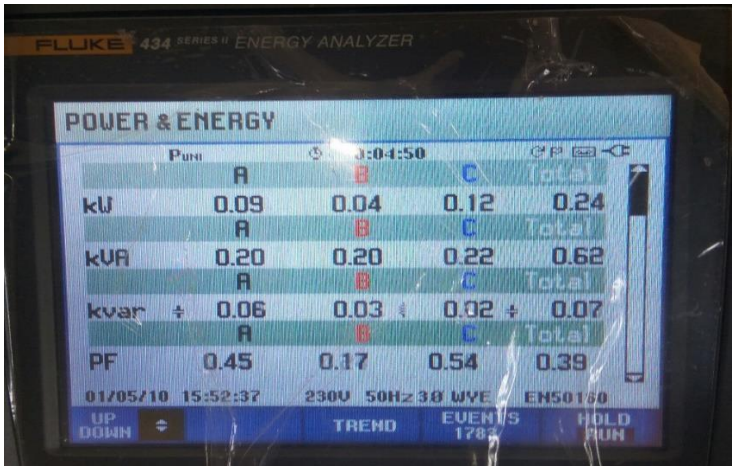


Fig. 4.22 (b) Power flow recorded at the DSTATCOM terminals

Fig. 4.22 (c) Power flow recorded at the load terminals

4.9 Summary

This chapter has described the principle of working of DSTATCOM and its control for reactive power compensation and partial real power transfer to the loads. Initially the developed DSTATCOM has been tested with reduced voltage level and then tested with nominal operating voltage. Further, the DSTATCOM is integrated with wind driven WRIG system (DC Motor driven WRIG in laboratory set up) and its capability to compensate the reactive power demand of the connected loads and transfer of part of real power demanded by the load.

4.10 Publications based on the work discussed in this chapter

1) K. Navin Sam, N. Kumaresan, N. Ammasai Gounden and Rajesh Katyal, "Optimal Reactive Power Controller for Wind-Driven Stand-Alone Doubly-Fed Induction Generators" **International journal of Wind Engineering**, Vol.41, No.2, April 2017, pp.124-143. (eISSN: 2048402X & ISSN: 0309524X)

2) K. Venkatraman, S. Moorthi, M.P. Selvan, P. Raja and Deepa Kurup, "Performance Evaluation of FPGA controlled DSTATCOM for load Compensation", **Arabian Journal of Science and Engineering,** Vol. 41, No. 9, September 2016, pp.3355-3367.(ISSN: 2191-4281)

3) K. Venkatraman, S. Moorthi, M.P. Selvan, P. Raja and Deepa Kurup, "Predictive Current Control of DSTATCOM for VAR Compensation of Grid Connected Wind Farms", **Journal of Renewable and Sustainable Energy,** March 2017. doi: http://dx.doi.org/10.1063/1.4977541

4) Hrishikesan, V.M., Venkatraman, K. and Selvan, M.P., "Performance of Custom Power Devices in SCIG based Windfarms during Abnormal Grid Conditions", ***IEEE International Conference INDICON-2014***, 11-13 December, 2014, Pune, INDIA.

5) Hrishkesan, V.M., Venkatraman, K., Selvan, M.P. and Moorthi, S.," Application of D-STATCOM in SCIG based Wind-farms during Normal and Abnormal Grid Conditions", ***National Power Systems Conference*** *(NPSC 2014),* 18-20 December, 2014, IIT-Guwahati, INDIA

CHAPTER 5

DESIGN OF FPGA CONTROLLER FOR ENERGY MANAGEMENT

5.1 Introduction

This chapter of the report comprises of (i) FPGA controller, (ii) accessory interfaces (iii) algorithm and (iv) implementation of controller and its operation with the system. FPGAs are logic devices which contain a matrix of reconfigurable gate array logic circuitry. These devices offer the combined advantage of high processing speed, re-programmability and parallel processing. The high level of integration available with these devices allow them to implement complex control algorithms. The advent of FPGA technology has enabled rapid design processes. The FPGA architecture consists of three types of configurable elements a perimeter of input/output blocks (IOBs), a core array of configurable logic blocks (CLBs), and resources for interconnection. The IOBs provide a programmable interface between the internal array of logic blocks (CLBs) and the devices connected external to the package pins. CLBs perform user-specified logic functions, and the interconnect resources carry signals among the blocks.

FPGAs have advantages of high speed operation and adaptability which are features of hardware and software respectively. In addition, FPGA has a function of parallel processing. So, FPGA based controllers can be used in various types of applications and in rugged conditions. The re-configurability of FPGAs can provide designers with almost limitless flexibility, unlike hard-wired Printed Circuit Board (PCB) designs that have fixed hardware resources. Unlike processors, FPGAs use dedicated hardware for processing logic and do not have an operating system. Because the processing paths are parallel, different operations do not have to compete for the same processing resources. That means speeds can be very fast, and multiple control loops can run on a single FPGA device at different rates.

5.2 FPGA Controller

The reconfiguration of the interconnection between logic blocks in FPGA can be made whenever there is a need for modification of the design residing in it. The concept of reprogramming in FPGA makes it capable for the design of any digital electronic system in a considerably small time. Consequently, the FPGA-based implementation of digital control schemes is cost effective which confirms its suitability even for small designs. Though there are various other cheaper microcontroller alternatives, the FPGA board offers the following advantages when integrated into a system:

1. Massive parallel processing capability.
2. Real time processing capability.
3. Efficient because of the capability to design even at gate level.
4. Expansion of the system can be done with no extra cost for upgrading the processor.

Thus, the cost of implementing a system in FPGA based processor is justifiable.

The comparison between FPGA and dSpace controller is shown in Table 5.1. From that it's evident that the cost factor and extra hardware requirement makes FPGA a clear choice between them. Another popular embedded controller used in control systems is a microcontroller or MCU. An MCU is time-limited. In order to accomplish more work, you need more processor cycles. Clocks have very real limits to their frequencies, so it's easy to hit a computational wall. MCUs works at lower frequencies and have severe limitations in terms of number of IO pins. Moreover, MCUs work in a sequential manner. The high level of instruction level parallelism boasted by FPGA is simply absent here.

Table 5.1 Comparison between FPGA and dSpace based implementation

Feature	dSpace	FPGA
Implementation	Easy	Relatively Hard
Hardware Requirement	Dedicated PC with high end specs	No separate hardware required
Software Requirement	MATLAB	Nil
Cost	dSpace controller itself costs in lakhs. Need of dedicated PC and licensed MATLAB software adds to the cost.	A fully equipped FPGA board which can work in standalone mode costs around 50k.

Digital Signal Processors (DSPs) are another possible alternative for FPGA. But these processors are difficult to program. They are better suited for applications where one-time programming is sufficient. The lack of sufficient programming resources and support platforms are another drawback. So in conclusion, FPGA based implementation is preferred in such systems which require high speed processing of a large number of sensed signals.

5.3 Altium Nanoboard 3000

Altium nanoboard NB3000XN, shown in Fig. 5.1 is the embedded controller platform used in this work. Altium's NanoBoards are reconfigurable development platforms that give designers high-level access to today's high-capacity, low-cost programmable devices. The NanoBoard is designed to be a perfect complement to Altium Designer, Altium's unified electronic product design environment. Together, they transform the desktop into a complete, interactive electronic design laboratory using Altium's LiveDesign environment. Development and debugging capabilities include a full embedded tool chain for supported embedded processors and a range of embedded instruments, including a Logic Analyzer. NanoBoard 3000XN comes with integration of Xilinx® Spartan™-3AN device (XC3S1400AN-4FGG676C), 4-channel 8-bit ADC, SPI-compatible – providing maximum sample rate of 200ksps , 4-channel 8-bit DAC,

SPI-compatible – operating at clock rates of up to 40MHz and many more functionality of which above mentioned were used extensively in the project.

Fig. 5.1 Altium Nanoboard NB 3000XN

5.4 Accessories to be Interfaced with FPGA

The accessories to be interfaced with FPGA include:

(1) Analog to Digital Converter and its extensions.
(2) Opto-coupler unit
(3) Display units and
(4) Ethernet communication

These accessories will be highly useful for interaction with the external world and enables the FPGA to be a controller for managing the huge power set-up like micro-grids. The Ethernet communication between FPGAs enabled them to be developed as standalone embedded systems without the use of dedicated computers with it.

5.4.1 Analog to Digital conversion

The analog to digital converter unit attached with the FPGA holds only four channels. ADCs are used for translating the analog quantities into digital signals. The ADC ADC084S021 in Altium nanoboard 3000XN is a 4 channel, 8 bit ADC device as shown in Fig. 5.2. It is a low power converter with a high speed serial interface. It is powered from a regulated 3.3V power supply and interfaces to the user FPGA over an SPI bus providing a sampling rate range of

50ksps to 200ksps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit. Successive approximation ADC is the advanced version of Digital ramp type ADC which is designed to reduce the conversion and to increase speed of operation. The major draw of digital ramp ADC is the counter used to produce the digital output will be reset after every sampling interval. The normal counter starts counting from 0 and increments by one LSB in each count, this result in 2^N clock pulses to reach its maximum value.

The limited number of channels presented in this architecture poses a challenge. A total of 12 signals must be acquired using these 4 channels. This is realized by using an analog multiplexer as discussed in earlier section. Among these 4 ADC channels, only 2 are utilized. Six signals are multiplexed and fed to each of these channels. After A/D conversion, they are demultiplexed back to obtain digital equivalent of sensed signals.

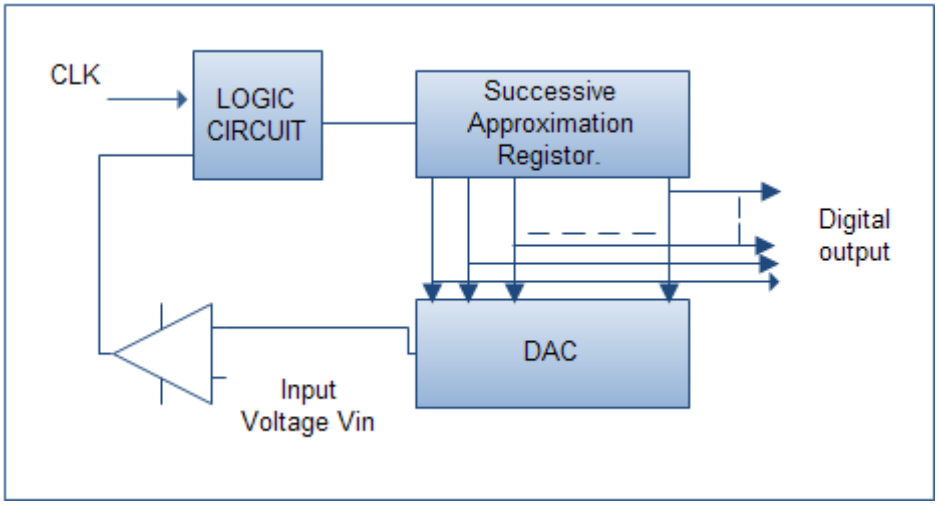


Fig. 5.2 Block diagram representation of SAR type ADC

The output of SAR is converted to analog out by the DAC and this analog output is compared with the input analog sampled value in the Opamp comparator. This Opamp provides a high or low clock pulse based on the difference through the logic circuit. In very first case the 3 bit SAR enables its MSB bit as high i.e. '1' and the result will be "100". This digital output is

converted to analog value and compared with input sampled voltage (V_{in}). If the deference is positive i.e. if the sampled input is high then the SAR enables the next bit from MSB and result will be “110”. Now if the output is negative i.e. if the input sampled voltage is less than the SAR resets the last set bit and sets the next bit and resultant output in this case will be “101” which will definitely approximately equal to the input analog value. The schematic developed in FPGA is shown below in Fig. 5.3.

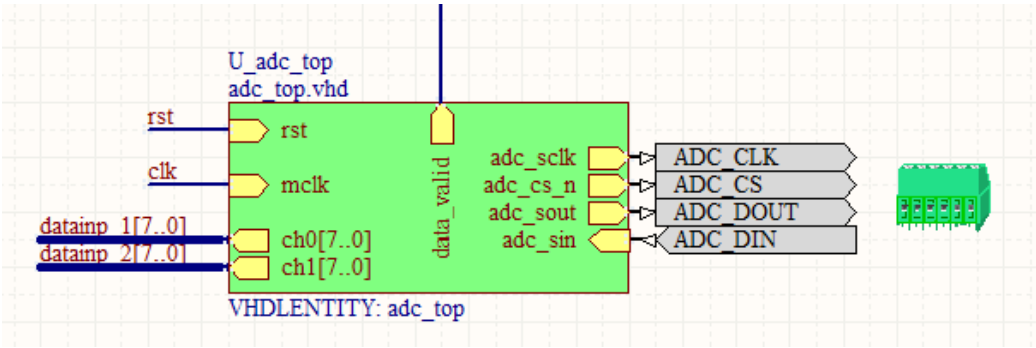


Fig. 5.3 Schematic of ADC module in Altium Design Suite

The ADC module used here has only 4 channels. To enhance the data handling capability, necessitates the use of a multiplexer for signal acquisition. The voltage and current samples obtained from the sensors are fed to two 16 X 1 multiplexers. The frequency of the multiplexer is set to 20 kHz. This high sampling frequency ensures no data is lost while multiplexing. Based on the 4 bit select signals given to the multiplexer, each of these input values are selectively sent to FGPA for further processing.

The MUX used for this application is CD74HC4067E which is a 16 bit multiplexer from Texas Instruments is shown in Fig. 5.4. The 4 bit select lines are used for selecting specific input from the 6 inputs of each multiplexer.

Table 5.2 shows the logic implementation of the select lines to MUX and ADC:

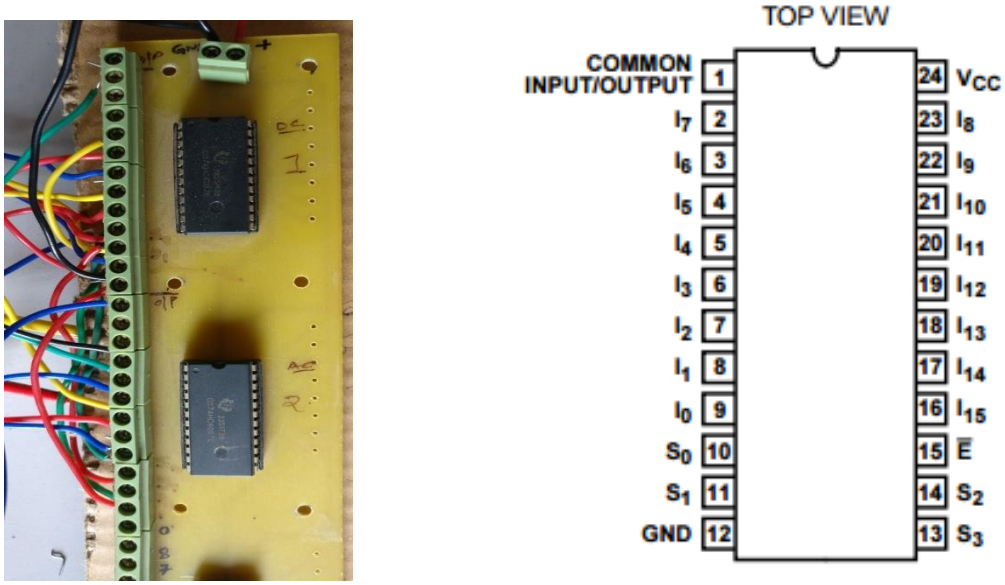


Fig. 5.4 Multiplexer and its pin diagram

Table 5.2 I/O of multiplexer

S_3	S_2	S_1	S_0	MUX1	MUX2
0	0	0	0	V_a	I_{lc}
0	0	0	1	V_b	I_{ln}
0	0	1	0	V_c	I_{inj_a}
0	0	1	1	V_{dc}	I_{inj_b}
0	1	0	0	I_{la}	I_{inj_c}
0	1	0	1	Il_b	I_{inj_n}

Here, V_{abc} represents phase voltages, I_{labcn} represents load currents. I_{inj_abcn} stands for injected currents and V_{dc} for dc link voltage. Select signals to MUX are shown in Fig. 5.5.

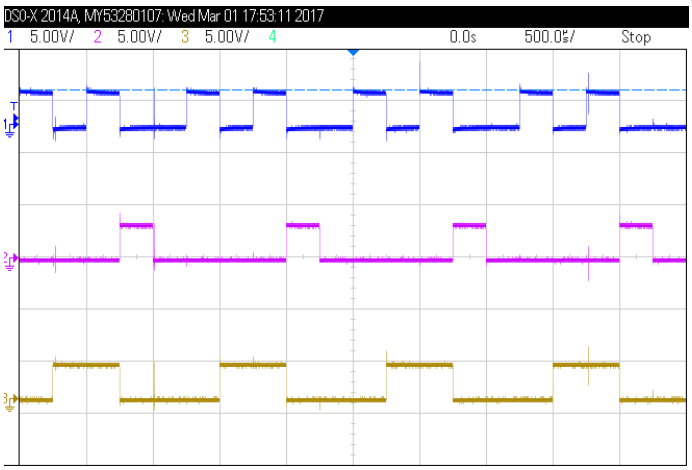


Fig. 5.5 Select signals to MUX

Fig. 5.6 shows the output voltage signals from the LEM voltage sensors. Another important thing to take care while tuning the sensors is to keep their values almost identical. In other words, level shifted signal output from the current sensors must be identical to each other. Same holds true for voltage sensors. Else the compensation will not happen effectively. Figure 5.7 shows the output of MUX1. All the signals applied to its input appears in a time multiplexed manner. These signals then need to be separated by using suitable logic inside FPGA and shown in Fig. 5.8.

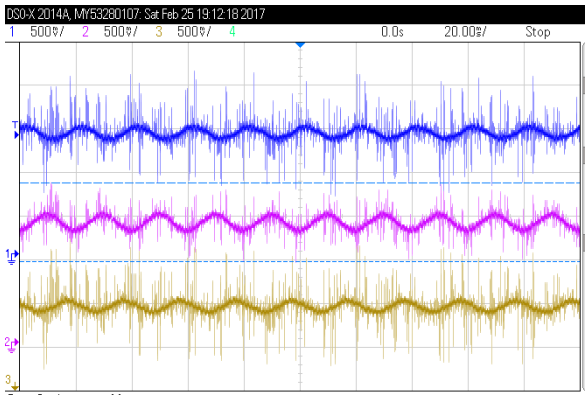


Fig. 5.6 Sensor phase voltage waveforms

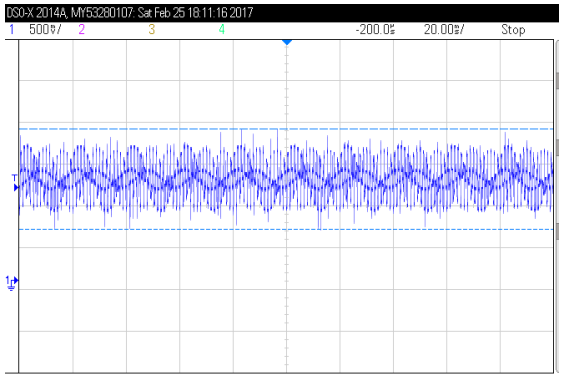


Fig. 5.7 MUX1 output waveform

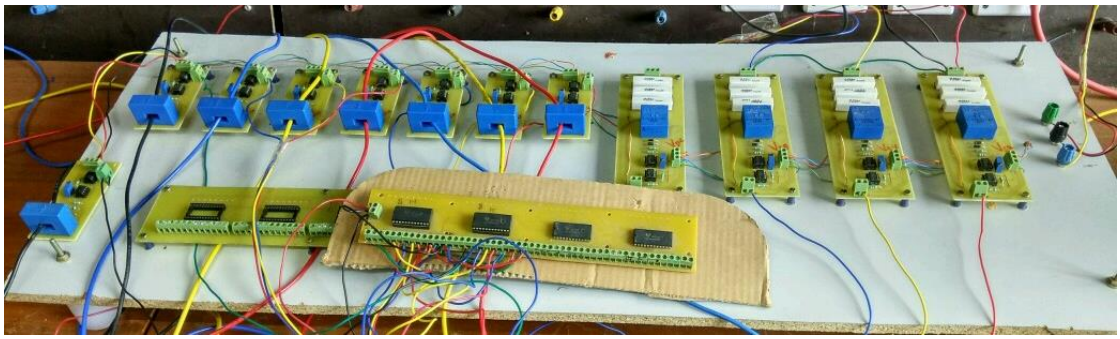


Fig. 5.8 Implementation of analog signal acquisition board

5.4.2 Signal Amplification and isolation circuits

The output pulses from FPGA switches between 0 and 3.3V. This voltage level is not high enough to turn ON the IGBT switches used in four leg inverter. Besides the maximum current sourcing capability of FPGA is also limited. Keeping these two aspects in mind, a gate driver IC is used to properly trigger inverter switches. The most commonly used gate driver ICs are HCPL3101 and ULN2003.

(a) HCPL3101

The HCPL3101 shown in Fig. 5.9 consists of an LED optically coupled to an integrated circuit with a power output stage. These optocouplers are suited for driving power MOSFETs and IGBTs used in motor control inverter applications. The high operating voltage range of the output stage provides the voltage drives required by gate controlled devices. The voltage and current supplied by these optocouplers allow for direct interfacing to the power device without the need for an intermediate amplifier stage.

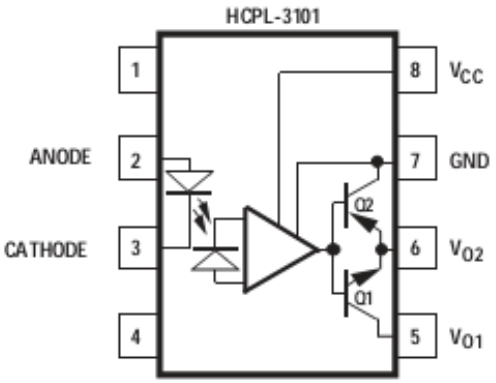


Fig. 5.9 Pin diagram of HCPL3101

The HCPL-3100 switches a 3000 pF load in 2 µs and the HCPL-3101, using a higher speed LED, switches a 3000 pF load in 0.5 µs. With a CMR rating of 15 kV/µs typical these opto-couplers readily reject transients found in inverter applications. The LED controls the state of the output stage. Transistor Q2 in the output stage is on with the LED off, allowing the gate of the power device to be held low. Turning on the LED turns off transistor Q2 and switches on

transistor Q1 in the output stage which provides current and voltage to drive the gate of the power device.

(b) ULN2003

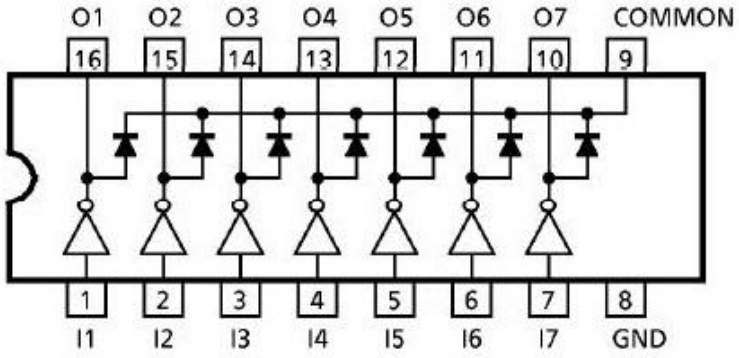


Fig. 5.10 Pin diagram of ULN2003APG

ULN2003 is a high voltage and high current Darlington array IC. It contains seven open collector darlington pairs with common emitters. A darlington pair is an arrangement of two bipolar transistors. Each channel or darlington pair in ULN2003 is rated at 500mA and can withstand peak current of 600mA. The inputs and outputs are provided opposite to each other in the pin layout. Each driver also contains a suppression diode to dissipate voltage spikes while driving inductive loads. The pin diagram of ULN2003 driver is given in Fig. 5.10.

Although the ULN2003 driver is easy to use, it lacks an important factor – isolation between power circuit and gate circuit. Hence the controller circuit is at greater risk if used with the ULN IC. It's always recommended to use HCPL gate driver instead of ULN for firing the IGBT switches of an inverter.

5.4.3 Display units

The hardware requirements for displaying the information on VGA monitor from FPGA board include a soft-core processor inside FPGA (TSK 3000A – 32 bit RISC processor), VGA controller and SRAM controller. The TSK3000A processor executes the native software code to boot up the FPGA board and initialization of other software wrappers apart from executing

user written software code. The VGA controller provides the interface between the hardware controller elements on the FPGA board and the software wrappers to bring up and initialize the VGA monitor. The SRAM controller provides memory for the display operations in terms of data buffers where the data is stored before it is sent to the VGA monitor. The flowchart for the software code, which runs for the display of information on VGA monitor, is shown in Fig. 5.11. The graphics t structure (inbuilt) initializes the display driver on the

FPGA board further it activates all hardware components and runs all associated software wrappers, which deal with initializing the display drivers on the FPGA board and the VGA monitor. The canvas t structure (inbuilt) helps the user in initializing in a way it has to be displayed in the monitor. Once the graphics driver and canvas are initialized, the canvas is filled with any background color and is set to visible. Thereafter, information is passed onto the monitor for display in terms of a string, x and y coordinates of position of display, text color and styles. Since the developed display system is an online monitoring system, the program runs individually for all the data that has to be monitored. Whenever there is a change in the monitoring data such as change in measured parameters, the display is updated after erasing the existing data.

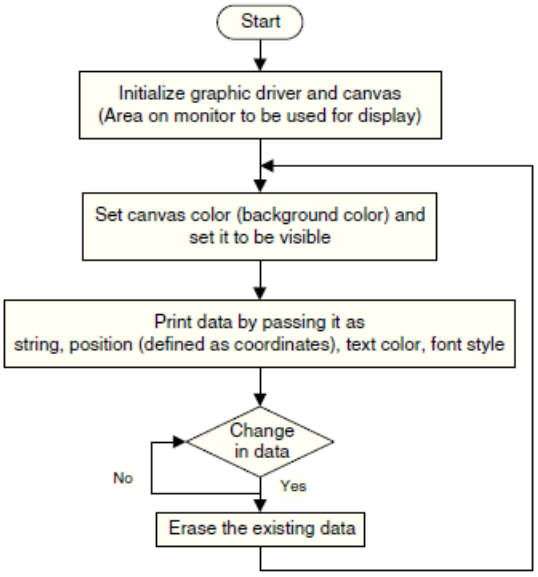


Fig. 5.11 Flow chart for the display of information in the VGA monitor

5.4.4 Ethernet Communication

Ethernet is a common name given to various closely related network standards. As a network standard, each version of Ethernet employs specifications for the physical network layer to organize and control the transfer of data. Protocols like Internet Protocol (IP) define communications without reference to the physical transport medium. Thus a TCP protocol is employed along with IP. TCP establishes connections, sequences and acknowledges packets sent, and recovers packets lost during transmission, thereby making it extremely reliable for communication. TCP breaks down the data into several packets at sending machine and assemble the packets at the machine where it is received. Packets are chunk of data grouped into one or more wrappers that identifies the particular chunk of data and route them to the appropriate destination. The wrappers consist of chunk of data along with few additional bits at the beginning and end which are called the headers and trailers respectively. The placement of these headers and trailers in each type of required information is decided by the network protocols.

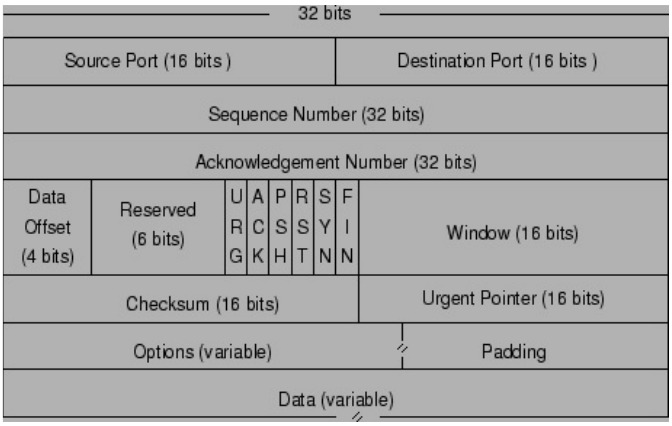


Fig. 5.12 TCP data format

From Fig. 5.12, it can be seen that TCP contains source port which is a 16-bit port number of the process that originated the TCP segment on the source device. Similarly, it also contains the destination port which is also a 16-bit port number of the process that is the intended recipient of the message. Added to these there are few other bits such as acknowledgement bit,

synchronizing bit, finish bit etc. for the proper synchronization, establishment of connection and transfer of data.

The design is developed for Altium Nanoboard (NB3000) FPGA host board which employs a TSK3000A (32-bit soft core). The processor is interfaced with many peripherals such as Random Access Memory (RAM), Ethernet port, SPI master controller, TFT display, touchscreen pointer context and I/O port. The TSK3000A is a RISC processor compatible with the Wishbone bus system. The Ethernet family of peripheral devices provide an interface between a processor and a physical layer device through the support of the IEEE802.3 Media Independent Interface (MII). Communication with multiple slave SPI peripherals are controlled by the SPI master controller. The TFT display unit provides a 32-bit interface between a host processor and a TFT LCD module. The controller supports the native module screen resolution of 240x320 and 320x240 and has a timing unit which is capable of generating all required control and timing signals. The pointer component detects the touchscreen pen input and feeds it to the processor. The I/O port block is a Wishbone-compliant, configurable parallel port unit, providing a simple register interface for storing data to be transferred to/from other devices in a design.

5.5 Implementation of FPGA based Energy Management System

Nomenclature

P_L	**–**	**Total Load Power**
P_{WRIG}	**-**	**WRIG output power**
P_{PV}	**-**	**Power from PV panels**
Ps	**-**	**Power supplied D-STATCOM**
P_B	**-**	**Balance Power**
ε	**-**	**Tolerance value for power mismatch**
V_B	**-**	**Battery Voltage**
V_{Bmin}	**-**	**Permissible minimum battery voltage**

The algorithm is framed based on the inputs received through various sensing units like voltage and current sensors, tacho-generator etc.

(1) The three-phase load voltage and current, and rotor speed are sensed from the WRIG to determine the total load power (P_L).

(2) The PV voltage and current values in addition to the battery voltage are sensed to determine the power fed from PV to the rotor terminals.

(3) A look-up table reference to determine the WRIG output power (P_{WRIG}) from the rotor speed is used.

(4) Comparison of P_L and P_{WRIG} is done.

   (a) If P_{WRIG} is greater than the load power, there will be an indication shown that some more loads can be added.

   (b) If P_{WRIG} is less on comparison, another comparison will be initiated for further action.

(5) Based on a check, $P_{PV} - P_S \geq P_L - P_{WRIG}$, further course of action in the controller will be initiated.

   (a) If the condition holds true, the signal from FPGA will be initiated to operate the DSTATCOM to transfer the additional real power, which will be updated as $P_S^{new} = P_S^{old} + \Delta P_S$ where $\Delta P_S = P_L - P_{WRIG}$ and an indication of 'more loads can be added' is given from the controller. The controller will now start calculating the new sensor values of WRIG and PV for further control action.

   (b) If it is false, the DSTATCOM will be operated to supply $P_S = P_{PV}$.

(6) After the operation of DSTATCOM to supply for equalising $P_S = P_{PV}$, compute the balance power, $P_B = P_L - P_{WRIG} - P_S$

(7) Now, the balance power P_B will be compared with a tolerance value, Є. Then the conditions $P_B \geq$ Є or the battery voltage $V_B \leq V_{Bmin}$ will be checked.

(a) If the condition holds false, there will be an indication of 'No more loads can be added' and the controller will sense the new values from the sensors of WRIG and PV for the control action.

(b) If the condition holds true, the controller will check for the low priority load and switch it OFF to balance the power. Also, there will be an indication that 'No more loads can be added'. After this action, the controller will compute the new power values and follow the steps from the beginning for newly sensed values.

(c) Suppose, if there is no low priority loads available to switch OFF, the controller will initiate a signal to switch ON SCIG to balance the power. Also, there will be an indication that 'No more loads can be added'. Following this action, the controller will wait for the newly sensed values from WRIG and PV to start the control action from the beginning.

The flow chart is incorporated as a controller in the FPGA hardware which will manage the energy flow in the entire system.

The Digital controller is developed using Verilog HDL program and synthesised to implement inside the FPGA. All sensed values which will be analog are fed through the Analog to Digital Converter (ADC) and the digitized values are fed to the FPGA IC which will process those values to calculate the power and other parameters. The FPGA board used for this implementation is Altium Nanoboard 3000 which used Spartan 3 AN FPGA in it. The technical details of this board is provided in section 5.3.Since the number of signals to be sensed is more an Analog Signal Acquisition Card (ASAC) which was discussed in section 5.4.1 has been utilised to fetch all the required analog values and they are converted into digital for computation. The flow chart of the energy management system to manage and maintain the

power balance in the developed micro-grid is shown in Fig. 5.13. The overall schematic of the controller is shown in Fig. 5.14 which shows the different modules incorporated inside FPGA.

The FPGA controller will compute all the power values and compares with the available look-up table reference value. The action signal will be initiated from the FPGA for further course of action in the power set-up. The signals generated from the FPGA are used as control signals by feeding it through an opto-coupler HCPL 3100 which is also explained in section 5.4.2.

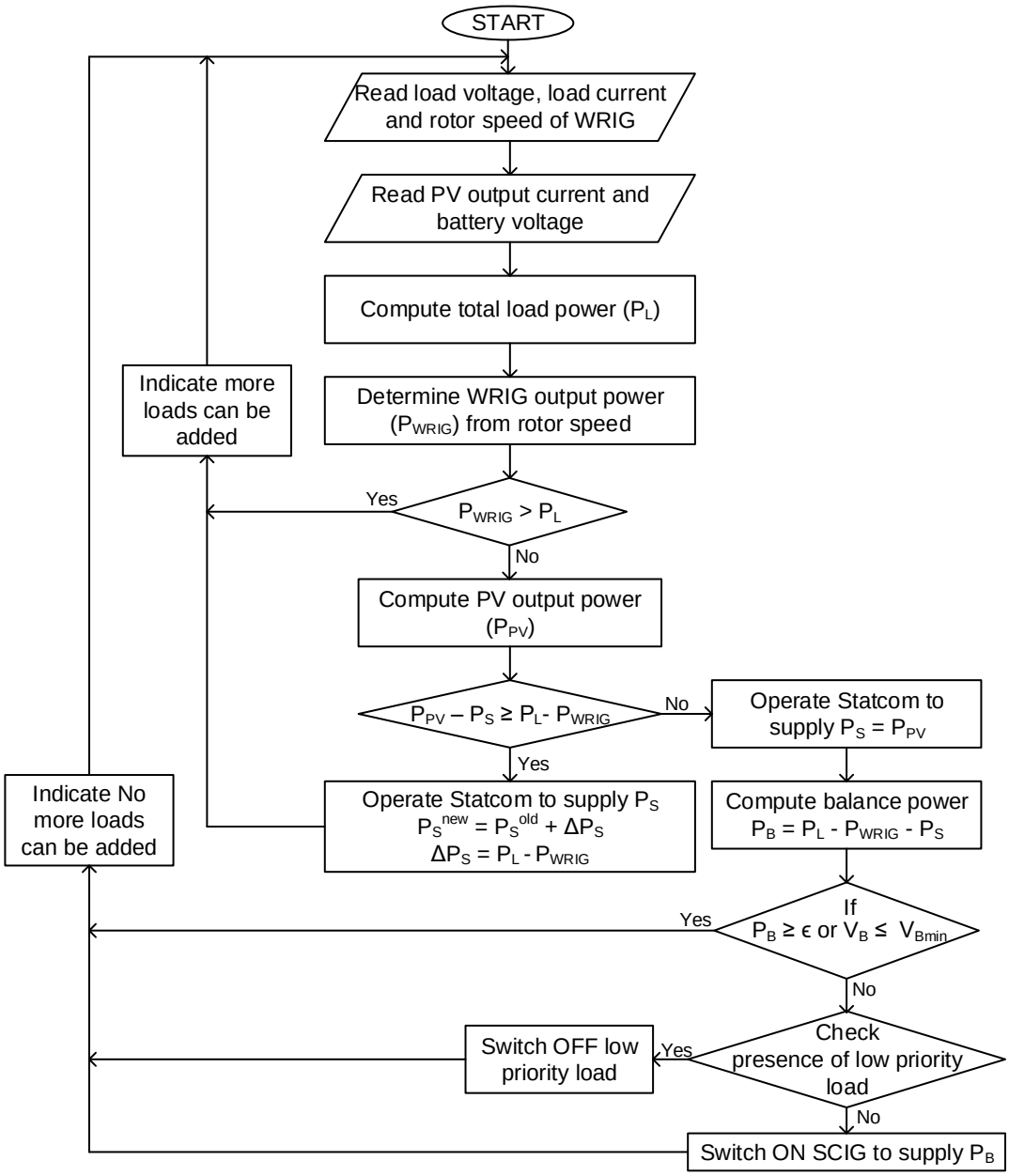


Fig. 5.13 Flow chart of the overall management system implemented in FPGA

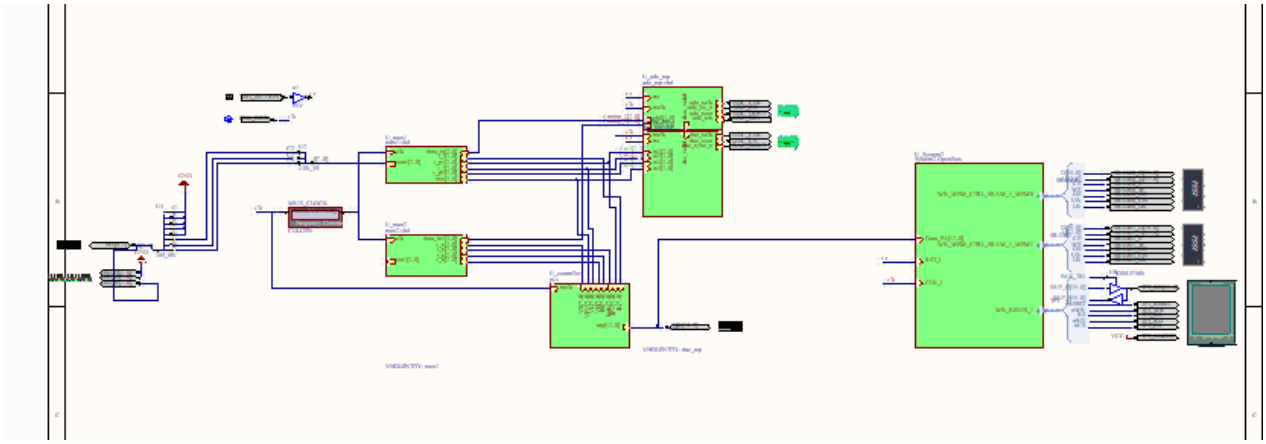


Fig. 5.14 Schematic of the Controller unit implemented inside FPGA

5.6 Summary

The FPGA based energy management system is implemented using Altium Nanoboard (NB 3000) and tested the algorithm for its various conditions. The insights of the FPGA, its capabilities, level of interaction with the accessories and its versatility for using it as controller are discussed. The responses from the controller unit has been reported in this chapter. Hence, the FPGA controller for energy management is tested for its features.

Chapter 6

SIMULATION OF PROPOSED MICROGRID SYSTEM

6.1 Introduction

Simulation of the proposed microgrid system shown in Fig. 1.5 was carried out in MATLAB/Simulink environment to show the integrated working of all the components in the WRIG-based microgrid.

6.2 Modelling of overall system in MATLAB/Simulink environment

The model of the overall system in MATLAB is shown in Fig. 6.1. A WRIG equivalent to the one used in the hardware prototype has been modelled in MATLAB/Simulink. The rating of the WRIG is 3 hp, 415 V, 50 Hz. The machine parameters have been measured by conducting appropriate tests, and used in this model. An inbuilt 210.16 W PV panel, with open-circuit voltage of 35. V and short-circuit current of 7.85 A at standard test conditions has been used for the purpose of simulation. The panel voltage at maximum power point, V_{mp} is 28.4 V, and the corresponding current I_{mp} is 7.4 A. Ten such panels are connected in series to form a PV array. The maximum power P_{mp} of the PV array is 2.1 kW.

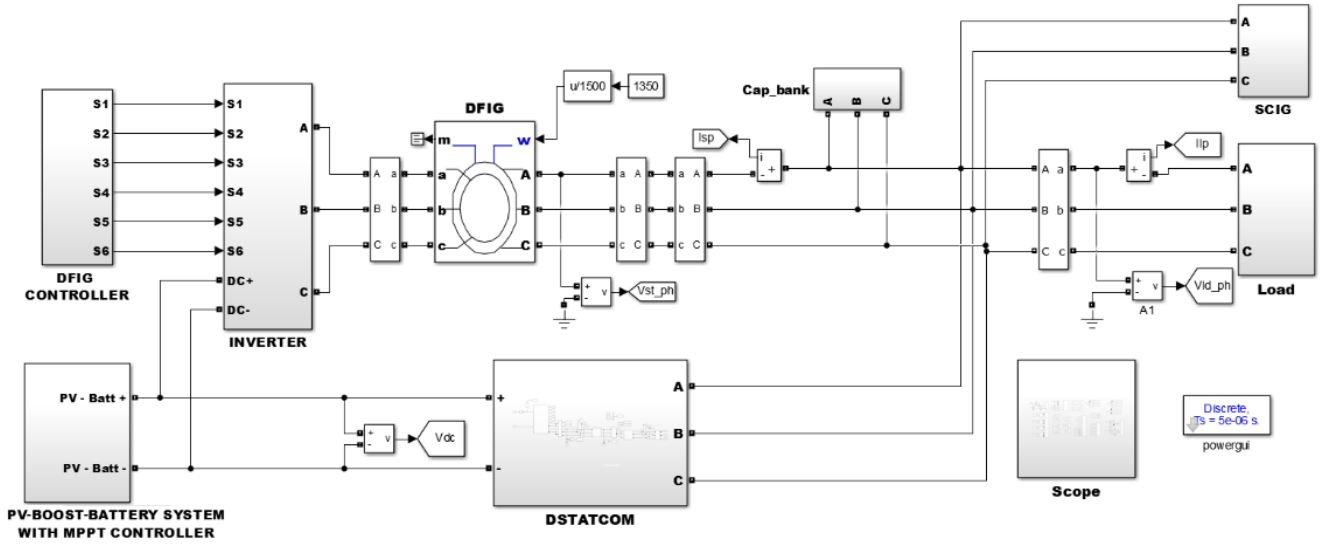


Fig. 6.1 Overall system in MATLAB/Simulink environment

The output of PV-array is utilised for supplying the required WRIG rotor power, DC link power of DSTATCOM as well as charging the battery bank rated at 440 V, 100 Ah. The battery bank clamps the DC link voltage of the WRIG rotor-side inverter and DSTATCOM, and also aids the PV array to supply required DC link power. To emulate the diesel generator, a 3 hp, 415 V, 50 Hz squirrel-cage induction generator has been modelled in MATLAB/Simulink. The parameters of the SCIG is same

s the machine used in the laboratory. A balanced three-phase star-connected passive element (R / R-L branch) has been considered as the load. The value of branch resistance/inductance has been changed to emulate different load setting.

The components of each block given in Fig. 6.1 are given separately below. The PV-boost converter-battery system along with MPPT controller is shown in Fig. 6.2. A DC-DC boost converter is designed and modelled using Simulink block set to interface the PV array with the battery bank and also to extract maximum power from the array. As the output voltage of boost converter, V_{BOOST} is fixed (445 V), any change in PV irradiation level is reflected in the magnitude of the boost converter output current I_{BOOST} alone. Hence, it is sufficient to sense only one signal (I_{BOOST}) for tracking the maximum power point here. The PV MPPT controller, computes the duty cycle of the power switch by sensing I_{BOOST}, and ensuring that this value is maximum corresponding to the irradiation level. The switching pulse for the power MOSFET is generated by comparing the duty cycle value (limited to a range of 0.20 – 0.75 for safe operation of boost converter) with a 10 kHz sawtooth signal of unit magnitude. The PV power generated is utilised for charging the battery bank as well as feeding the required WRIG rotor power and the set value of the real-reactive power of the DSTATCOM.

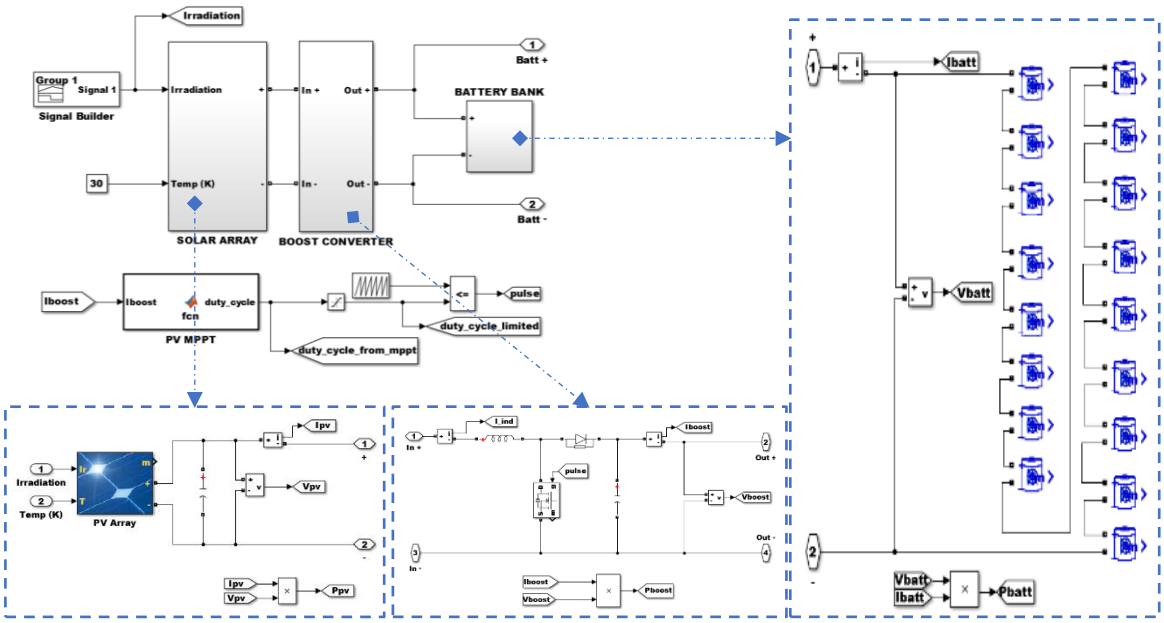


Fig. 6.2 Model of PV-BOOST converter-battery system in MATLAB/Simulink

The WRIG controller along with the pulse generation circuit for the rotor-side SPWM inverter is shown in Fig. 6.3. A simple PI controller is employed to maintain the magnitude of WRIG stator terminal voltage as 415 V. The error in WRIG voltage is constantly minimised by generating appropriate modulation index for SPWM rotor-inverter. The reference signal of the IGBT-based SPWM inverter shown in Fig. 6.4 comprises of three-phase balanced sinusoidal signals at slip frequency and magnitude equal to the modulation index. The switching pulses for the six power devices are generated by comparing the three-phase reference signals with a triangular signal of 10 kHz frequency.

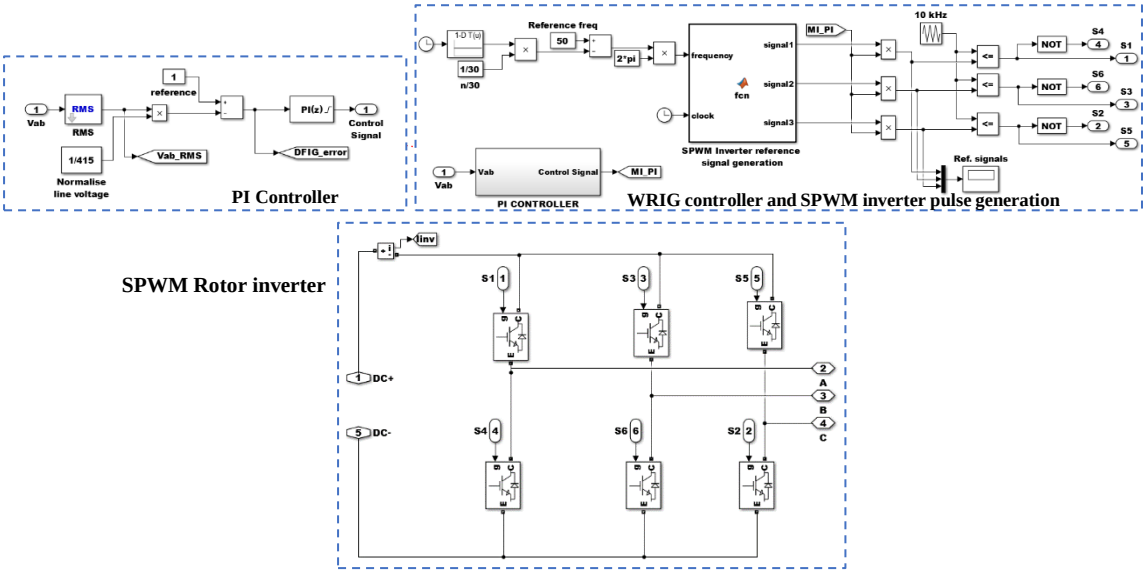


Fig. 6.3 Model of WRIG Controller and Pulse generation for rotor-side SPWM inverter

The wound rotor induction generator with measuring blocks is shown in Fig. 5.

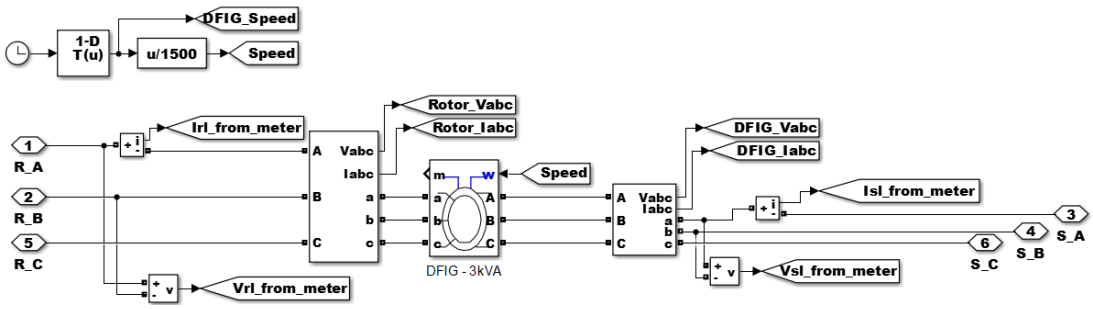


Fig. 6.4 Model of WRIG with measuring blocks in MATLAB/Simulink environment

A three-phase delta-connected 2 kVAr capacitor bank utilised for additional reactive power support for the PV-battery system is shown in Fig. 6.5. It is to be noted that this block is disconnected when demonstrating the operation of the system without capacitor bank.

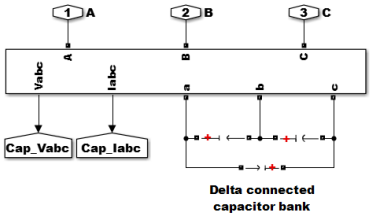


Fig. 6.5 Model of three-phase delta-connected capacitor bank in MATLAB/Simulink

A three-phase asynchronous machine block, shown in Fig.6.6 has been used to simulate the diesel generator employing a squirrel-cage induction generator for forming the AC microgrid. A three-phase star-connected resistive branch as shown in Fig. 6.7 has been used as a load in the microgrid system.

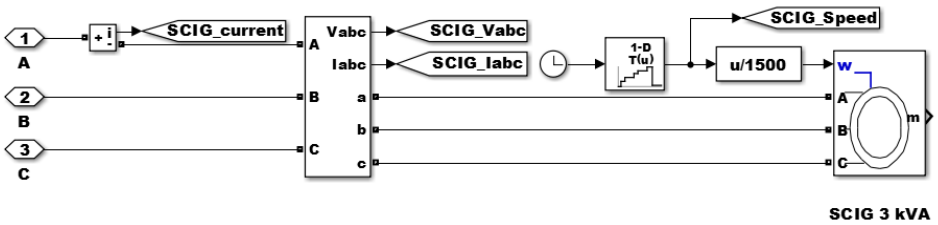


Fig. 6.6 Model of three-phase SCIG in MATLAB/Simulink environment

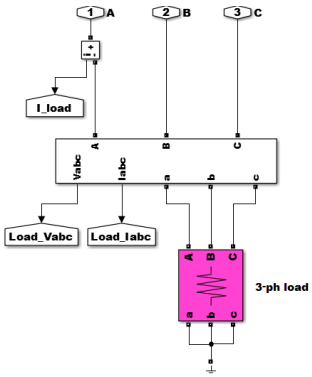


Fig. 6.7 Model of three-phase resistive load in MATLAB/Simulink

The model of DSTATCOM and its controller is shown in Fig. 6.8. As the DC bus voltage is only 440 V (for battery SOC 82 %), the maximum RMS output voltage of DSTATCOM is 270 V for a modulation index of unity. Hence, a three-phase step-up transformer is required for integrating the DSTATCOM with the micro-grid. This can be seen in Fig. 6.9 along with the measuring blocks.

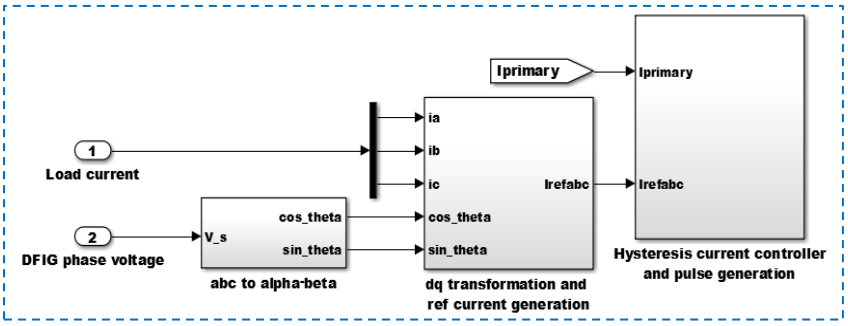
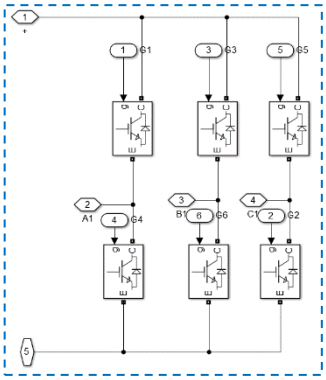


Fig. 6.8 DSTATCOM and controller circuit



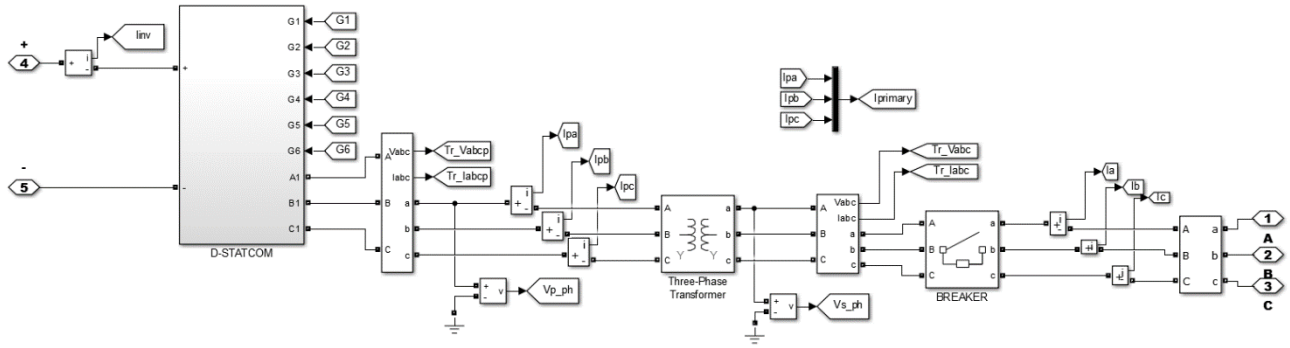


Fig. 6.9 Integration of DSTATCOM with microgrid

6.3 Simulation Results

The simulation of the system was carried out, and results are presented to demonstrate the operation of the system without and with capacitor bank, and with DSTATCOM connected to the system for both real and reactive power support. For each of the above cases, the operation of the system is shown for different possible scenarios mentioned below in Table 6.1.

Table 6.1 Modes of operation of proposed Microgrid system

DIFFERENT MODES OF OPERATION OF PROPOSED MICROGRID			WRIG Speed	SCIG Speed	Irradiation	Load
CASE I	Without external reactive power support	**(a)**	Constant	Varying	Varying	Constant
		(b)	Varying	Constant	Varying	Constant
		(c)	Constant	Constant	Varying	Step Change (Rload)
CASE II	Reactive power support from three-phase capacitor bank	**(a)**	Constant	Varying	Varying	Constant
		(b)	Step change	Constant	Varying	Constant
		(c)	Constant	Constant	Varying	Step Change (R-L load)
CASE III	Real and reactive power support (for load alone) from DSTATCOM & Reactive power support from three-phase capacitor-bank		Constant	Constant	Varying	Step Change (R / R-L loads)
CASE IV	Wind speed is below cut-in speed		Not connected in the system	Varying	Varying	Step Change

The load sharing by WRIG, DSTATCOM, PV-battery system and diesel generator (SCIG) are demonstrated through simulation results. The sampling time of the simulation solver is set as 5 μs, which is realistic, and possible in a real-time hardware controller.

CASE I: WRIG – PV – BATTERY – DIESEL GENERATOR SYSTEM FEEDING ISOLATED LOAD WITHOUT EXTERNAL REACTIVE POWER SUPPORT

The operation of the WRIG – PV – Battery – SCIG system feeding a 3-phase AC load without reactive power support from external sources is elucidated through simulation results.

Mode I (a) The speed of WRIG is set as 1300 rpm, and SCIG is made to operate at speeds greater than the synchronous speed (1500 rpm) of the machine. As a grid-connected SCIG can operate as a generator with restricted slip range (maximum 6%), the maximum possible speed of operation of SCIG is 1590 rpm. Hence, speed of SCIG is varied within the range 1500 – 1590 rpm. The solar irradiation level is varied continuously, between 300 and 1000 W/m^2. The load connected in the system is 2 kW, UPF. The set values of speed and irradiation at different instants of time are shown in Fig. 6.10.

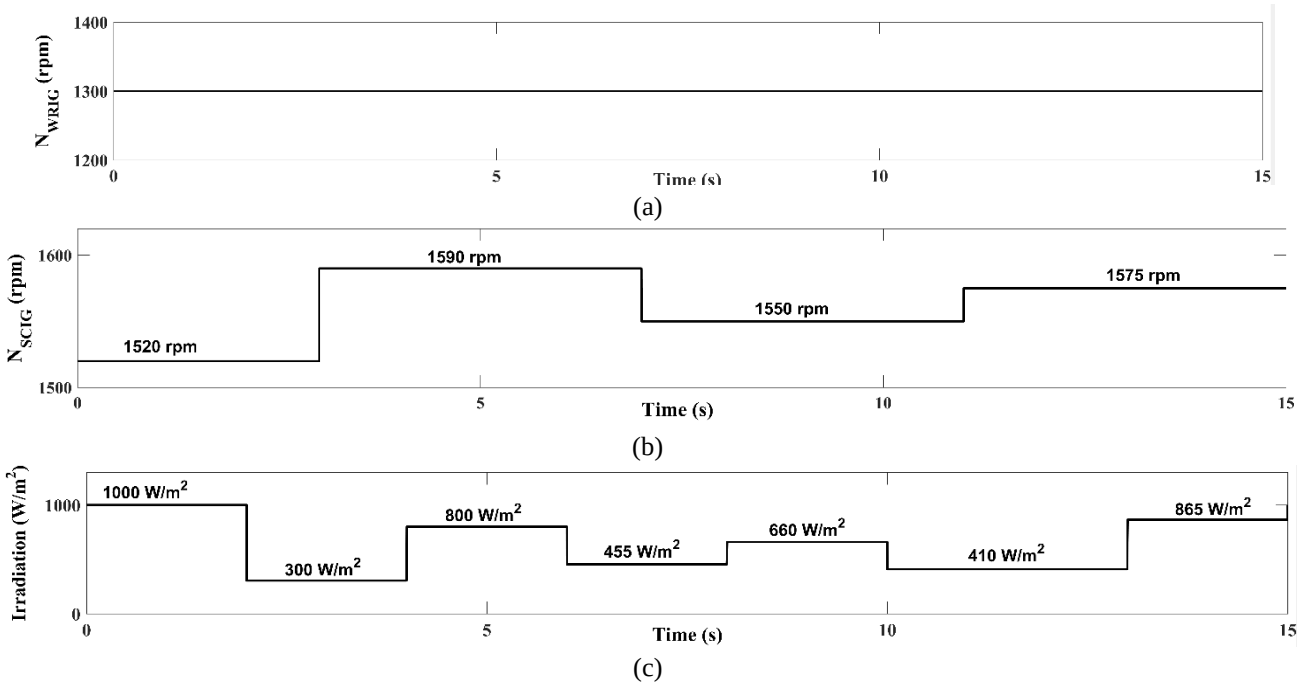


Fig. 6.10 Setpoints of the system (a) WRIG speed (b) SCIG speed (c) Irradiation level

A simple Perturb and Observe algorithm for tracking the maximum power of PV array has been programmed with initial value of duty cycle as 0.3, and the incremental change in the duty cycle, $\Delta\delta$ equal to 0.005. From Fig. 6.11 (a), it can be seen that the DC-DC converter is operated with the duty cycle computed by the PV-MPPT algorithm corresponding to maximum power of PV array for different irradiations as in Fig. 6.2. For a given duty cycle, the output voltage of PV array, V_{PV} will

be fixed as the battery terminal voltage, V_{BATT}, is fixed. This is evident from Fig. 6.11 (b). However, the change in irradiation is reflected in the PV array current, I_{PV}, shown in Fig. 6.11 (c). The magnitude of I_{PV} is in close relation with the peak current of the array for a given irradiation. The corresponding output current of DC-DC boost converter I_{BOOST}, and power of PV array, P_{PV} are shown in Figs. 6.11 (d) and (e). It is to be noted that output power of DC-DC converter is same as P_{PV}, as the elements used in the simulation are assumed to be ideal devices. The power supplied by PV array is to be utilised for charging the battery bank when in excess of the requirement of the WRIG rotor power. The waveforms of the WRIG rotor circuit are shown later in the text. Positive sign convention is followed for current flowing out of the PV array for all cases through I to IV.

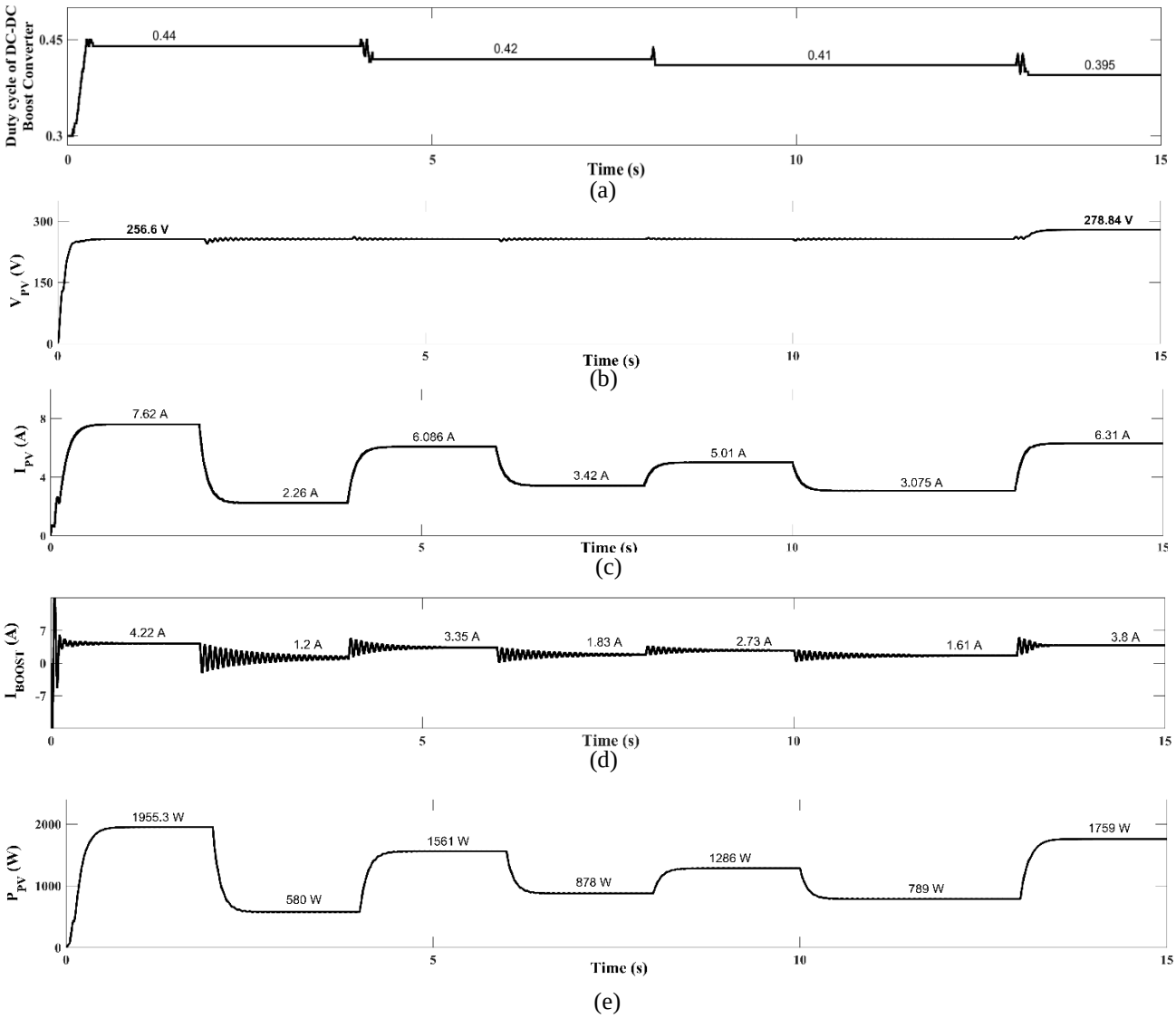


Fig. 6.11 Waveforms of PV-Boost converter system for different irradiation levels (a) Duty cycle of DC-DC converter (b) PV array terminal voltage (c) PV array terminal current (d) Terminal current of DC-DC boost converter (e) Power output of PV array.

The battery bank forms the stiff DC link of the rotor side SPWM inverter. It is assumed that the initial SOC of the battery is 92%, which leads to a voltage of 445 V, as shown in Fig. 6.12 (a). There

is a gradual infinitesimally small increase in battery voltage during the time intervals 0 to 2s, 4 to 6s, 8 to 10s and 13 to 15s, owing to the charging of the bank with substantial magnitude of battery current I_{BATT}, as shown in Fig. 6.12 (b). In the time intervals 2 to 4s, 7 to 9 s and 10 to 13 s, V_{BATT} is almost flat. This scenario is possible when P_{PV} is just sufficient to meet rotor power demand alone or when the magnitude of charging current is fractional. The corresponding power absorbed by the battery P_{BATT} can be seen in Fig. 6.12 (c). It is to be noted that the polarity of I_{BATT} is taken as positive for charging condition.

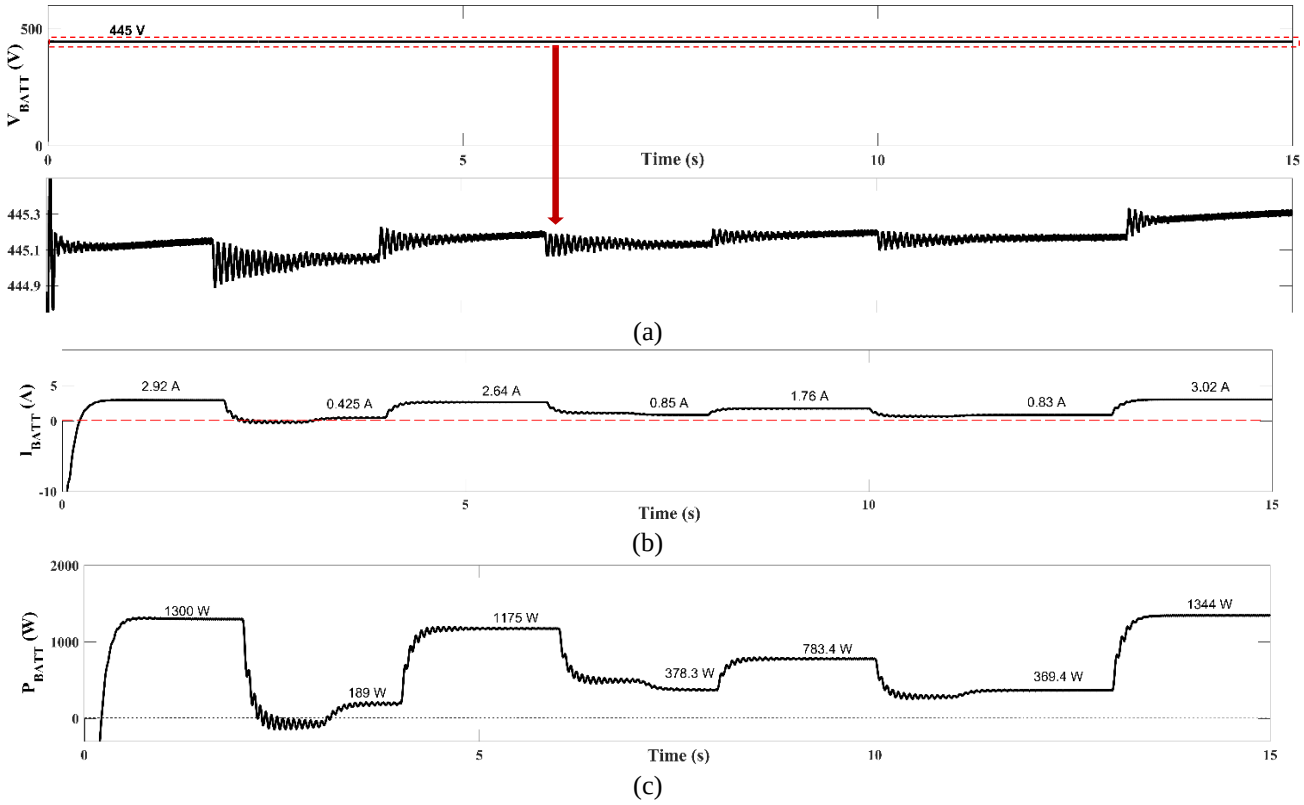


Fig. 6.12 Waveforms of battery bank for different irradiation levels and rotor power demand (a) Battery terminal voltage (b) Battery terminal current (c) Power absorbed by battery bank

From Fig. 6.12 (c), it can be seen that the battery aids the PV array to meet rotor power demand for very low irradiation values.

The efficient working of the WRIG controller is demonstrated through the results presented below. For varying SCIG speeds and a fixed load, the WRIG controller must act to maintain the AC microgrid voltage at constant magnitude of 415 V. A simple PI controller has been used for the same. The range of values of the PI controller parameters have been provided in the design document. These values have been obtained through manual tuning.

It is well-known that the power output of a grid-connected SCIG is constant for a given running speed N_{SCIG}. While this can be a potential advantage in the operation of a microgrid, the major

drawback is that it also draws a large amount of reactive power from the grid for its operation, i.e., from the WRIG in this case as there are no other active AC 3-phase sources in the system. Hence, the challenge in this case is that the WRIG must supply the fraction of load as well as the reactive power requirement of the SCIG Q_{SCIG}, even at low values of N_{WRIG}. The second challenge lies with the increase in N_{SCIG}. As the N_{SCIG} increases, the power output of SCIG, P_{SCIG} also increases, as slip of the machine increases in the negative direction. When P_{SCIG} increases, the magnitude of the microgrid voltage, V_{WRIG_ST} will also increase. The reverse happens when N_{SCIG} decreases. The controller should be capable of maintaining the magnitude of V_{WRIG_ST} irrespective of this variation in N_{SCIG} and the magnitude of P_{LOAD}. The efficient operation of the controller considering all the above factors for a P_{LOAD} of 2 kW UPF, N_{WRIG} of 1300 rpm and varying N_{SCIG} can be seen in Fig. 6.13. The magnitude of V_{WRIG_ST} is maintained as 415 V.

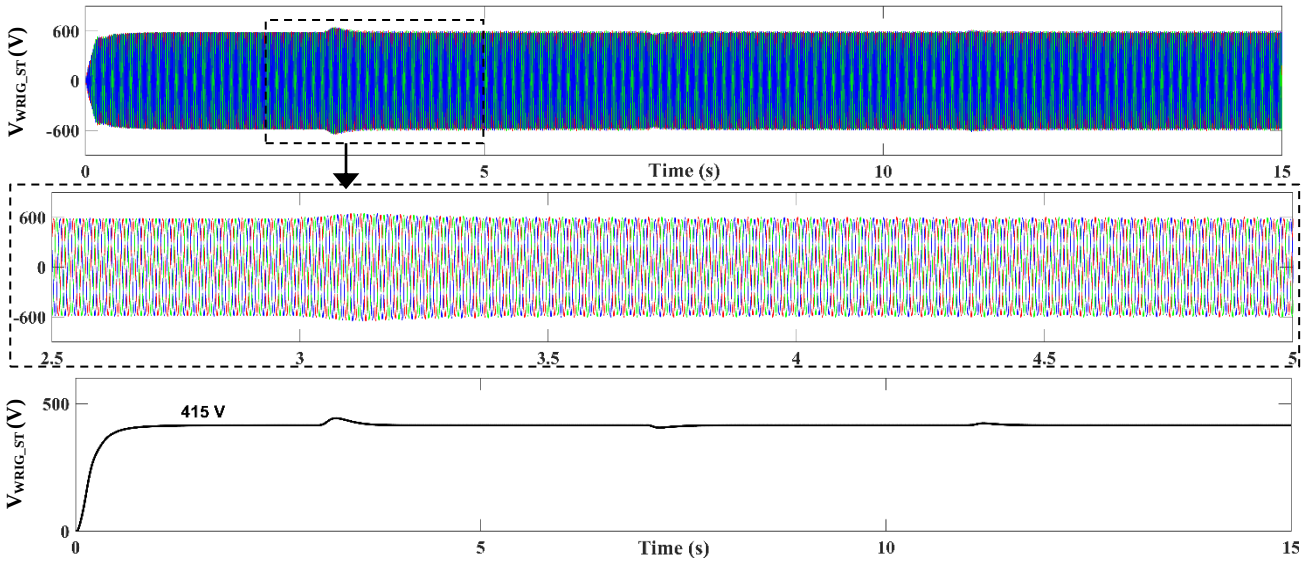


Fig. 6.13 Waveform of WRIG stator terminal voltage

The corresponding rotor-inverter waveforms are provided in Fig. 6.14 Figs. 6.14 (a) and (b) show the rotor-circuit voltage $V_{WRIG\ ROTOR}$ and current I_{WRIG_ROTOR} respectively, at a frequency equal to the slip frequency, 6.66 Hz. It can be inferred from Fig.6.14 (c) that real power injected in the rotor, $P_{WRIG\ ROTOR}$ is inversely proportional to N_{SCIG}, i.e., when N_{SCIG} is low, $P_{WRIG\ ROTOR}$ increases, and vice-versa. The reactive power injected in the rotor, $Q_{WRIG\ ROTOR}$ varies in proportion with N_{SCIG} as in Fig. 6.14 (d). As N_{SCIG} increases, Q_{SCIG} absorbed by the SCIG also increases. For the WRIG to meet this demand also, the reactive power injected in rotor increases. The modulation index (MI) of the rotor-inverter in Fig. 6.14 (e) conforms to the variation in $P_{WRIG\ ROTOR}$ alone. The resulting current drawn from the DC link, $I_{ROTOR\ INV}$ is shown in Fig. 6.14 (f). It can be verified that the DC currents I_{BOOST}, I_{BATT} and $I_{ROTOR\ INV}$ satisfy Kirchoff's Current Law.

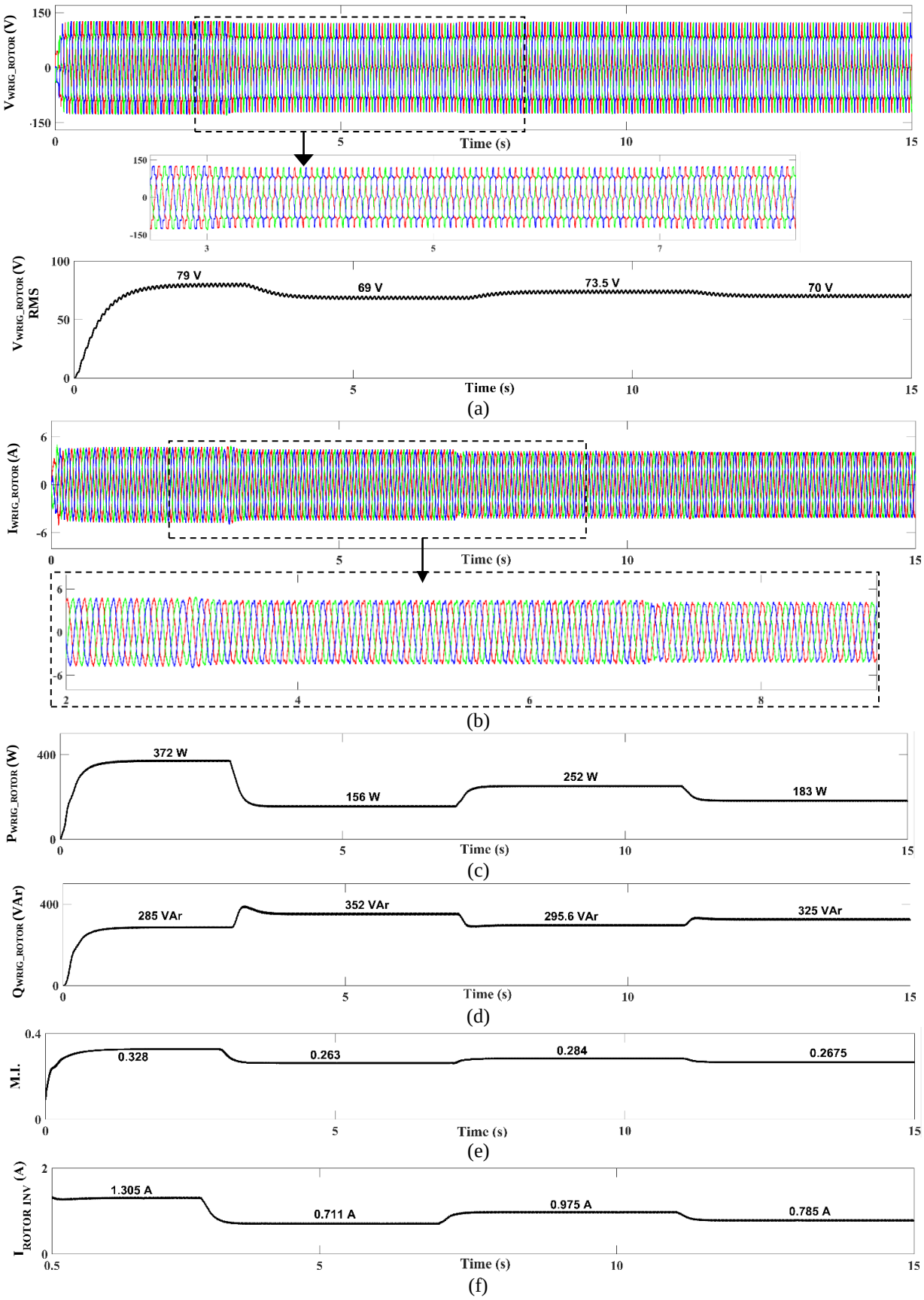


Fig. 6.14 Waveforms at WRIG Rotor terminal (a) Voltage (b) Current (c) Real power injected (d) Reactive power injected (e) Modulation index of rotor-inverter (f) Current in DC link of rotor inverter.

So far, the operation of WRIG controller has been demonstrated through the working mechanisms in the rotor circuit alone. The resulting effects in the stator side of the WRIG, i.e., the AC microgrid are studied and presented. The terminal voltage of SCIG and load will be the same as that of the WRIG. Hence, to show the sharing of power by the two induction machines, only the current waveforms are shown along with the load current waveform in Fig 6.15.

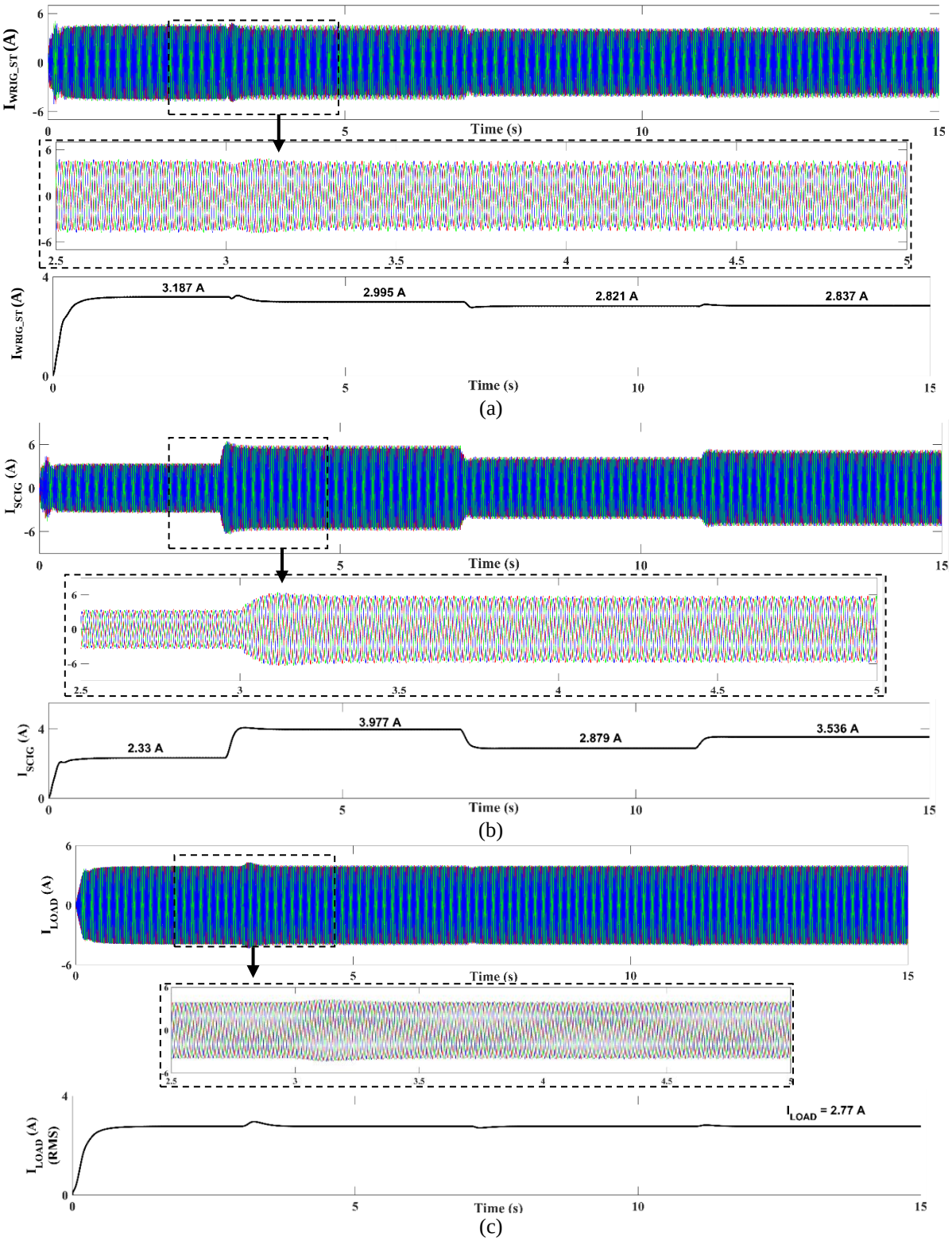


Fig. 6.15 Three-phase current waveforms (a) WRIG Stator terminal (b) SCIG terminal (c) Load terminal

It can be seen that when N_{SCIG} increases from 1520 rpm to 1590 rpm at time t=3s, there is an increase in SCIG terminal current, I_{SCIG}. During this interval, WRIG stator terminal current I_{WRIG_ST} decreases to balance the load requirement. This change in real power supplied by WRIG is reflected in the rotor inverter MI, as mentioned earlier. On the contrary, when N_{SCIG} decreases from 1590 rpm to 1550 rpm at time t=7s, I_{SCIG} also decreases, which leads to an increase in I_{WRIG_ST} to balance load requirement.

The power supplied/absorbed by the WRIG and SCIG and power absorbed by the load are shown in Fig 6.16. It is clearly seen from Figs. 6.16 (a) and (b) that with increased speed of operation, the SCIG delivers more power to the load (Fig. 6.16 (c)), thereby reducing the real power delivered by the WRIG. Also, the reactive power needed for SCIG to operate is supplied by the WRIG, i.e., $Q_{SCIG} = Q_{WRIG}$. It can be seen that the WRIG is capable of generating real and reactive power independently.

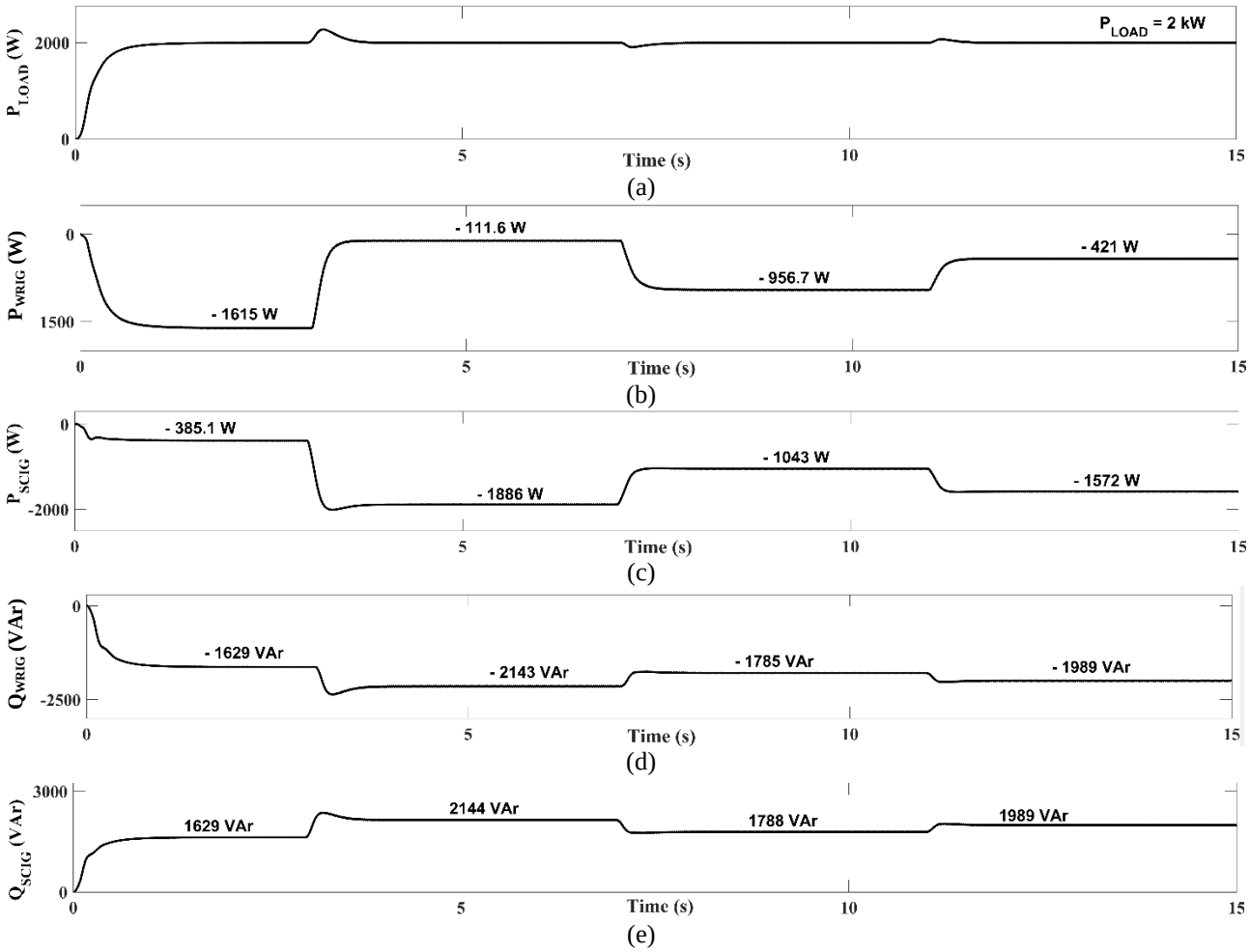


Fig. 6.16 (a) P_{LOAD} (b) P_{WRIG} (c) P_{SCIG} (d) Q_{WRIG} (e) Q_{SCIG}

It can be inferred that change in irradiation level does not have any effect on the three-phase AC microgrid terminal voltage, and hence the power sharing by the WRIG and SCIG. Although the PV-Battery system forms the DC link of the

WRIG rotor-inverter, henceforth, for the sake of brevity, the DC side waveforms are not presented. It is to be noted that the PV-battery system is present in all modes of operation that follow.

Mode I (b) Constant SCIG speed and load, varying WRIG speed and irradiation level

In this mode, WRIG is operated at different speeds, while the SCIG speed is maintained constant at 1575 rpm. The PV irradiation level is maintained same as earlier in Case (i). The system set-points are shown in Fig. 6.17. The load connected in the system is 3 kW.

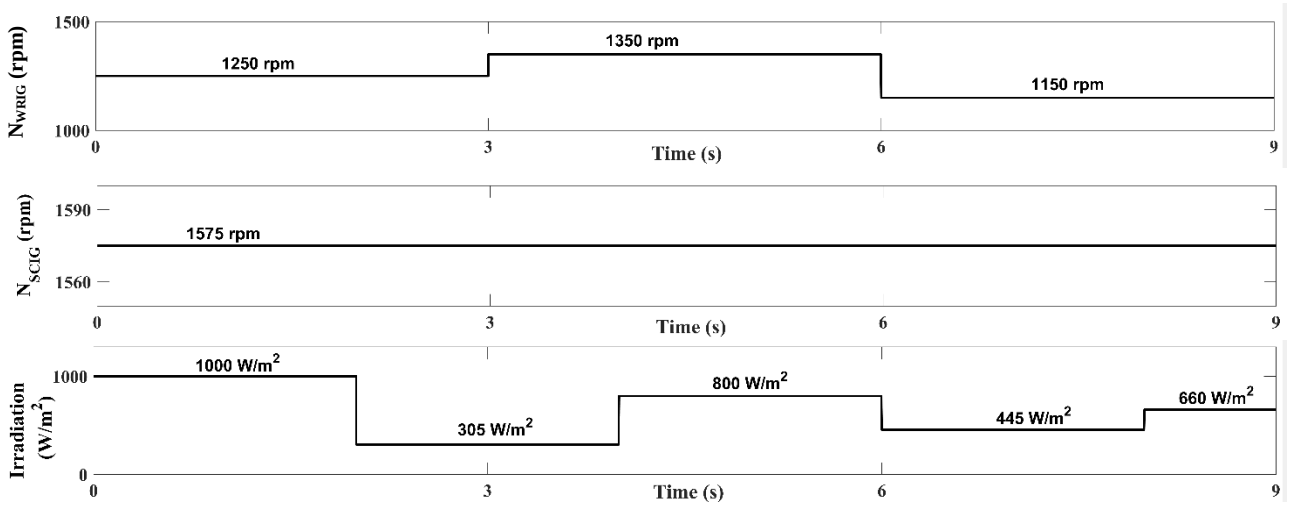


Fig. 6.17. Setpoints for Case I (b)

Fig. 6.18 shows the injected voltage and current in the rotor circuit of the WRIG. It can be seen that the frequency of the rotor circuit waveforms varies with the speed of the machine, and is equal to the corresponding slip frequency. The magnitude of the rotor voltage varies with the modulation index (MI) generated by the WRIG controller, shown in Fig. 6.19. The corresponding stator terminal voltage is shown in Fig. 6.20. The magnitude of the WRIG stator voltage is maintained at 415 V for different running speeds, and its frequency is maintained as 50 Hz by injected voltage in the rotor circuit at slip frequency.

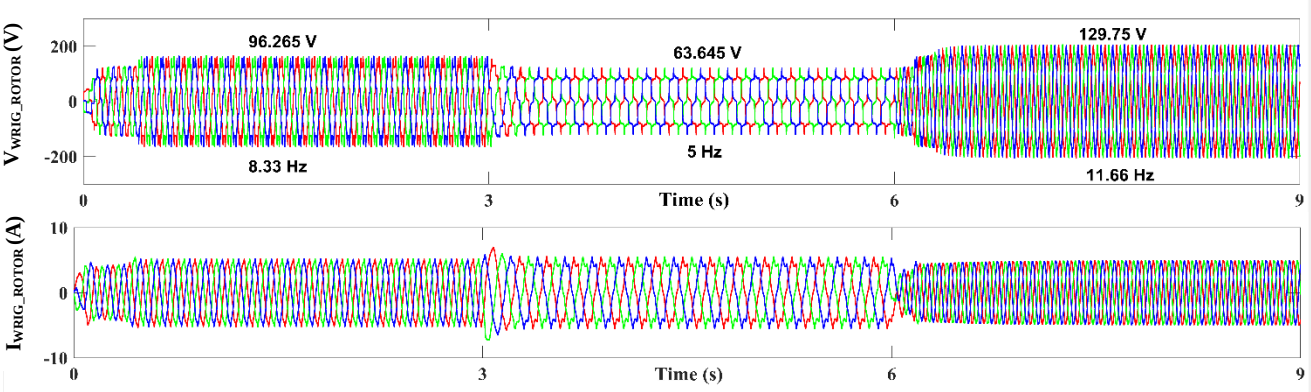


Fig. 6.18 Three phase waveforms of WRIG Rotor voltage and current

Fig. 6.19 Modulation index of rotor-side inverter

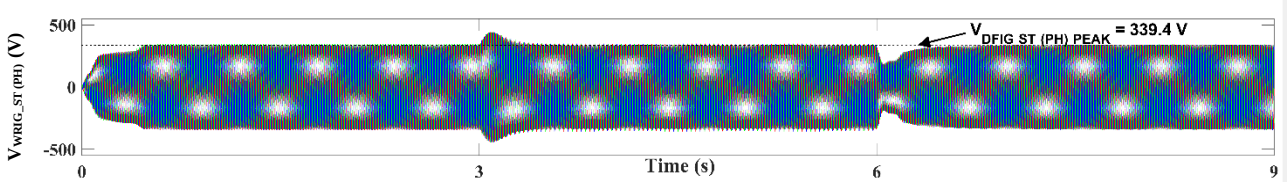


Fig. 6.20 WRIG Stator terminal voltage

The power sharing by the SCIG and WRIG is shown in Figs. 6.21 and 6.22 for feeding the connected 3 kW load.

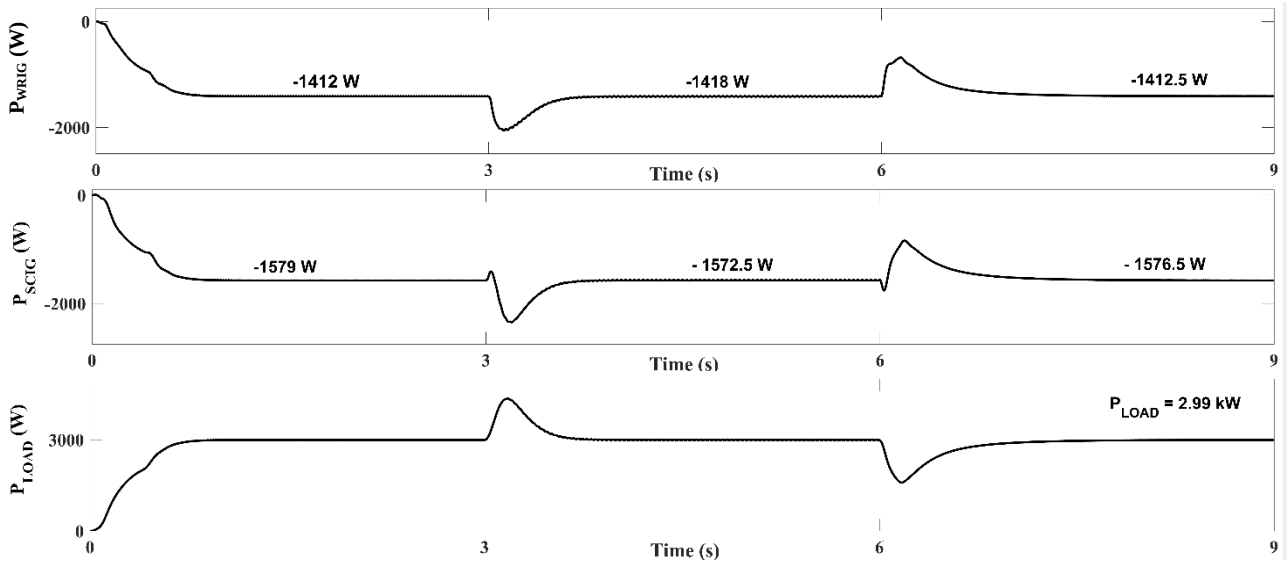


Fig. 6.21 Real power sharing by WRIG and SCIG

The WRIG delivers the reactive power required by the SCIG for its operation.

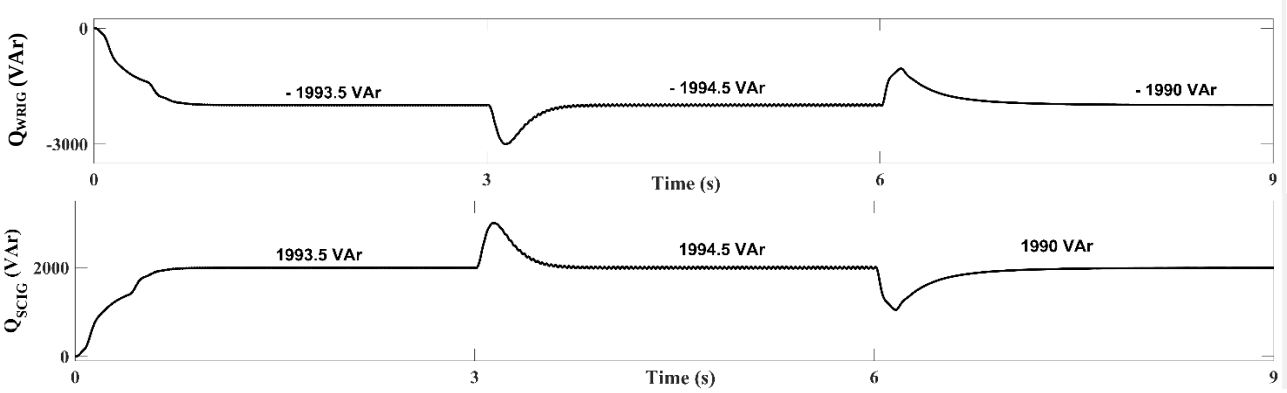


Fig. 6.22 Reactive power balance in the AC microgrid

Mode I (c) Step change in load

To demonstrate the effective operation of the system for sudden change in load, the WRIG speed, N_{WRIG} is set as 1300 rpm, SCIG speed N_{SCIG} is 1560 rpm, and the irradiation level is changed continuously. The different set-points are shown in Fig. 6.23. The load is changed from 3 kW to 1.5 kW at time t=3 s.

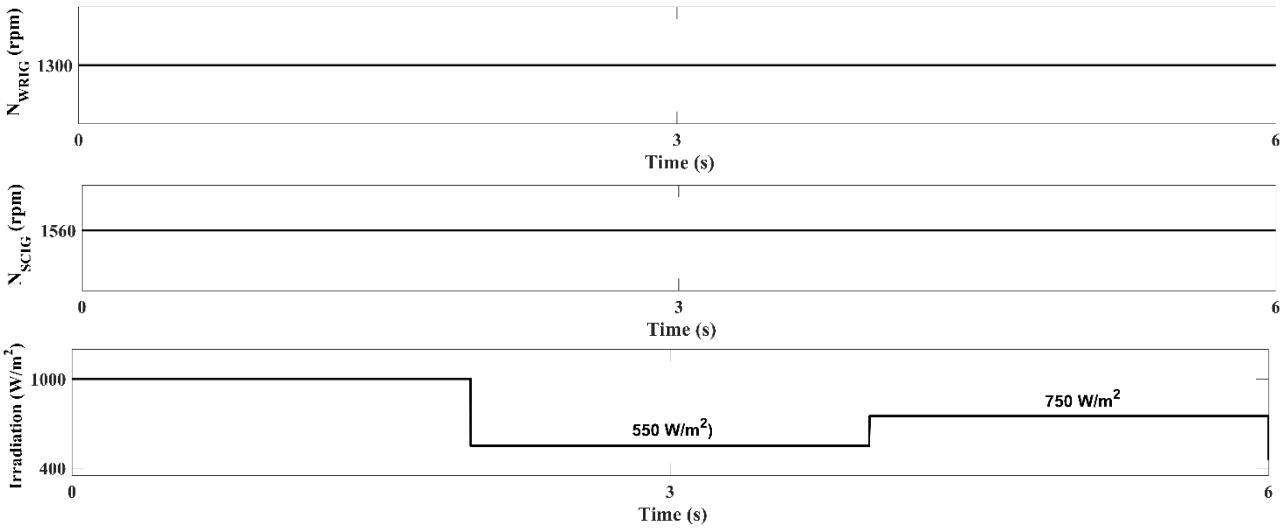


Fig. 6.23 Setpoints of system for Case I (c)

For a step change in load, it can be seen from Fig. 6.24 that the WRIG stator terminal voltage is maintained as 415 V. As the SCIG output power is uncontrolled, it will deliver a fixed power corresponding to the running speed. So, the power generated from WRIG will vary to meet load demand. This can be seen in Fig. 6.25. The magnitude of rotor voltage and current of WRIG decreases when the load decreases from 3 kW to 1.5 kW. This can be seen in Fig. 6.26. Correspondingly, the WRIG rotor real and reactive power also decreases. This has been shown in Fig. 6.27. It can be seen that the change in real power demand at stator side reflects in P_{WRIG_ROTOR}. However, as the reactive power demand at stator side is the same, the change in rotor reactive power is small. For a fixed SCIG speed, the reactive power demanded by SCIG is met by the WRIG, as in Fig. 6.28.

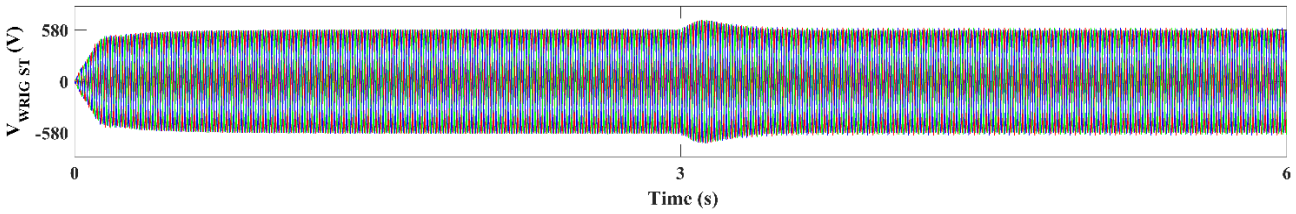


Fig. 6.24 WRIG Stator terminal voltage

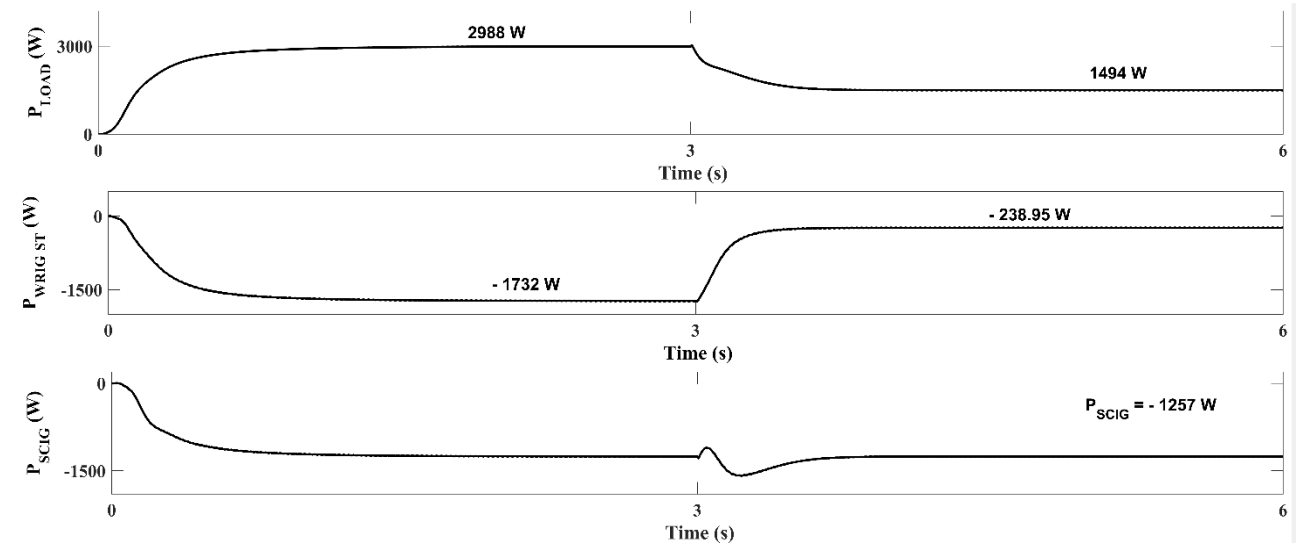


Fig. 6.25 Real power sharing by WRIG and SCIG

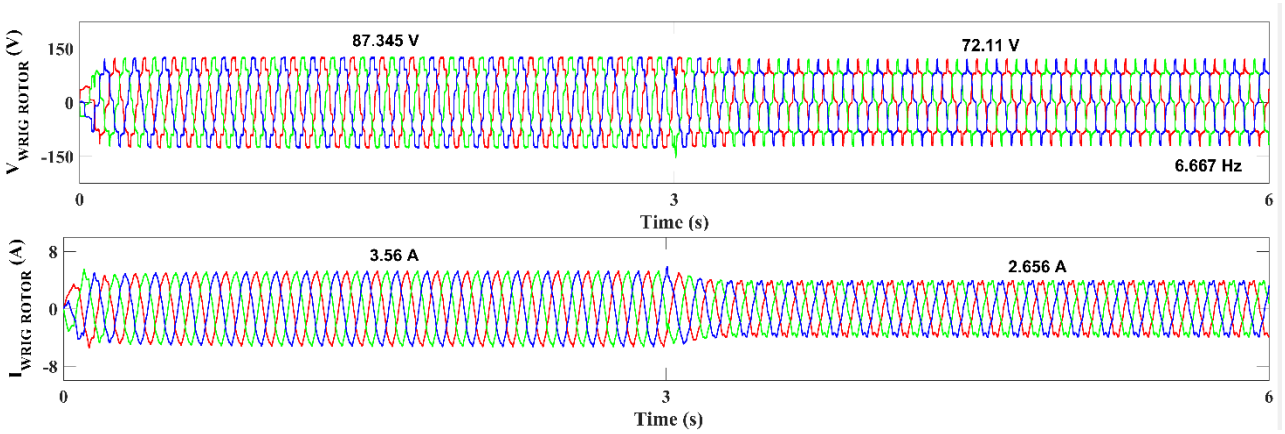


Fig. 6.26 WRIG Rotor voltage and current waveforms

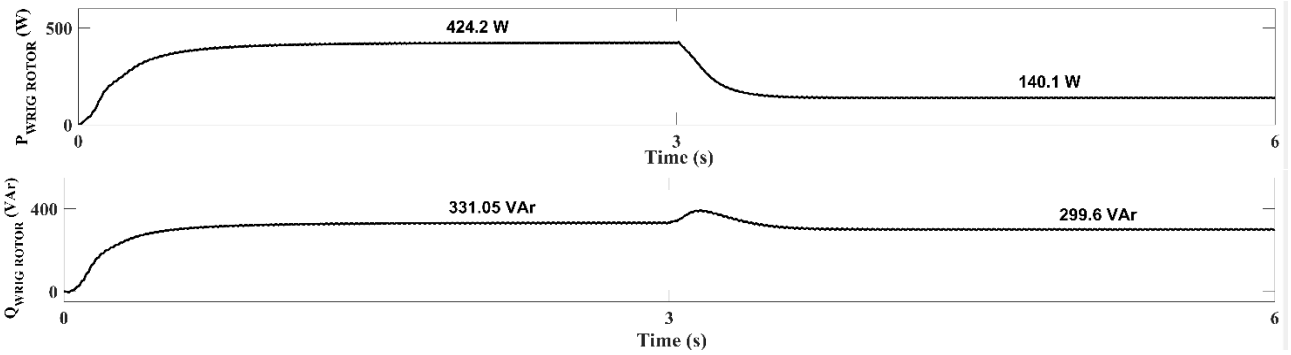


Fig. 6.27 Real and reactive power injected in WRIG rotor

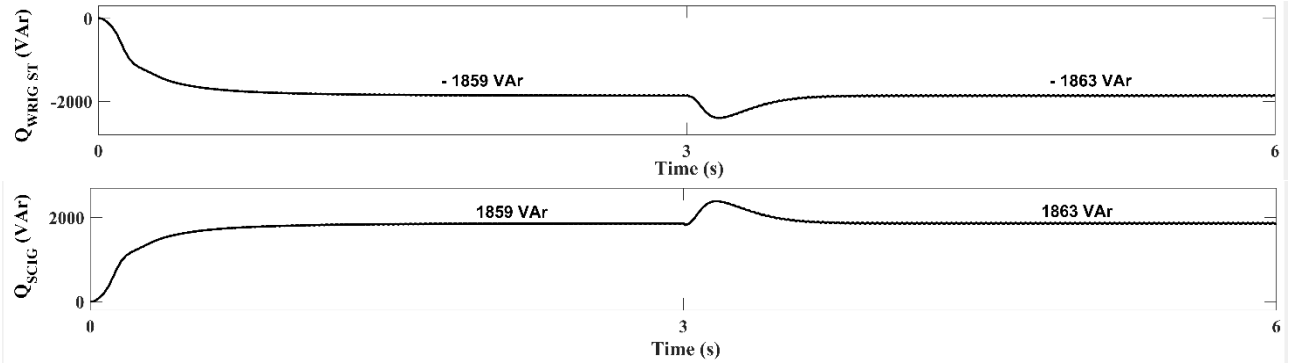


Fig. 6.28 Reactive power of SCIG and WRIG

From all the three modes of operation of the microgrid under Case I, it was observed that $Q_{SCIG} = Q_{WRIG}$. This poses a constraint on the maximum load that can be connected in the system. As the WRIG and SCIG are rated for only 3 kVA each, the actual total real power delivered should be 4.5 kW, and 3.96 kVAr, considering that both machines deliver rated reactive power. However, the generation of reactive power to feed an R-L load is not possible, as Q_{SCIG} absorbed is almost near to rated Q capacity of the WRIG, 1.98 kVAr. Hence, it is suggested to employ an external reactive power source, such as a capacitor bank, that will meet out the Q_{SCIG} demand alone. In that case, the load connected in the microgrid can be increased. The simulation of the proposed microgrid system with capacitor bank connected at the point of common coupling is carried out and results are presented in the following section as Case II.

CASE II: WRIG – PV – BATTERY – DIESEL GENERATOR SYSTEM FEEDING ISOLATED LOAD WITH REACTIVE POWER SUPPORT FROM THREE-PHASE CAPACITOR BANK

Mode II (a) N_{WRIG} is set as 1300 rpm, and the load connected in the system is an R-L load of rating 3 kW, 0.8 p.f (lag). N_{SCIG} is varied from 1520 to 1590 rpm. Irradiation level is changed continuously. The setpoints of the system for this mode are shown in Fig. 6.29.

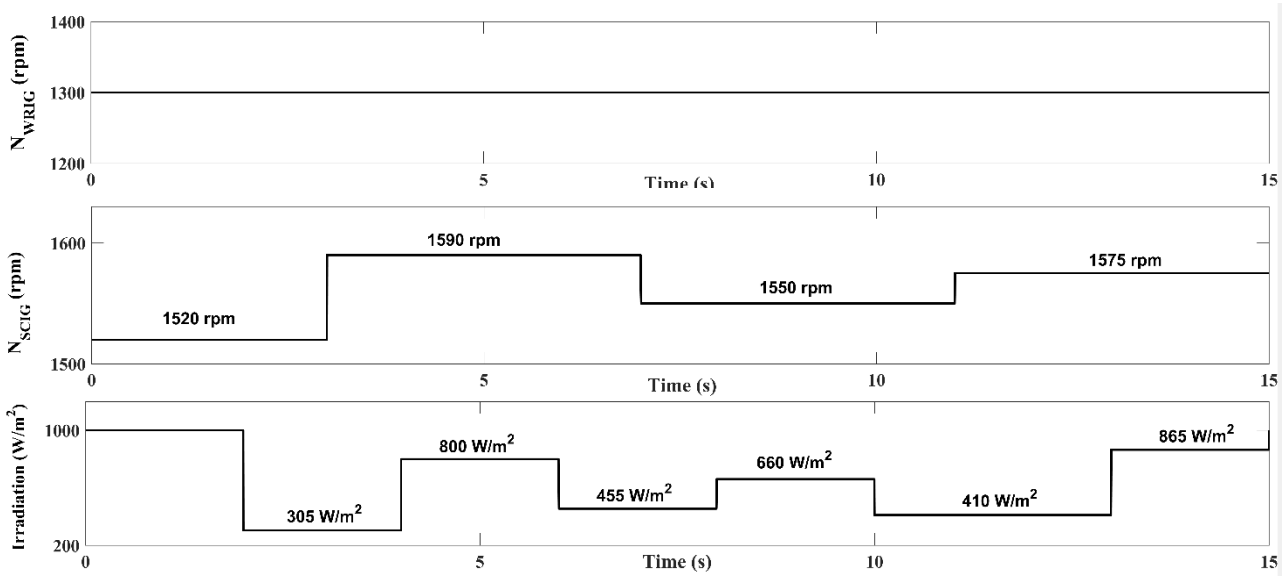


Fig. 6.29 Setpoints for Case II (a)

It can be seen from Fig. 6.30 that the microgrid voltage is maintained as 415 V, irrespective of change in N_{SCIG}.

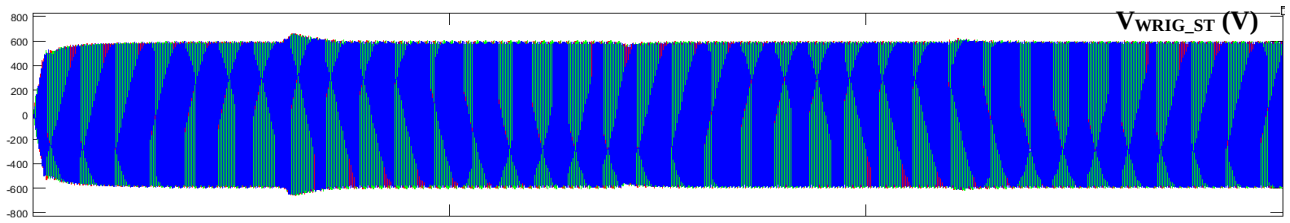
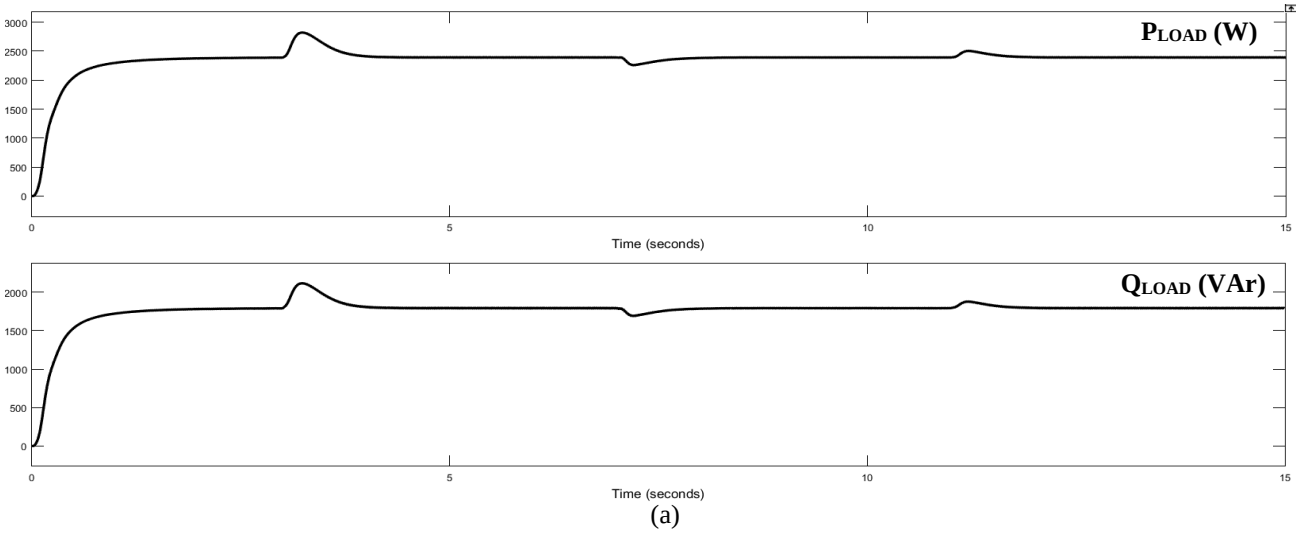
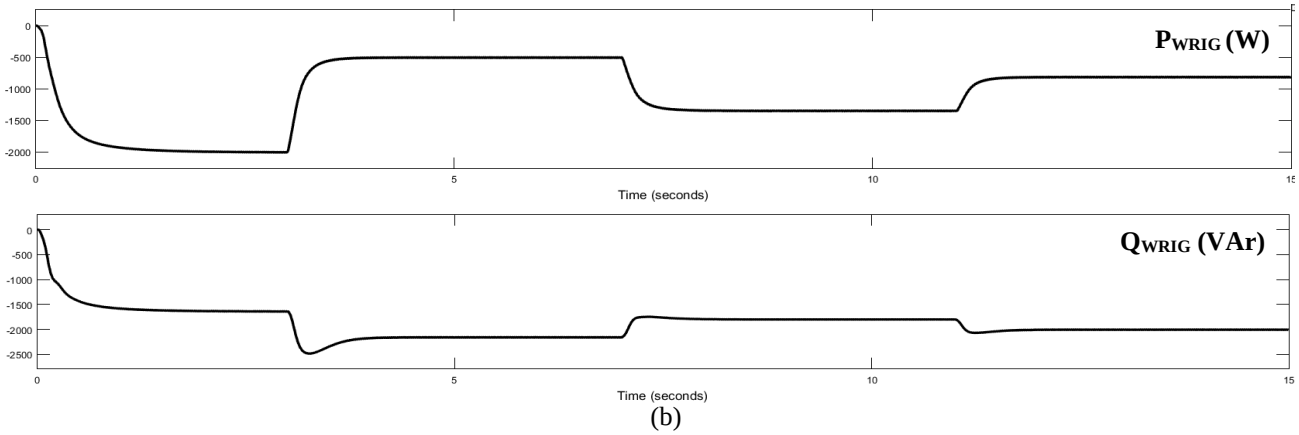


Fig. 6.30 WRIG terminal voltage

The real/reactive power sharing by WRIG, SCIG and 3 – phase capacitance bank is shown in Fig. 6.31. It can be seen that SCIG and WRIG supply P_{LOAD} = 2400 kW, while the reactive power demand of load Q_{LOAD} = 1800 VAr is met by the WRIG. In this mode, $Q_{SCIG} = Q_{CAP}$. It is to be noted that the Q_{SCIG} varies proportionally with N_{SCIG}. When Q_{SCIG} exceeds Q_{CAP}, the reactive power shortage is met out by the WRIG. It is to be noted that the real/reactive power balance is maintained for all operating points.



(a)



(b)

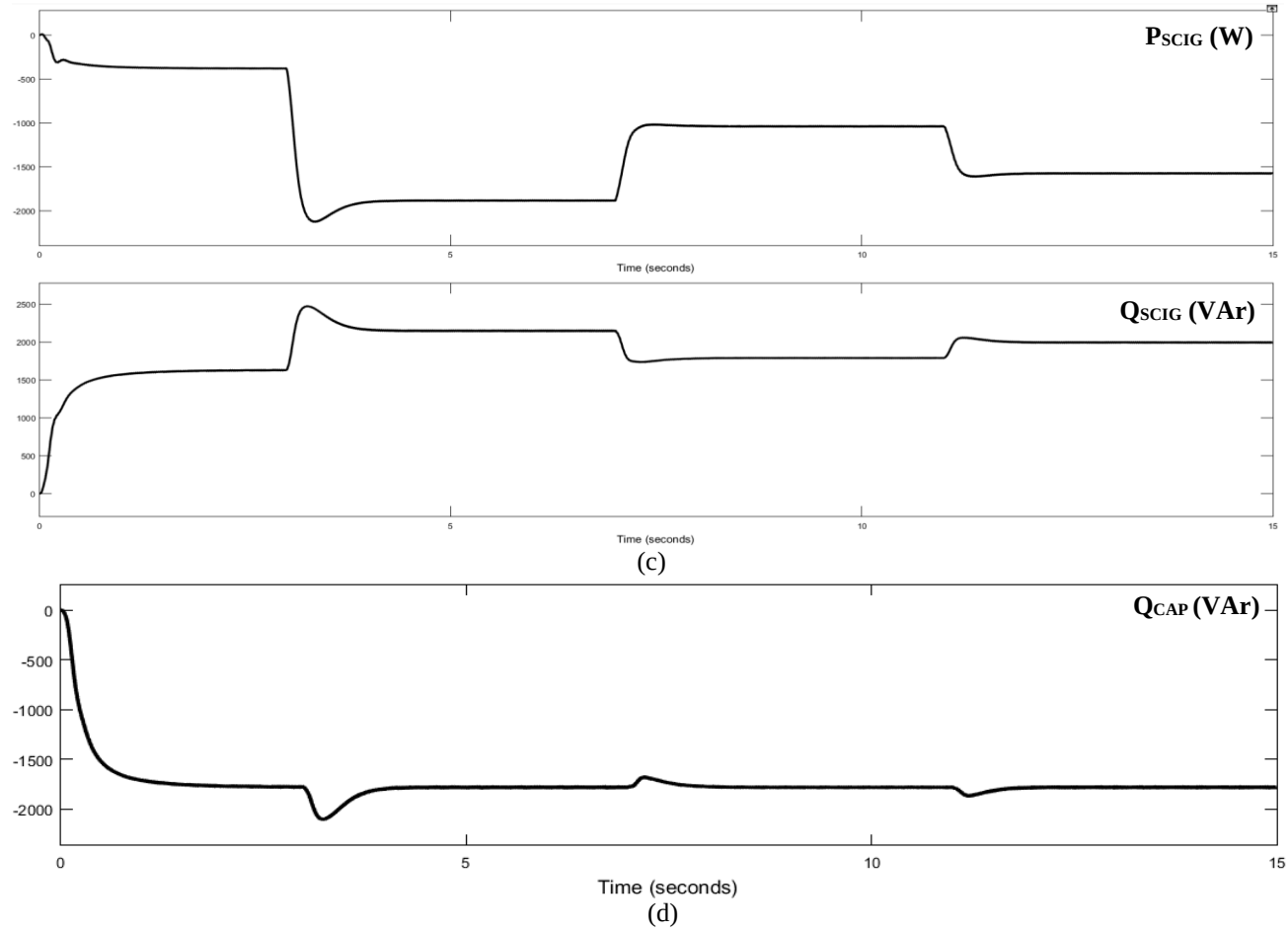


Fig. 6.31 Real/Reactive power at different terminals (a) Load (b) WRIG (c) SCIG (d) Capacitor bank

The corresponding rotor real and reactive power waveforms are shown in Fig. 6.32.

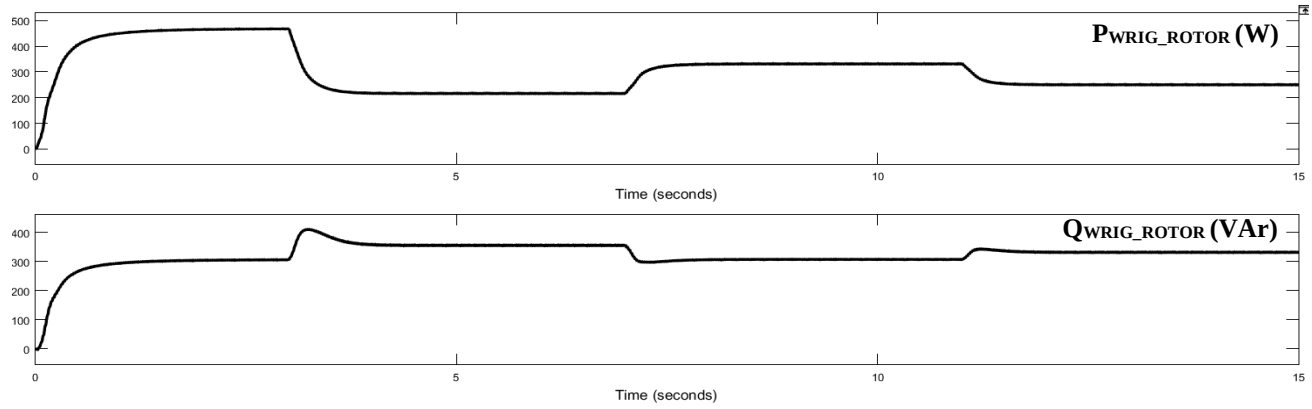


Fig. 6.32 Real/Reactive power injected in WRIG Rotor circuit

Mode II (b) Constant SCIG speed and load, step change in WRIG speed and varying irradiation level

In this mode, N_{WRIG} is changed from 1250 to 1350 rpm at time t=3s, while the SCIG speed is maintained constant at 1575 rpm. The PV irradiation level is maintained same as earlier in Case I(b). The load connected in the system is 3 kVA, 0.9 p.f. (lag) R-L load.

In this mode of operation also, the WRIG stator terminal voltage is maintained as 415 V, as in Fig. 6.33.

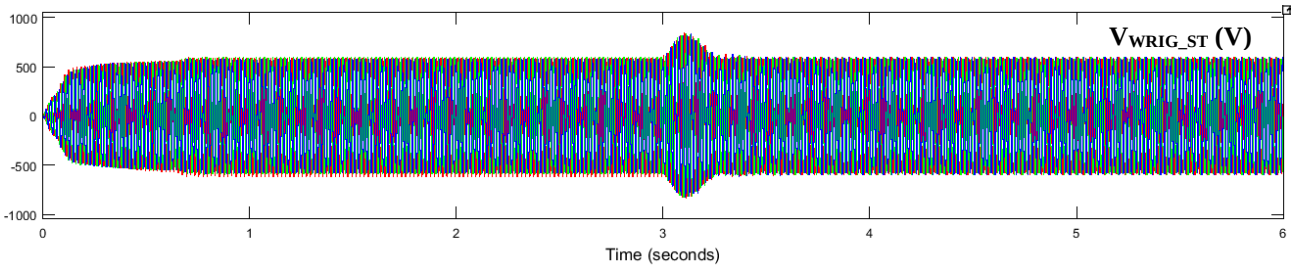
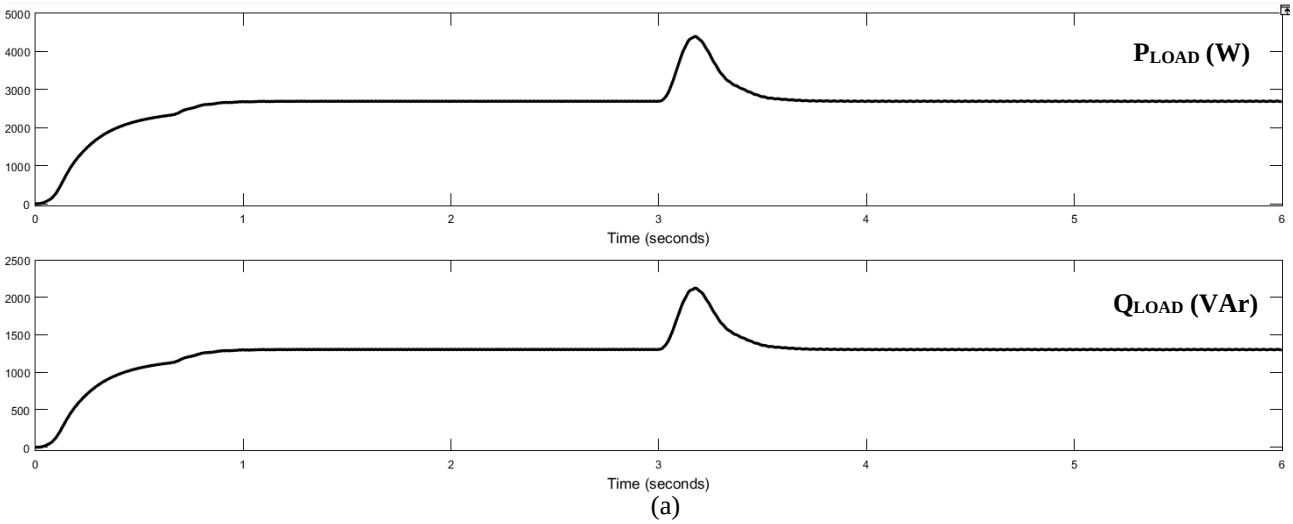


Fig. 6.33 WRIG stator terminal voltage

As the value of N_{SCIG} is constant, the power generated by SCIG will be constant, and reactive power absorbed for the operation will also be constant. With variation in N_{WRIG}, the real/reactive power balance for load in maintained by the WRIG and capacitor bank in tandem with SCIG that delivers fixed real power, and absorbs fixed reactive power. Figs. 6.34 (a) to (d) show the real/reactive power balance in the AC microgrid when N_{WRIG} is changing. The frequency of rotor variables is equal to the corresponding slip frequency, as shown in Fig. 6.35.



(a)

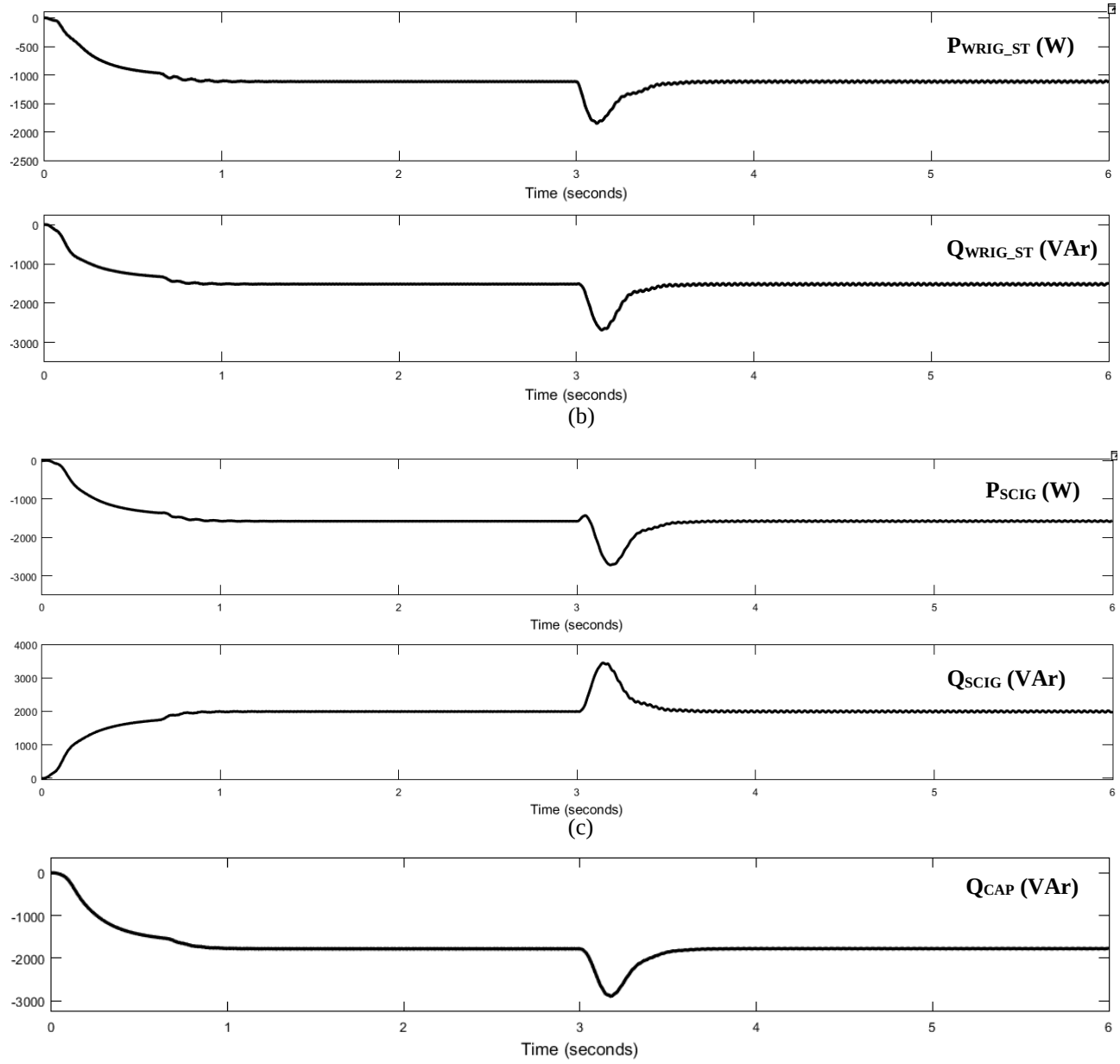


Fig. 6.34 Real/Reactive power at different terminals (a) Load (b) WRIG (c) SCIG (d) Capacitor bank

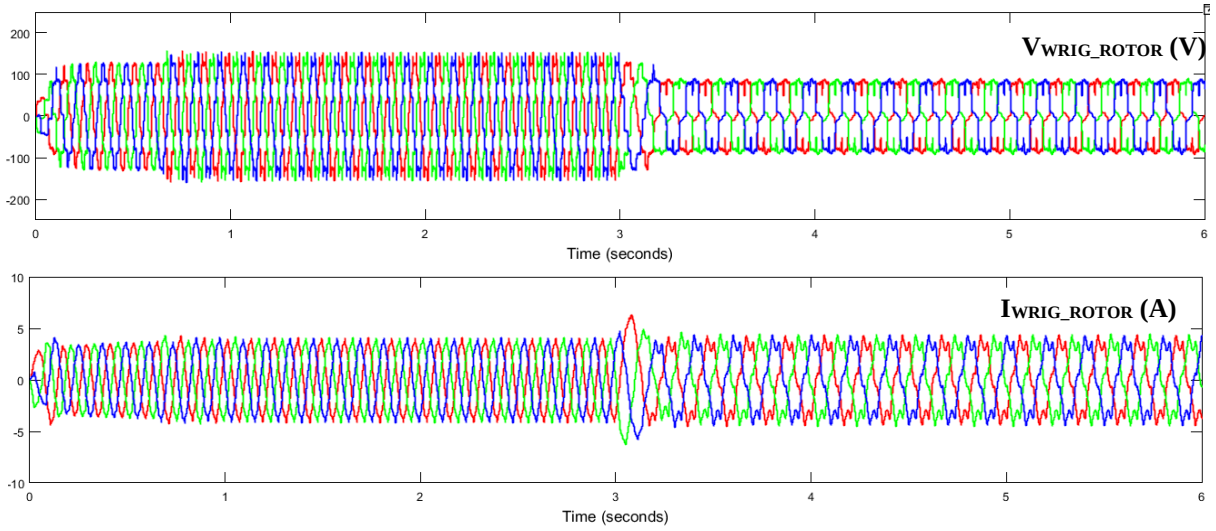


Fig. 6.35 WRIG Rotor voltage and current waveforms

Mode II (c) Step change in load

To demonstrate the effective operation of the system for sudden change in load, the WRIG speed, N_{WRIG} is set as 1300 rpm, SCIG speed N_{SCIG} is 1575 rpm, and the irradiation level is changed from 1000 W/m^2 to 900 W/m^2. However, the load connected in the AC microgrid is changed from 3 kVA, 0.9 p.f. (lag) to 4 kW at time t=3 s.

In this mode of operation also, the WRIG stator terminal voltage shown in Fig. 6.36 is maintained as 415 V.

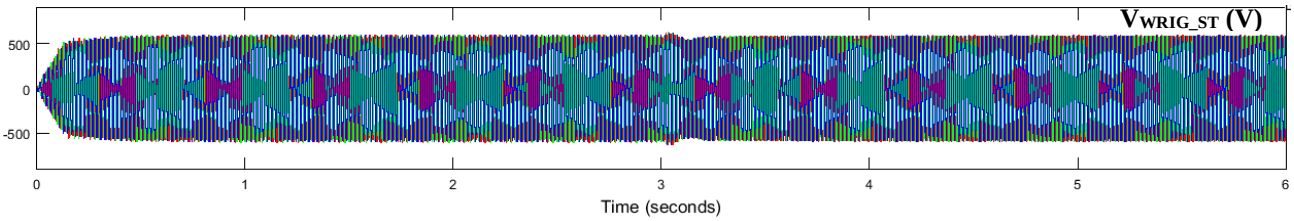
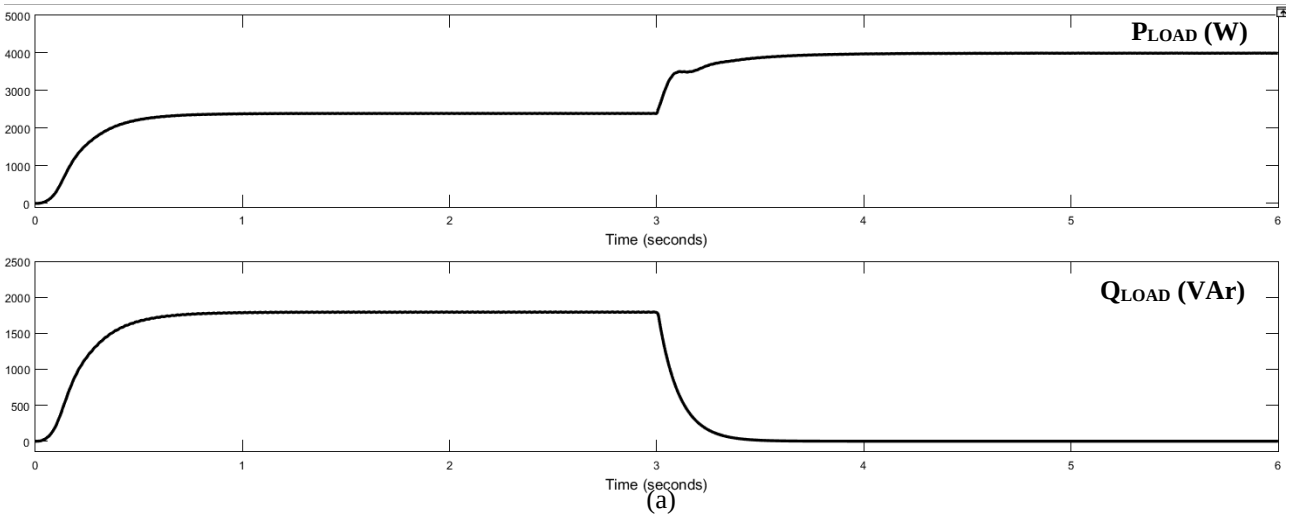


Fig. 6.36 WRIG stator terminal voltage

As the value of N_{SCIG} is constant, the power generated by SCIG will be constant, and reactive power absorbed for the operation will also be constant. With variation in load, the real/reactive power balance for load in maintained by the WRIG and capacitor bank in tandem with SCIG. Figs. 6.37 (a) to (d) show that the real/reactive power balance in the AC microgrid is maintained for step change in load. The corresponding rotor power injected is shown in Fig. 6.38.



(a)

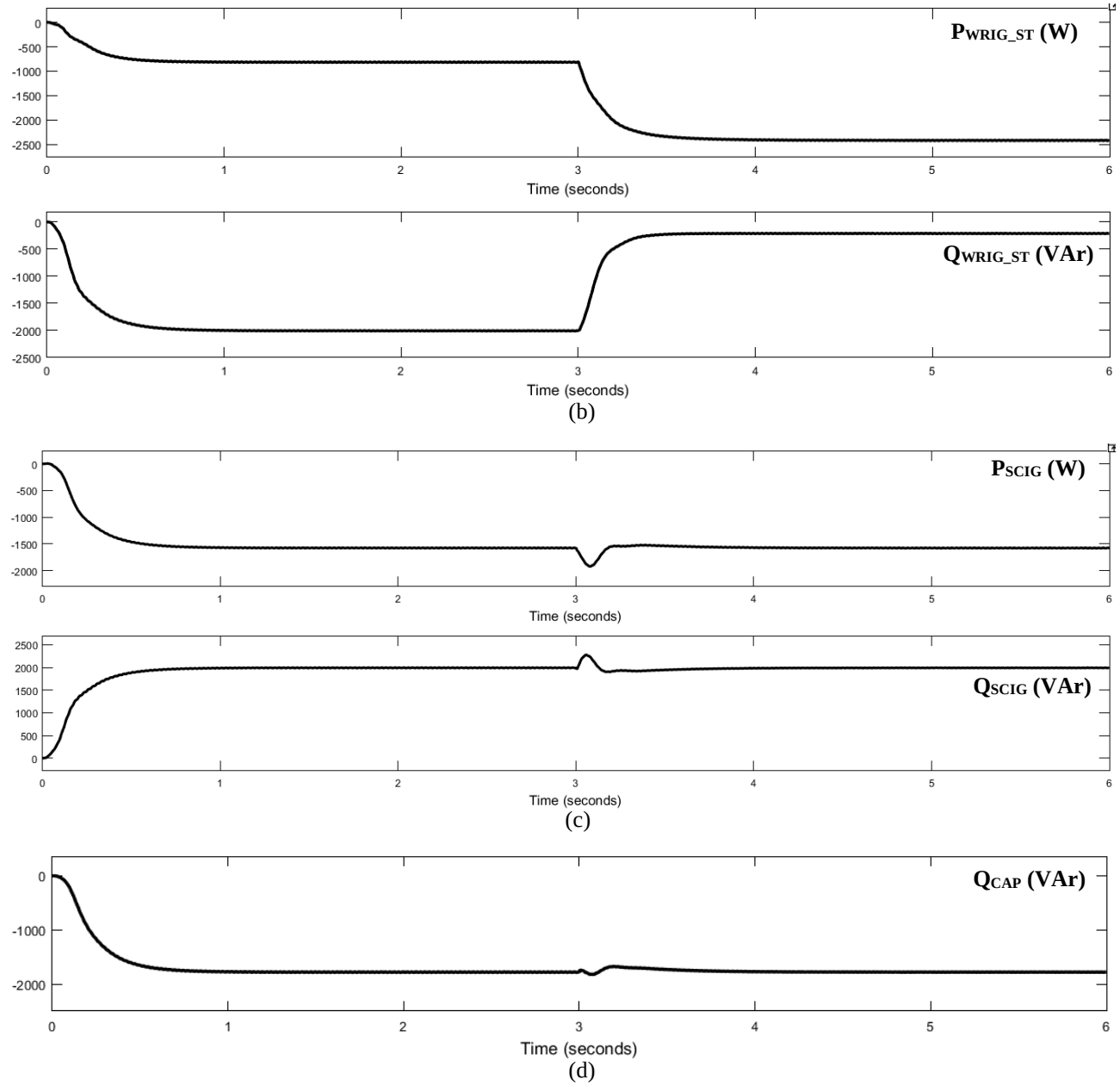


Fig.6.37 Real/Reactive power at different terminals (a) Load (b) WRIG (c) SCIG (d) Capacitor bank

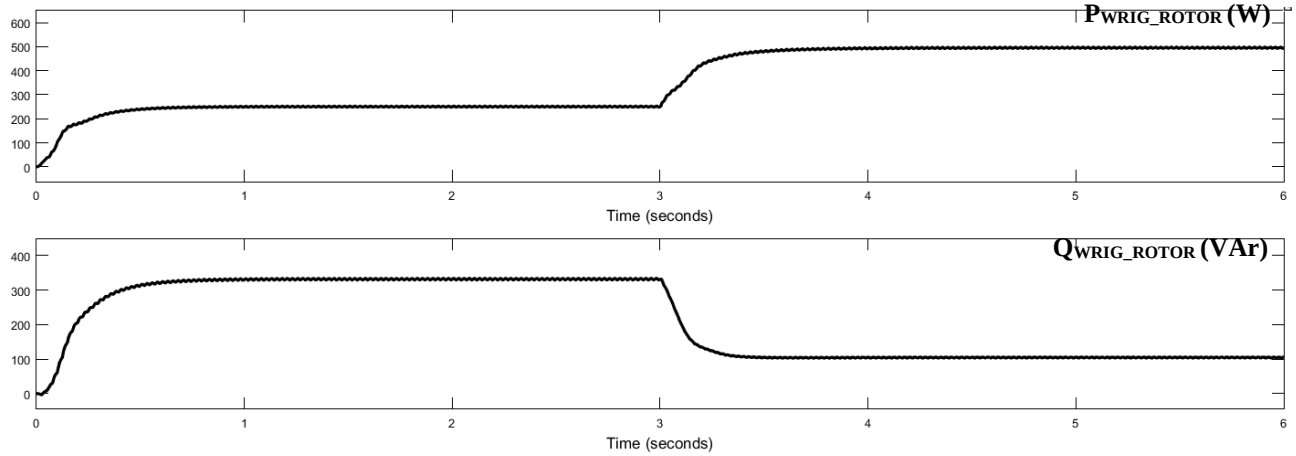


Fig. 6.38 Real/Reactive power injected in WRIG Rotor circuit

In Case I, the maximum load that could be supplied from WRIG and SCIG was limited to 3 kW, UPF. Throughout Case II, it was seen that the inclusion of the 2 kVAr delta-connected capacitor enabled operation of the system for loads greater than 3 kW, UPF as well as lagging power factor linear loads. The response of the system to change in N_{SCIG}, N_{WRIG}, Irradiation and load was tested and presented. It is observed that it is possible to expand the range of loads in the system if the reactive power of the SCIG is met by an external apparatus. In Case III, the operation of the microgrid is tested when a DSTATCOM is interfaced in the PCC to deliver a portion of the load real power requirement and complete load reactive power requirement. This is carried out to make a pathway for direct power flow from the PV-battery system to the AC microgrid.

CASE III: WRIG – PV – BATTERY – DIESEL GENERATOR SYSTEM FEEDING ISOLATED LOAD WITH REAL AND REACTIVE POWER SUPPORT (FOR LOAD ALONE) FROM DSTATCOM & REACTIVE POWER SUPPORT FROM THREE-PHASE CAPACITOR-BANK

In this mode of operation, the three-phase terminals of the D-STATCOM module is connected at the point of common coupling of the AC Microgrid. The PV-battery system forms the DC link of the WRIG rotor-inverter as well the D-STATCOM. The D-STATCOM has been operated to supply 50% of the load real power, P_{LOAD} and complete reactive power demand of load, Q_{LOAD}. The algorithm and controller for the same has been presented in detail in Chapter 4.

The speed of WRIG, N_{WRIG} is set as 1300 rpm, and N_{SCIG} is set as 1550 rpm. Irradiation level is initially equal to 1000 W/m^2. From 5s to 11 s, irradiation is considered as 800 W/m^2, thereafter it is changed to 950 W/m^2. Initially, the WRIG-PV-Battery-SCIG system is allowed to settle down before the DSTATCOM breaker shown in Fig. 6.9 is closed at time t=2.1 s. The load connected in the system is changed periodically to show the efficient power sharing by the three active sources in the microgrid. The different load settings are shown in Table 2.

Table 2 Load setting for Case III

Time, t (s)	Load present in the system
$0 < t \leq 4$	3 kW, UPF
$4 < t \leq 7$	4 kW, UPF
$7 < t \leq 10$	4 kVA, 0.8 p.f. (lag)
$10 < t \leq 13$	3 kVA, 0.8 p.f. (lag)

For successful operation of the D-STATCOM, it is essential that the WRIG stator terminal voltage behaves like a stiff three-phase grid. The WRIF controller maintains a stiff grid of magnitude 415 V, shown in Fig. 6.39 for all operating conditions. This has been achieved irrespective of multiple sources injecting power in the microgrid.

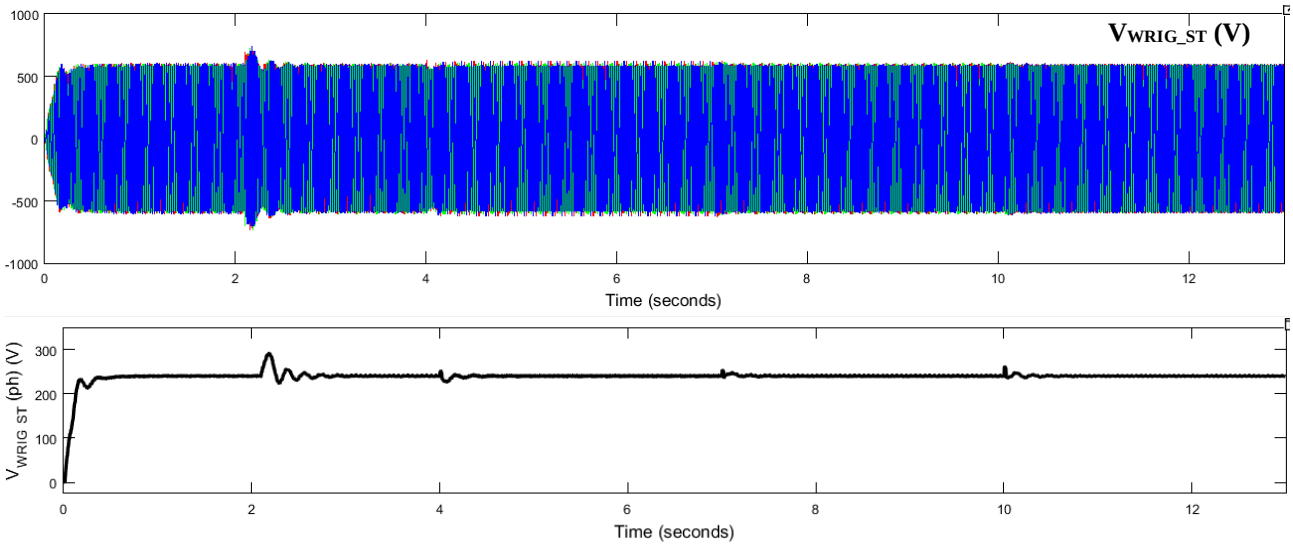


Fig. 6.39 Voltage of AC Microgrid

First, the working of DSTATCOM is explained through simulation results, followed by demonstration of power sharing in the AC microgrid. Lastly, the waveforms of the PV-battery system, rotor-side inverter and DSTATCOM DC-link are presented to show overall integrated operation of the proposed microgrid system.

The purpose of the DSTATCOM is to provide a pathway for supplying a fraction of the load real/reactive power directly from the PV array. As the load terminal voltage is fixed, the load kVA will be reflected in the current drawn by the load alone. So, it is sufficient to sense the load current for determining the load power that is to be compensated by DSTATCOM. The three-phase current at the load terminal is transformed to the dq0 axis with the d-axis aligned with 'a' phase of I_{LOAD}. By transforming the three-phase waveform from abc-domain to dq0-domain, the oscillating time domain waveform is converted to a more convenient DC form for the purpose of easy control action. The selection of reference waveform to compute angle theta, θ for transforming the variables in abc domain to dq0 domain needs to be done carefully. It is known that in a star-connected three-phase load, there is a 30° in angle between the line voltage and load current, which leads to non-zero reactive power component of load current (I_{QL}) even for UPF loads. As a result, the line-to-line voltage waveform cannot be considered for computing the angle of reference for abc-to-dq0 transformation. However, the AC microgrid phase voltage will be in-phase will the load terminal current for UPF

load. Hence, the three-phase to ground voltage at WRIG terminal has been considered for evaluating angle θ, which is computed using abc-αβ transformation.

The component of load current along the d-axis, I_{DL} represents P_{LOAD}, whereas the component along q-axis, I_{QL} represents Q_{LOAD}. In order that 50% of P_{LOAD} be supplied from DSTATCOM, the magnitude of corresponding reference current I_{DL_REF} will be 0.5*I_{DL}. As Q_{LOAD} will be supplied as such from DSTATCOM, the magnitude of corresponding reference current I_{QL_REF} will be equal to I_{QL}. The reference currents I_{DL_REF} and I_{QL_REF} are transformed back to the abc-coordinate system. This will be the current that the DSTATCOM will inject in the PCC to compensate for the given load power compensation setting. As the DC-link voltage is 445 V, a step-up transformer with turns ratio 1.667 has been used to interface the DSTATCOM with the PCC. The values of I_{DL} and I_{QL} are scaled appropriately before computing I_{DL_REF} and I_{QL_REF}.

Fig. 6.40 shows the angle of WRIG terminal phase voltage, theta evaluated through abc-αβ transformation. The load terminal current is transformed from abc- αβ frame of reference using the computed angle theta. The sinusoidal orthogonal components of the load current are shown in Fig. 6.41.

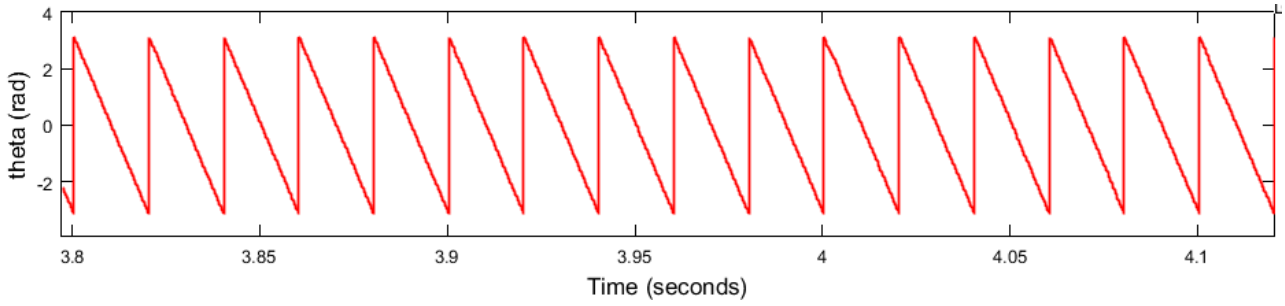


Fig. 6.40 Angle of WRIG terminal 'phase' voltage

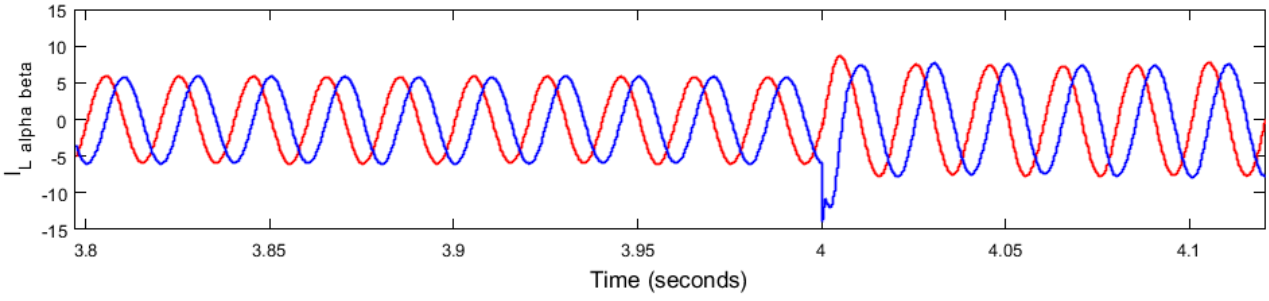


Fig. 6.41 Load current in αβ frame of reference

Subsequent transformation of load current from αβ frame of reference to dq0 frame of reference is carried out to get I_{DL} and I_{QL}. The current required to be injected by the DSTATCOM is computed by the control algorithm, and reference currents I_{DL_REF} and I_{QL_REF} are computed. The reference currents for different load settings are shown in Fig. 6.42.

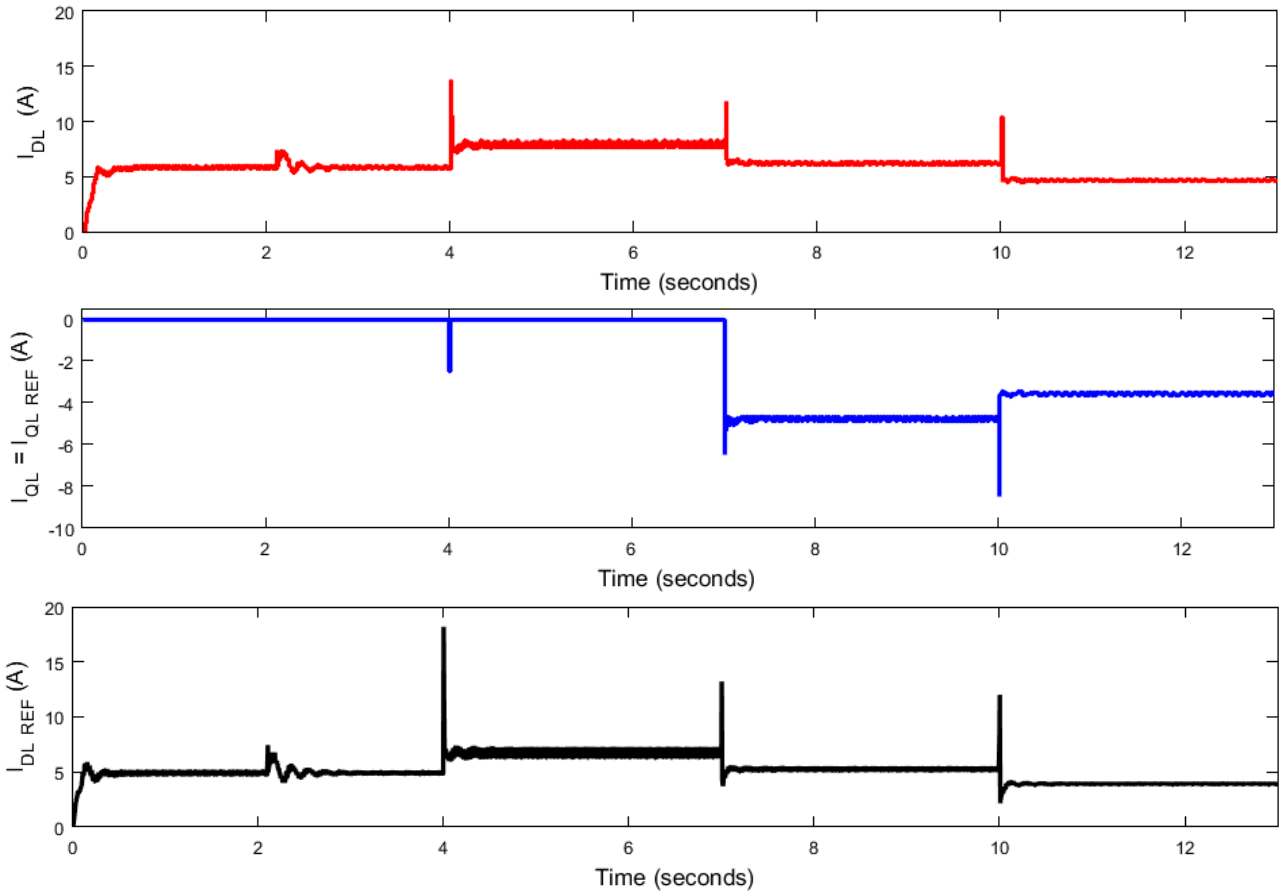
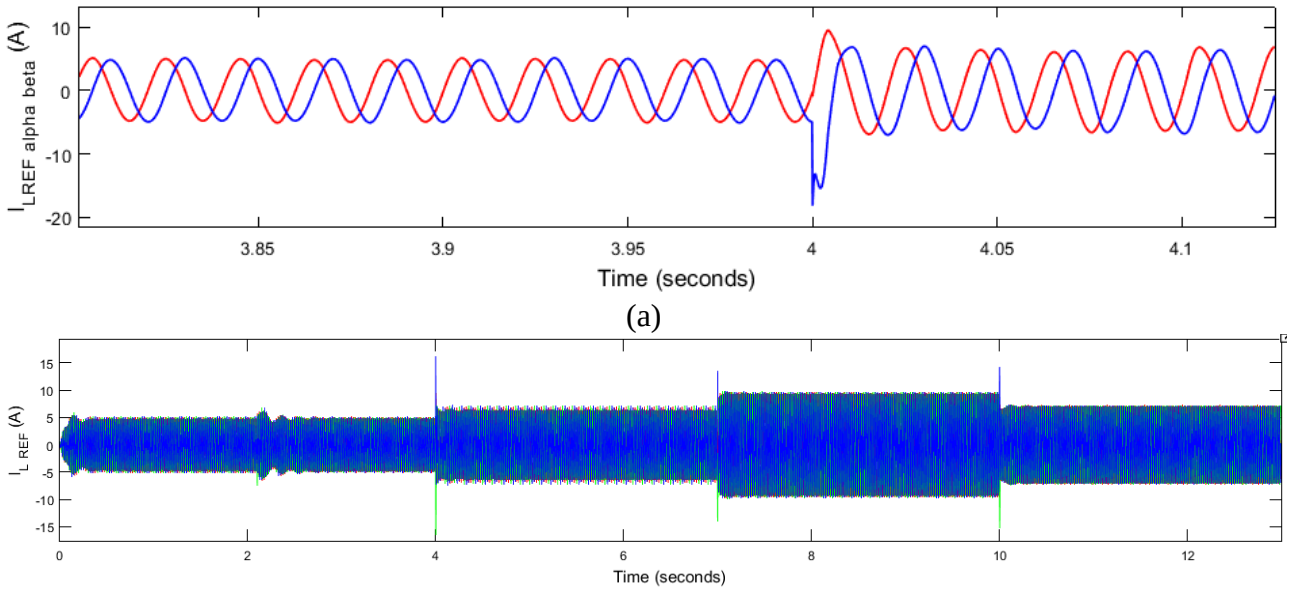


Fig. 6.42 Load current in dq reference frame and reference current for DSTATCOM

For injecting the current in the PCC, the reference currents must be transformed back to the abc domain through dq0- αβ transformation, followed by αβ-abc transformation. The corresponding waveforms are shown in Fig 6.43. The current I_{L_REF} is the reference current that is to be injected in the PCC by DSTATCOM to achieve load real/reactive power compensation.



(a)

(b)

Fig. 6.43 Transformation of reference currents from (a) dq0- αβ reference frame (b) αβ-abc reference frame

A hysteresis current controller of bandwidth 0.02 compares the generated reference current I_{L_REF} with the current injected in the primary winding of the step-up transformer, I_{INJ_PRI} continuously. Based on the deviation between I_{L_REF} and I_{INJ_PRI}, the pulses for the upper and lower IGBT switches in the three legs of the DSTATCOM inverter are switched ON/OFF. The corresponding waveforms of primary and secondary winding currents are shown in Fig. 6.44.

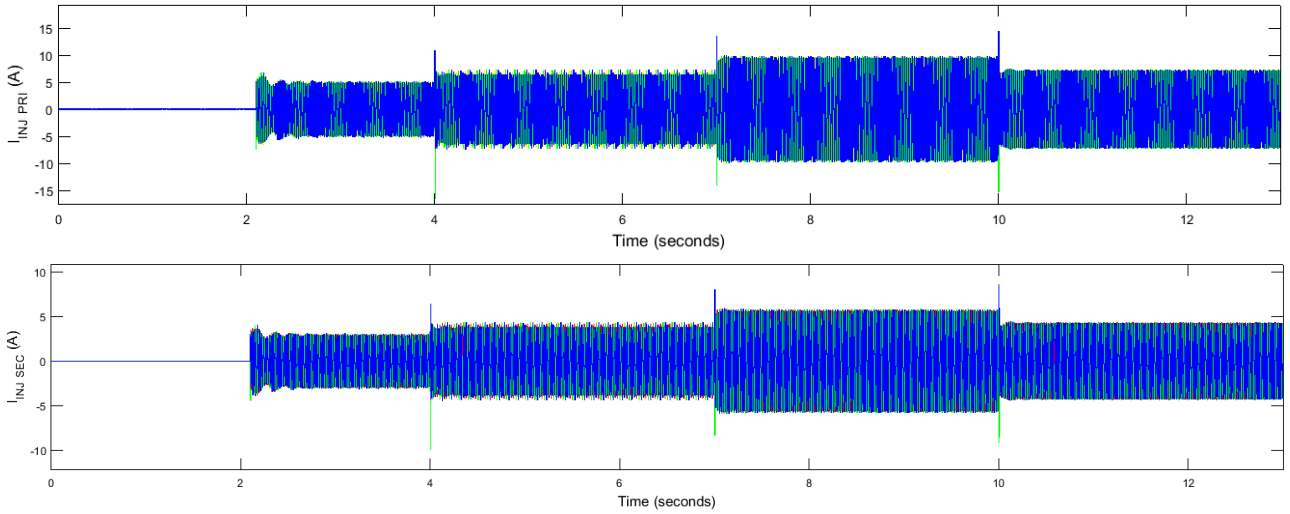


Fig. 6.44 Current injected by DSTATCOM in the transformer windings

The reference current tracking by the hysteresis current controller is shown in Fig. 6.45 along with the load current and currents in the transformer primary and secondary windings. The injected primary current I_{INJPRI} is made to follow the generated I_{L_REF} by the action of hysteresis current controller. Also, the transformer primary and secondary currents are in-phase which is an indication that the phase angle of the current waveform that is injected in the PCC is preserved.

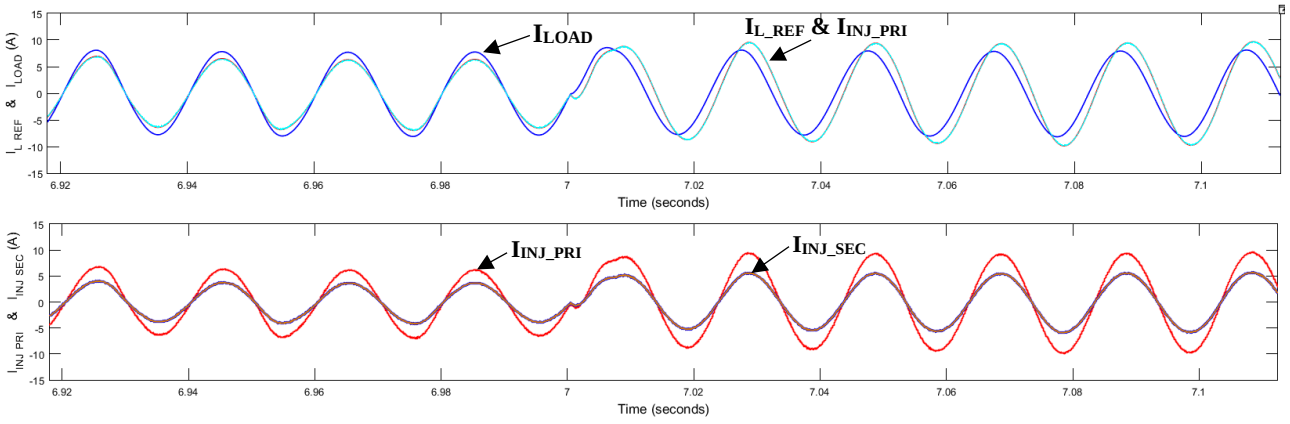


Fig. 6.45 Injected current waveforms

Before closing the DSTATCOM breaker, the load current is supplied by the WRIG and SCIG. After closing the breaker, the DSTATCOM injects power in the grid. As I_{SCIG} is fixed due to constant

N_{SCIG} before and after the DSTATCOM is connected, the WRIG stator current will reduce to maintain the power balance in the microgrid. This is shown in Fig. 6.46.

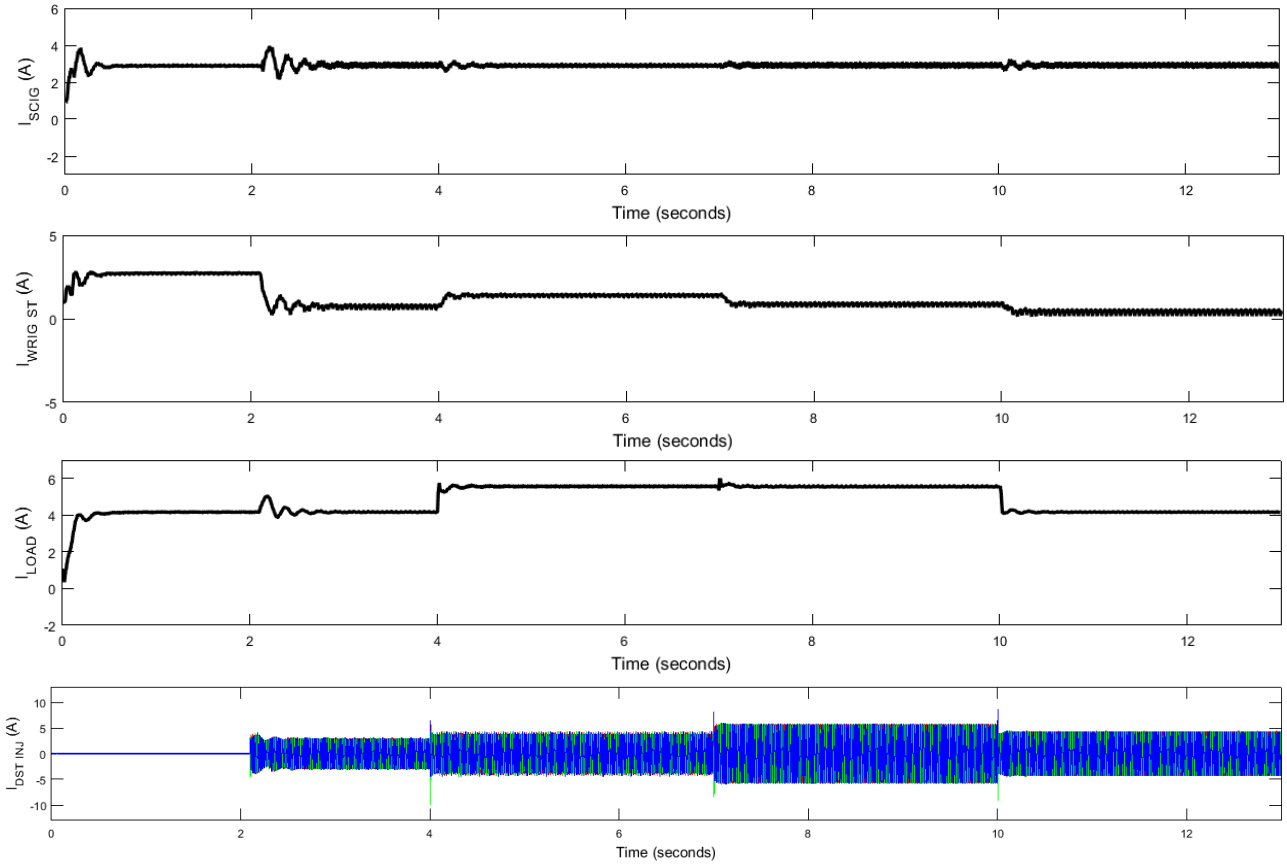
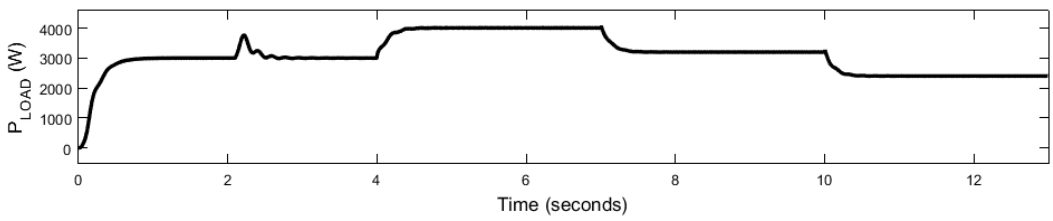


Fig. 6.46 Current measured at different terminals in the AC microgrid

The real/reactive power balance in the microgrid is shown in Fig. 6.47. The SCIG generates a constant power of 1.4kW before and after DSTATCOM breaker is closed at t=2.1s. In the time interval $0<t\leq2.1$ s, WRIG supplies the remaining 1.96 kW to meet load power requirement. However, Q_{WRIG} is almost zero as Q_{LOAD} is equal to zero, and $Q_{SCIG} = Q_{CAP}$. When the breaker is closed at t=2.1 s, the real power injected by DSTATCOM, $P_{STATCOM}$ is nearly 50 % of P_{LOAD}, i.e., 1.46 kW and reactive power injected by STATCOM is zero, as the load is a purely resistive one. Now, P_{WRIG} decreases to - 490 W to maintain the power balance in the system. In case of lagging p.f. loads, it can be seen that $Q_{STATCOM} = Q_{LOAD}$, $P_{STATCOM} = 0.5\ P_{LOAD}$, P_{SCIG} =1.04 kW, and $P_{WRIG} = P_{LOAD} – P_{SCIG} – P_{STATCOM}$. However, $Q_{WRIG} \approx 0$ when DSTATCOM is connected in the system.



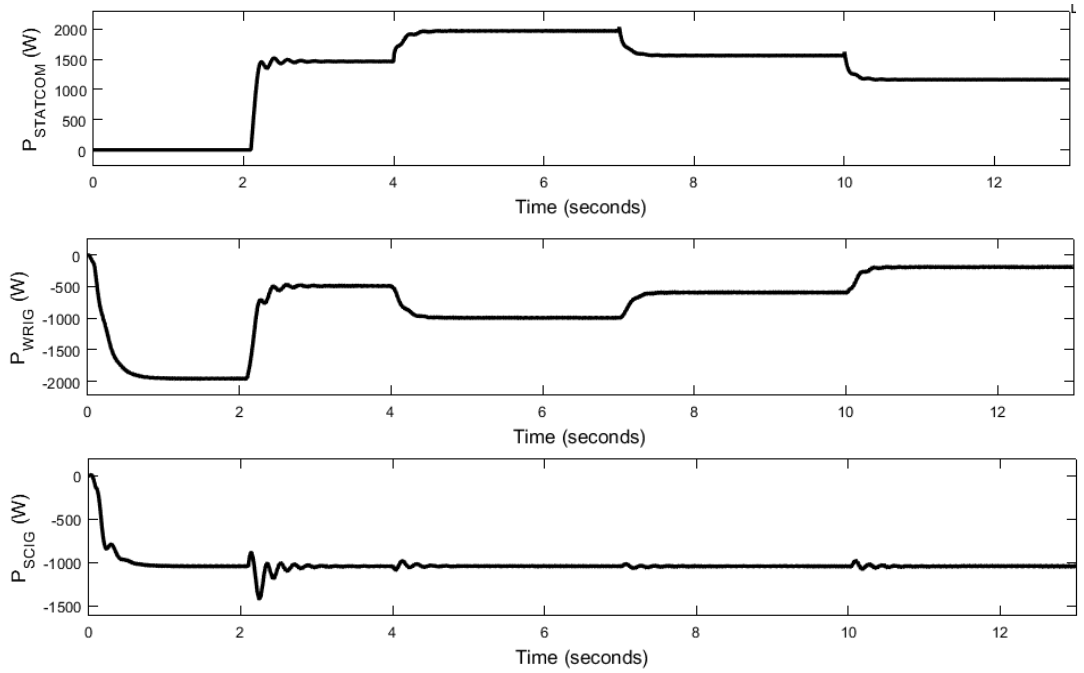
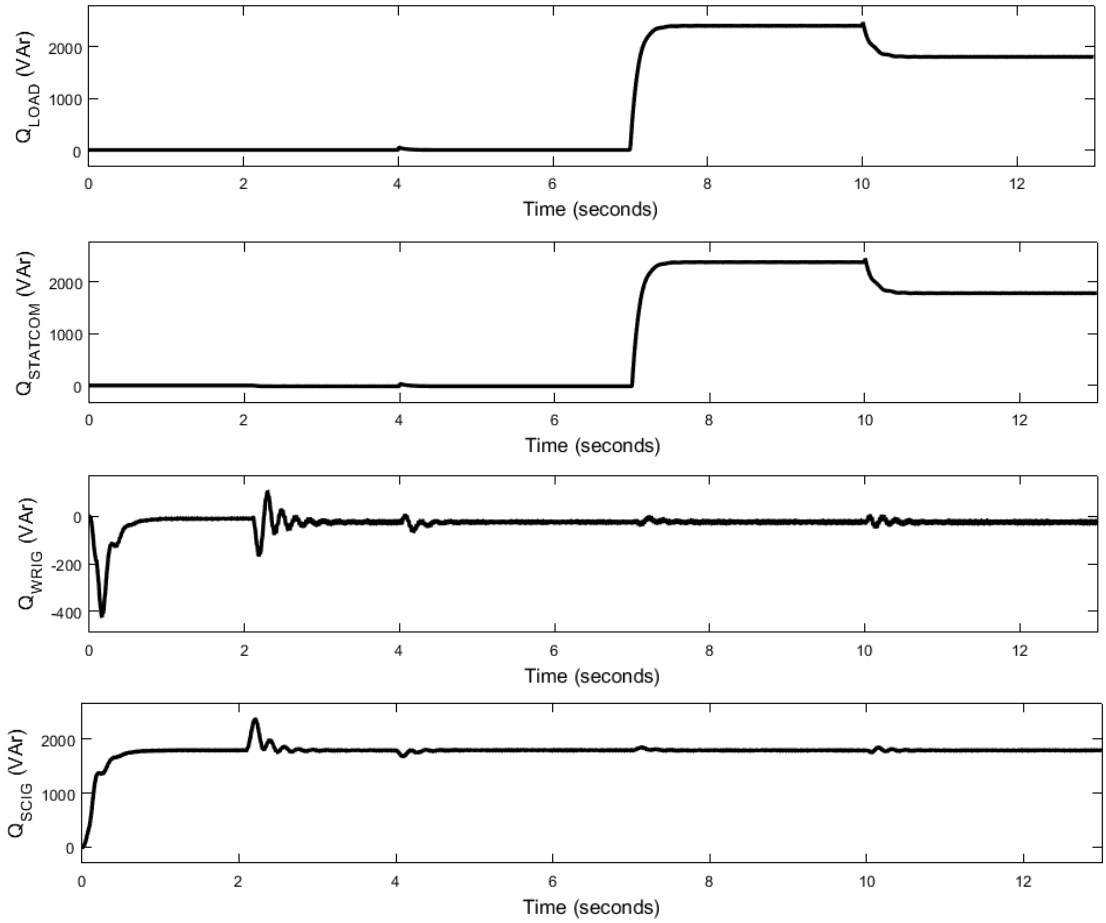


Fig. 6.47 (a) Real power balance before and after closing DSTATCOM breaker



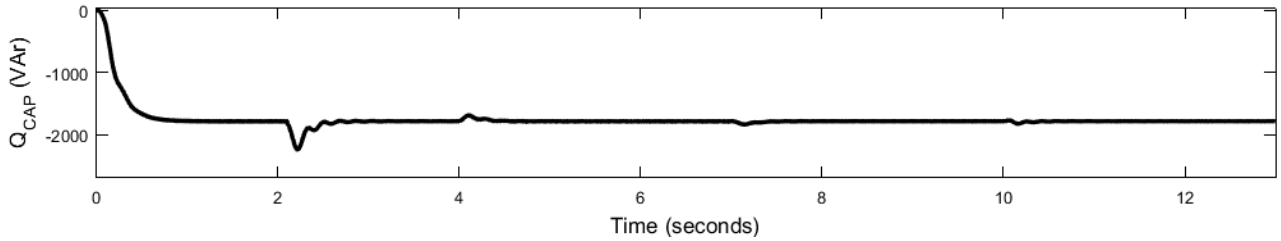


Fig. 6.47 (b) Reactive power balance before and after closing DSTATCOM breaker

The corresponding power flow in the DC side of the microgrid is presented below. The DC link voltage is maintained as 445.1 V by the battery bank, which is charged when P_{PV} is in excess of $P_{ROTOR\ INV}$ and $P_{DSTATCOM\ (DC)}$. The corresponding currents satisfy KCL at all times, irrespective of the load connected or variation in N_{WRIG}, N_{SCIG} and irradiation. This can be inferred from Fig. 6.48.

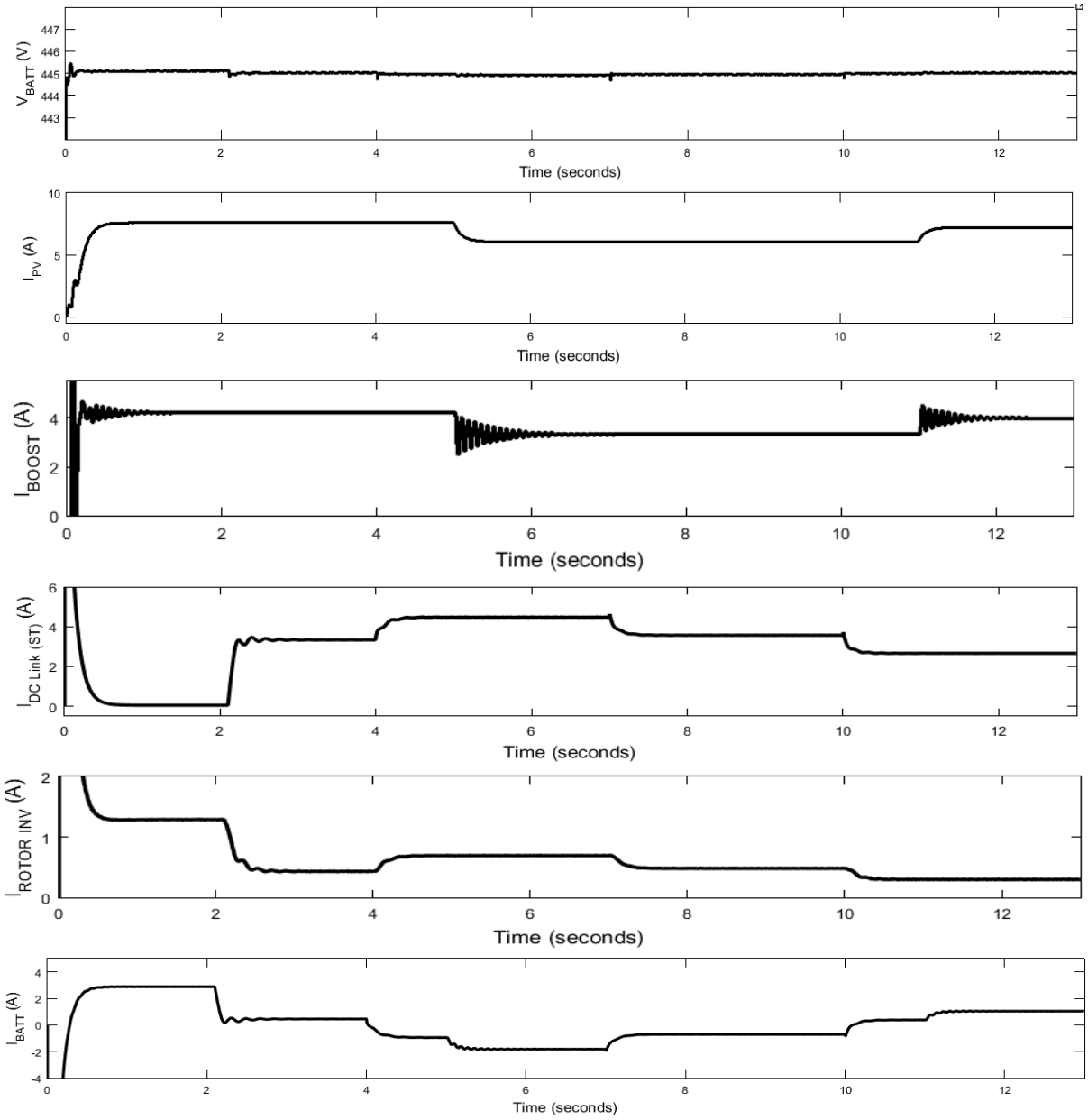


Fig. 6.48 Voltage and Current waveforms in the DC link

As the DC link voltage is constant, and all the currents in the DC link satisfy KCL, the power balance is also achieved. The corresponding real/reactive power injected by the rotor inverter is shown in Fig. 6.49. The modulation index of rotor-inverter is shown in Fig. 6.50.

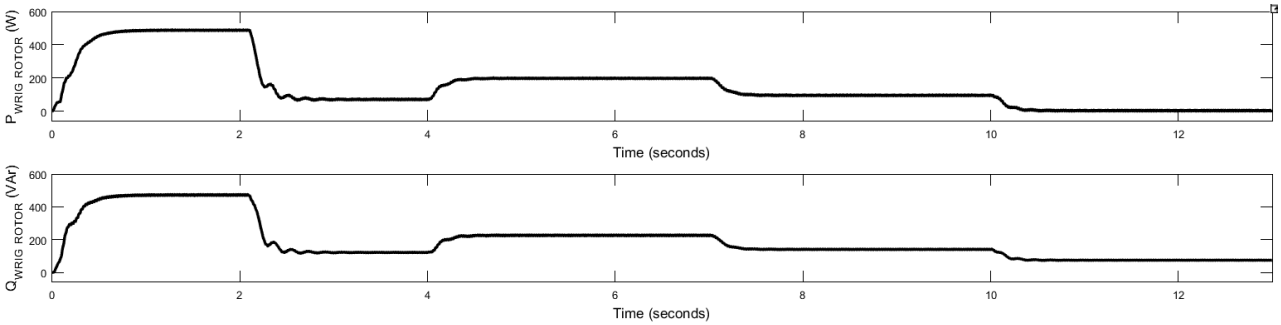


Fig. 6.49 Real and reactive power injected by WRIG rotor-inverter

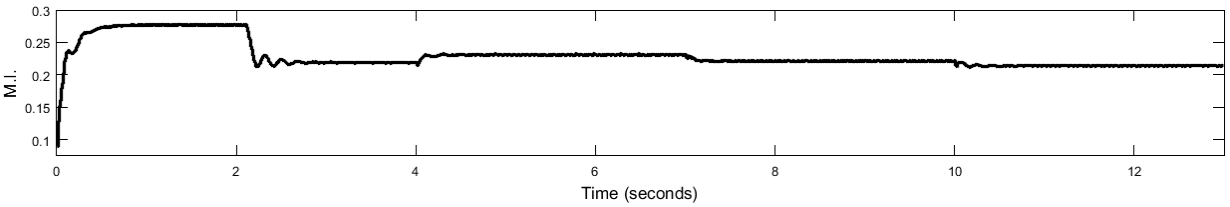


Fig. 6.50 Modulation index of rotor-inverter

CASE-IV: OPERATION OF DSTATCOM AS 50 Hz INVERTER SYSTEM POWERING THE ISOLATED LOADS IN THE ABSENCE OF WIND

In the proposed system shown in Fig. 1.5 the microgrid is formed by the wind and solar renewable energy sources. In the microgrid if the wind speed is less or power generation from wind energy is zero then there needs to be an alternative to supply the given load. In such condition by using solar PV panels it is possible to supply the AC loads, if we operate the 3- phase SPWM inverter with 50 Hz frequency. The simulation has been carried out by operating the SPWM inverter at 50 Hz for different loading conditions in MATLAB/Simulink environment.

6.4 Modelling of DSTATCOM as 50 Hz inverter in MATLAB/Simulink environment

The model of DSTATCOM as 50 Hz inverter in MATLAB is shown Fig. 6.51. The 50 Hz inverter system with Diesel generator (SCIG) is shown Fig. 6.52. The PV-boost converter-battery system along with MPPT controller which is explained in the above three cases is used in this case. A simple PI controller is employed to maintain the magnitude of inverter terminal voltage as 415 V. The error in inverter terminal voltage is constantly minimized by generating appropriate modulation index for SPWM 50 Hz inverter. The reference signal of the IGBT-based SPWM inverter shown in Fig. 6.51

comprises of three-phase balanced sinusoidal signals at 50 Hz frequency and magnitude equal to the modulation index. The switching pulses for the six power devices are generated by comparing the three-phase reference signals with a triangular signal of 10 kHz frequency. As the DC bus voltage is only 440 V (for battery SOC 82 %), the maximum RMS output voltage of inverter is 270 V for a modulation index of unity. Hence, a three-phase step-up transformer is required for powering the isolated loads. As shown in Fig. 6.52, while the load shared by the both inverter and SCIG, inverter gives reactive power support for the SCIG and additional reactive power support is given by Δ connected 2 kVAr capacitor.

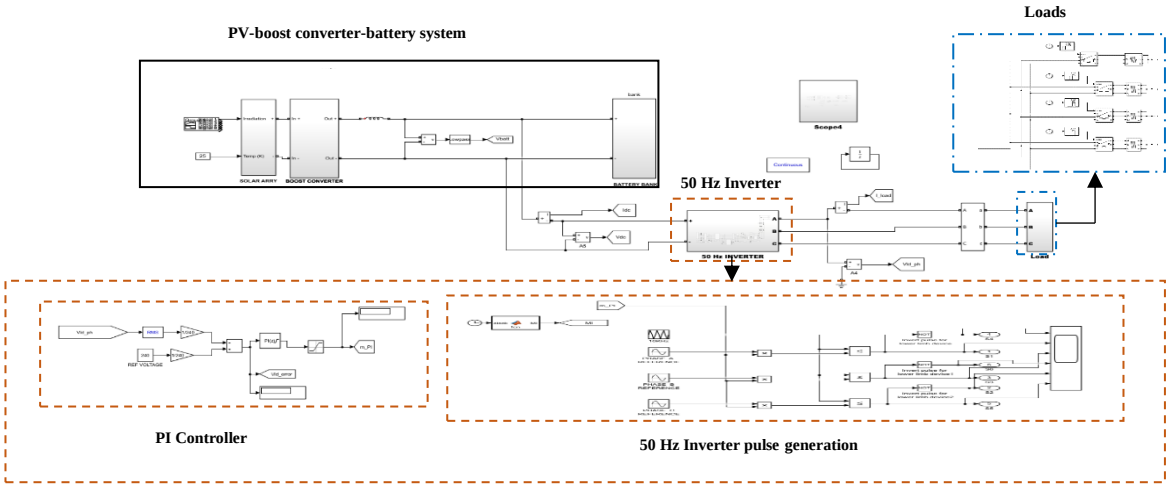


Fig. 6.51 50 Hz inverter system in MATLAB/Simulink environment

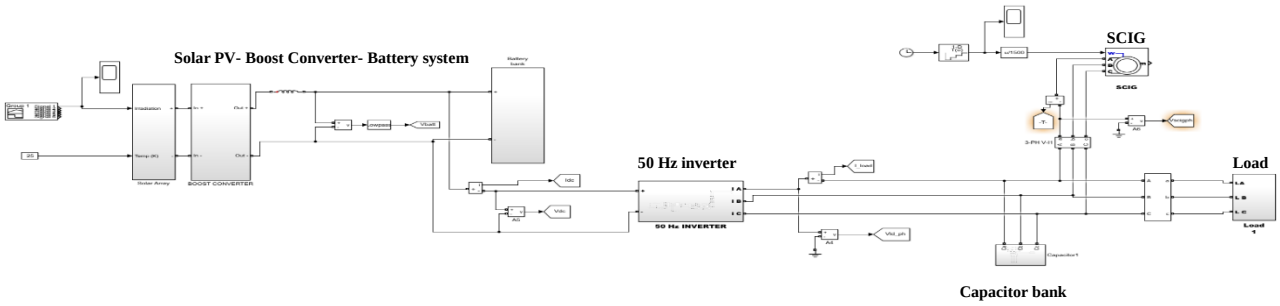


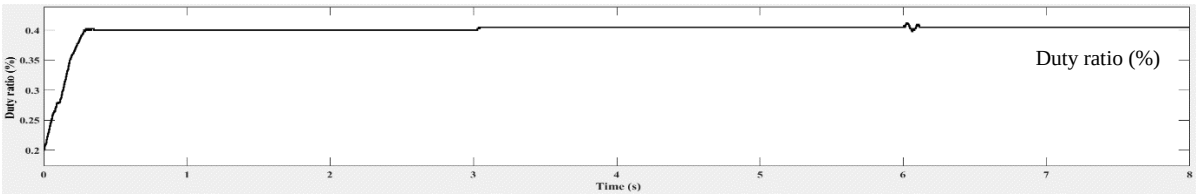
Fig. 6.52 50 Hz inverter system with SCIG in MATLAB/Simulink environment

6.5 Simulation results

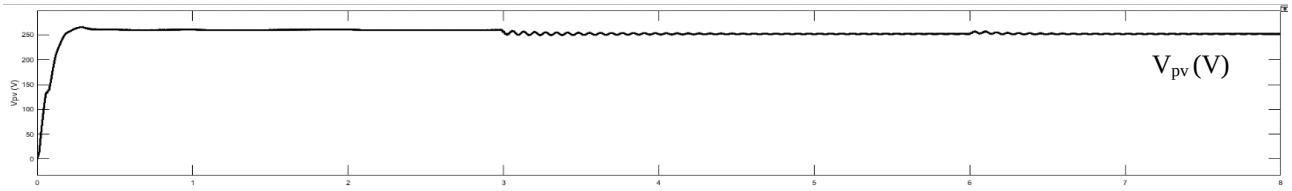
The simulation of the system has been carried out, and results are presented to demonstrate the operation of the 50 Hz inverter system without diesel generator (SCIG) and with diesel generator (SCIG). The load powering by PV-Battery-50 Hz inverter system and diesel generator (SCIG) are demonstrate through simulation results. The sampling time of the simulation solver is set as 5 µs.

Mode-I: **PV- BATTERY- 50 Hz INVERTER SYSTEM POWERING THE ISOLATED LOADS IN THE ABSENCE OF WIND (Without SCIG)**

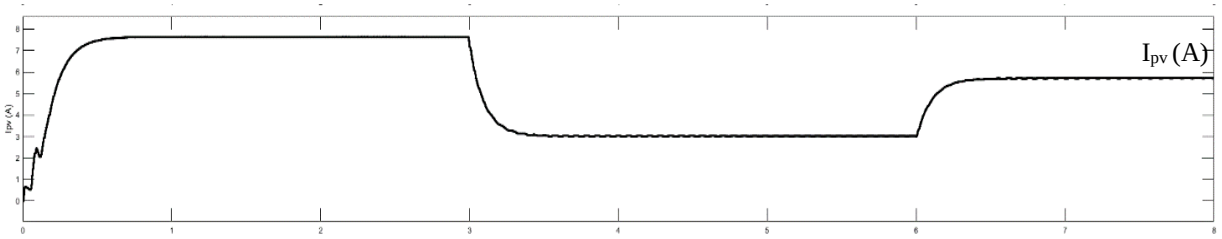
The operation of PV- battery- 50 Hz inverter system powering the 3-phase isolated loads without diesel generator (SCIG) is explained through simulation results. The Solar PV-BOOST converter-battery system, which is explained in the above three cases has been used for this system. The solar irradiation level is varied continuously, between 400 and 1000 W/m^2. The isolated load connected in the system is varied from 0.5 kW to 2 kW, UPF. Fig.6.53 (a) (b) and (c) shows the duty ratio of boost converter, voltage and current from the PV panel for different irradiation levels. Variation in Solar array current (I_{pv}), boost converter output current (I_{boost}) and PV array power output (P_{pv}) with variation of solar irradiation is given in Fig. 6.53 (c), (d) and (e).



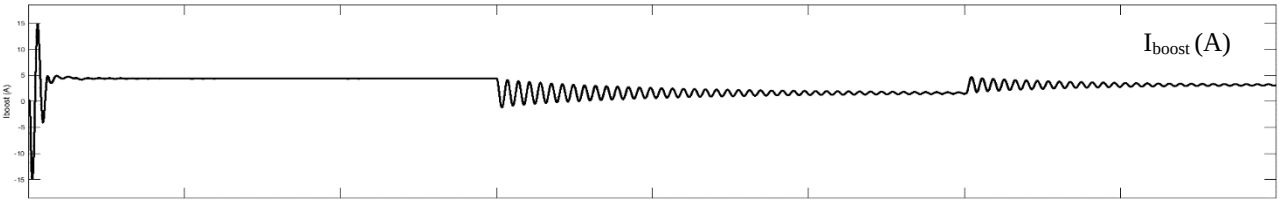
(a)



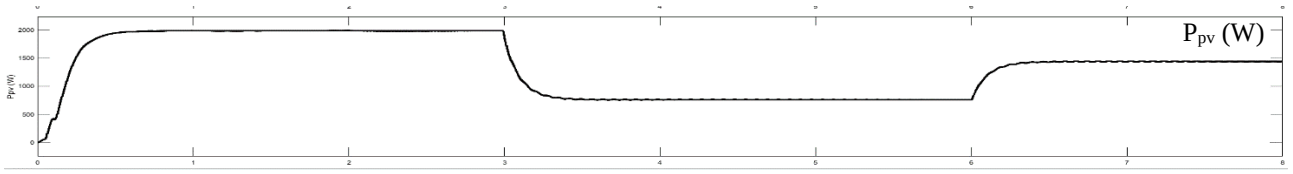
(b)



(c)

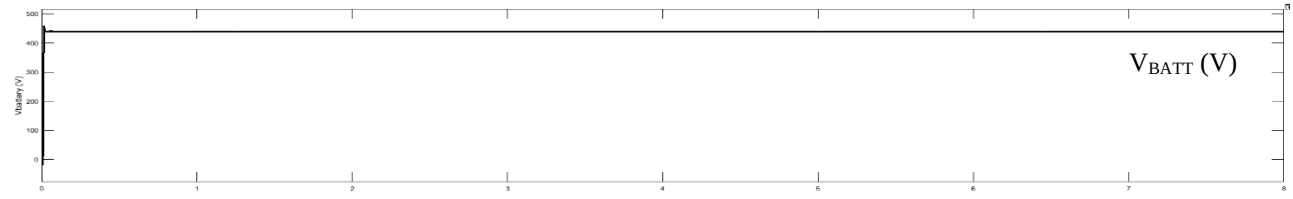


(d)

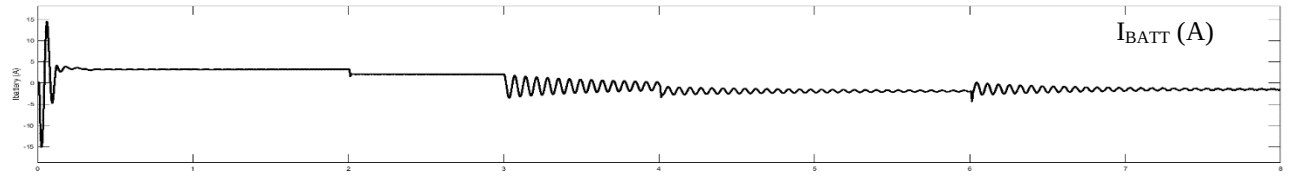


(e)

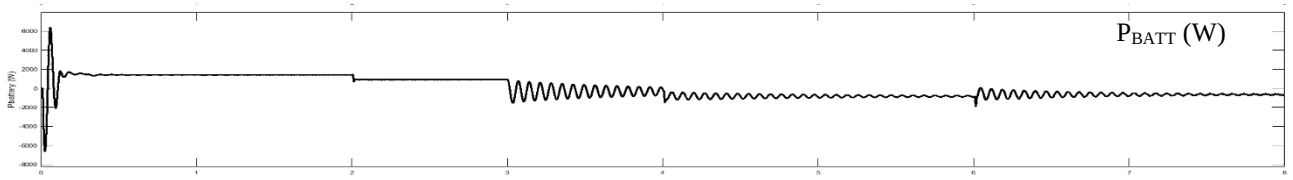
Fig. 6.53 Waveforms of PV-Boost converter system for different irradiation levels (a) PV array terminal voltage (b) PV array terminal current (c) Terminal current of DC-DC boost converter (d) Power output of PV array.



(a)



(b)

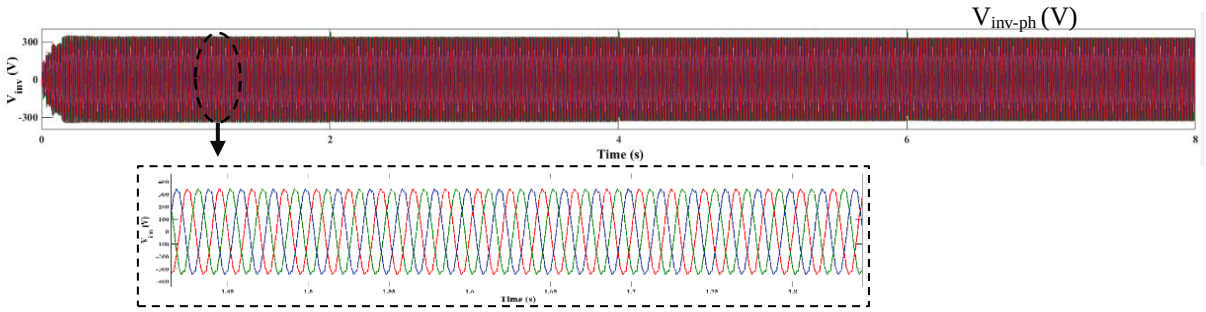


(c)

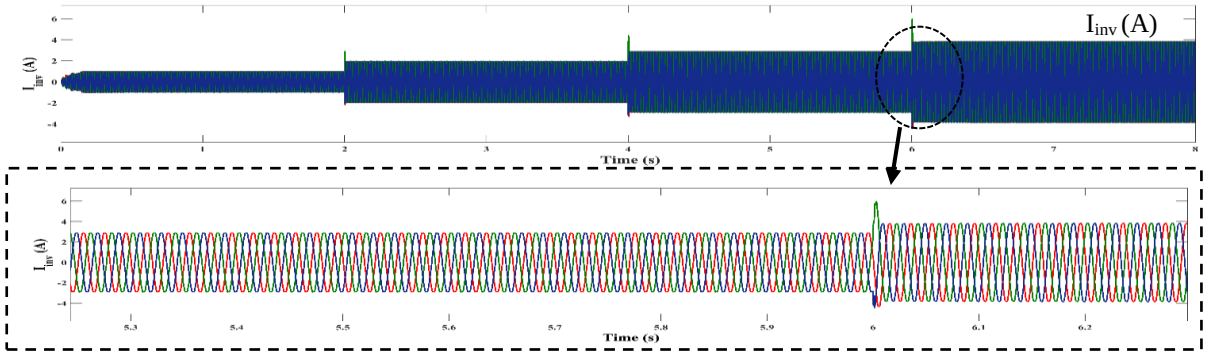
Fig.6.54 Waveforms of battery bank for different irradiation levels (a) Battery terminal voltage (b) Battery terminal current (c) Power absorbed by battery bank

There is a gradual infinitesimally small increase in battery voltage during the time intervals 0 to 3s and 6 to 8s, owing to the charging of the bank with substantial magnitude of battery current I_{BATT}, as shown in Fig.6.54 (b). Battery voltage is almost constant, which is show in Fig.6.54 (a) and corresponding power absorbed by the battery is given in Fig.6.54 (c).

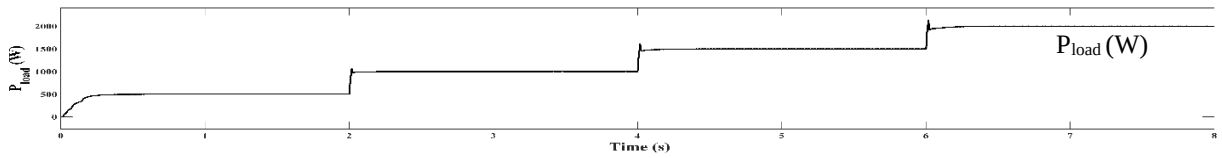
Working of the DSTATCOM as 50Hz inverter for powering the isolated loads is demonstrated through simulation results. The 50 Hz inverter must provide constant AC voltage of 415 (V_{L-L}) for the load. A simple PI controller has been used for the same. The values of the PI control parameters are $K_p = 0.09$, and $K_i = 12$. These values have been obtained through manual tuning.



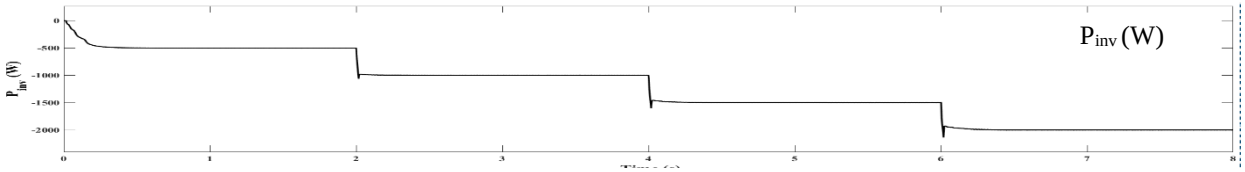
(a)



(b)



(c)



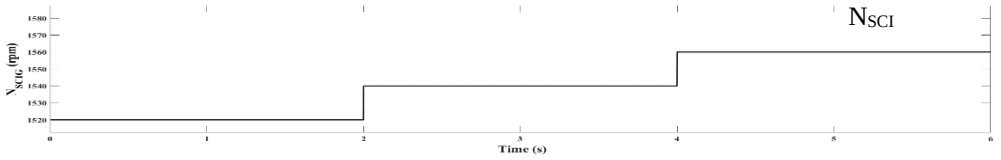
(d)

Fig.6.55 Waveforms of 50 Hz inverter and load (a) Inverter terminal voltage (b) Inverter current (c) Load power (d) Inverter power

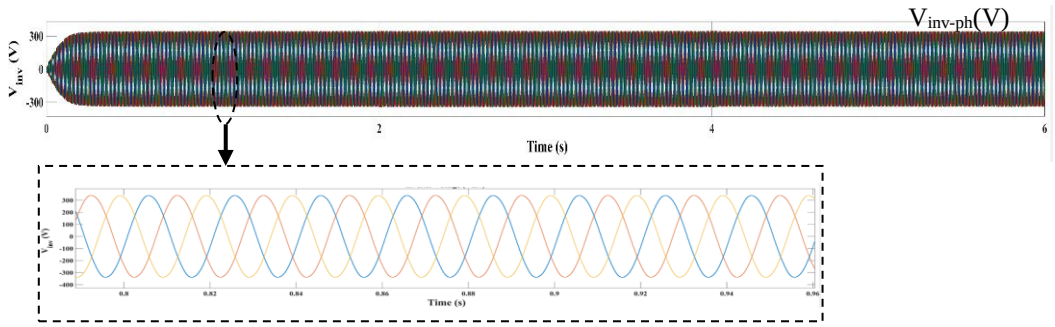
The operation of PV- battery- 50 Hz inverter system is tested with the isolated load of 0.5 kW to 2kW. For each time interval of 2 seconds load demand is increasing by 0.5 kW and it is limited to 2 kW because of solar PV array power rating. The inverter is maintaining constant voltage of 415 (V_{L-L}) at its terminals (V_{inv}) for different load values, which is given in Fig.6.55 (a). The load voltage and current are same as the inveter. As the load value increases, the current supplied by the inverter (I_{inv}) is also increased as in Fig.6.55 (b) and the inverter powering is the given loads as in Fig. 6.55 (c) and (d).

Mode-II: PV- BATTERY- 50 Hz INVERTER SYSTEM WITH DISEL GENERATOR (SCIG) POWERING THE ISOLATED LOADS IN THE ABSENCE OF WIND

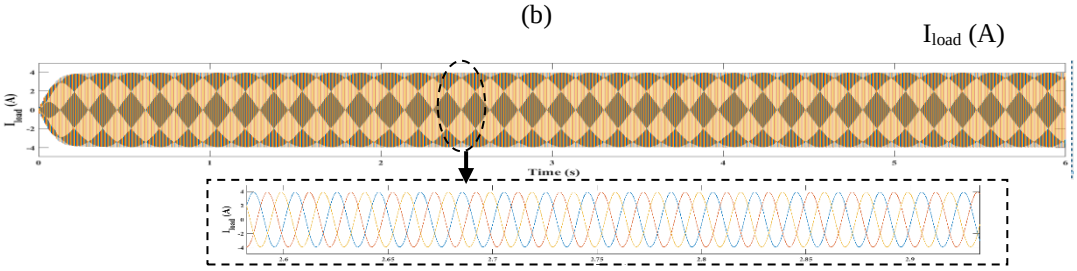
In this mode the operation of PV- battery- 50 Hz inverter system powering the 3-phase isolated loads with diesel generator (SCIG) is explained through simulation results. The isolated load connected in the system is 2 kW, UPF. The reactive power support for SCIG is provided through Δ-connected 2 kVAr capacitor bank and inverter. SCIG rotor speed varies from 1520 rpm to 1560 rpm as mention in Fig. 6.56 (a) to share the load. 50 Hz inverter is maintaining the constant voltage 415 V (V_{L-L}), which is shown in Fig.6.56 (b) and voltage at load and SCIG terminals are same as the inverter voltage. As the speed of SCIG (N_{SCIG}) increases load sharing by SCIG increases and reactive power absorption (Q_{SCIG}) also increases. The waveforms of load, inverter and SCIG currents in Fig. 6.56 (c) to (e).



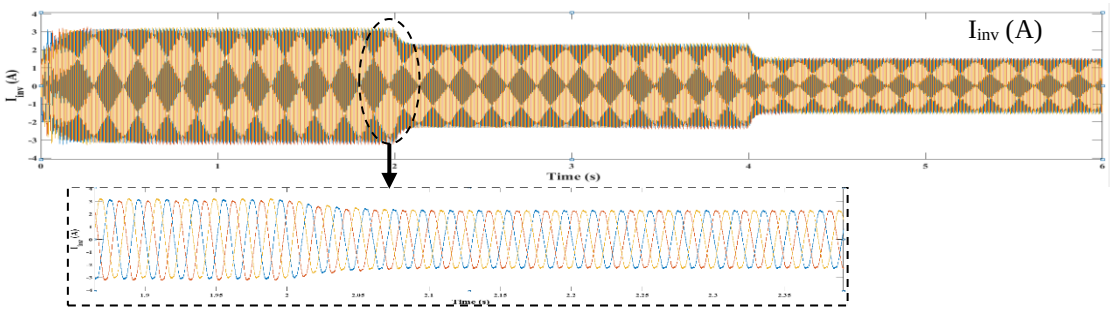
(a)



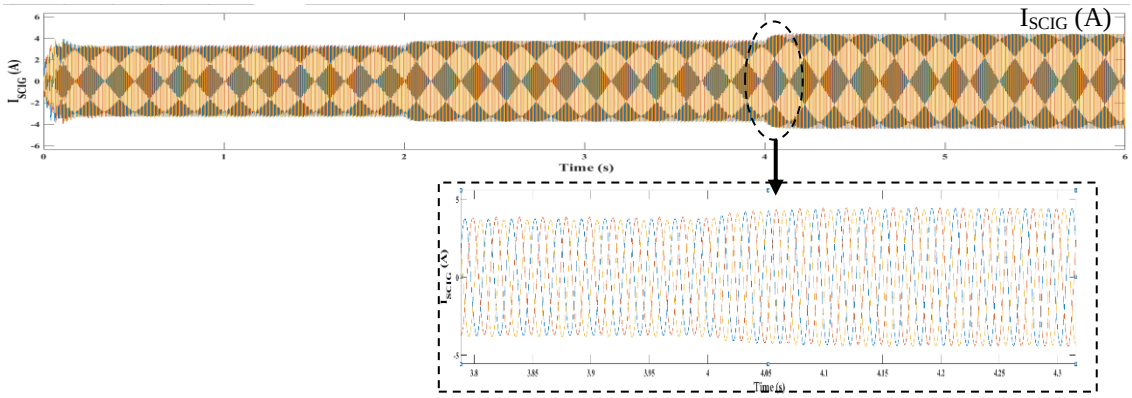
(b)



(c)



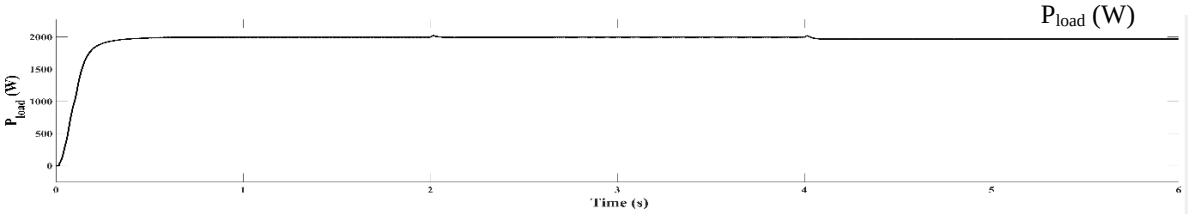
(d)



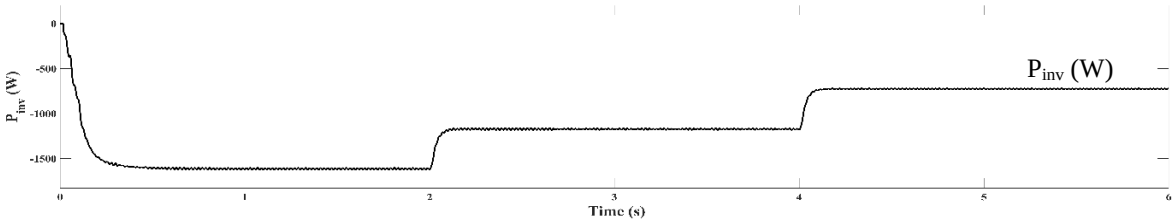
(e)

Fig. 6.56 Waveforms of load, 50 Hz inverter and SCIG (a) SCIG speed (b) Inverter terminal voltage (c) Load current (d) Inverter current (e) SCIG current

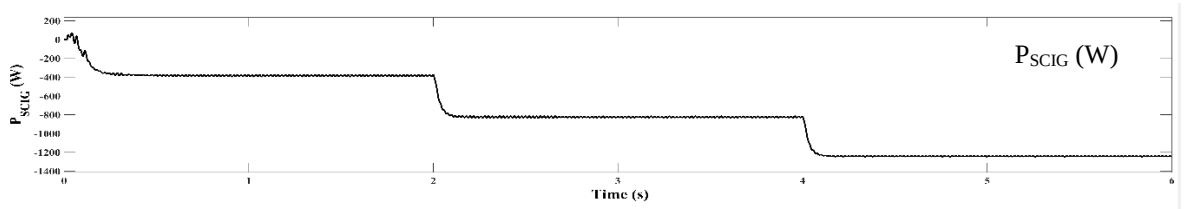
As the speed of SCIG increases, load power sharing by SCIG is also increases. The load power and power sharing by inverter and SCIG are mentioned in Fig.6.57. (a) to (c).



(a)



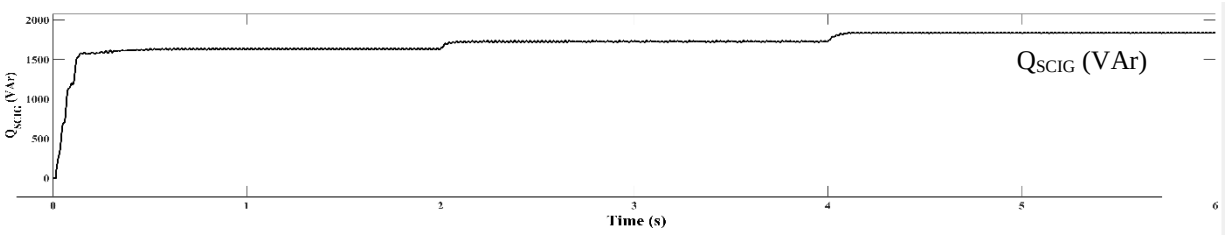
(b)



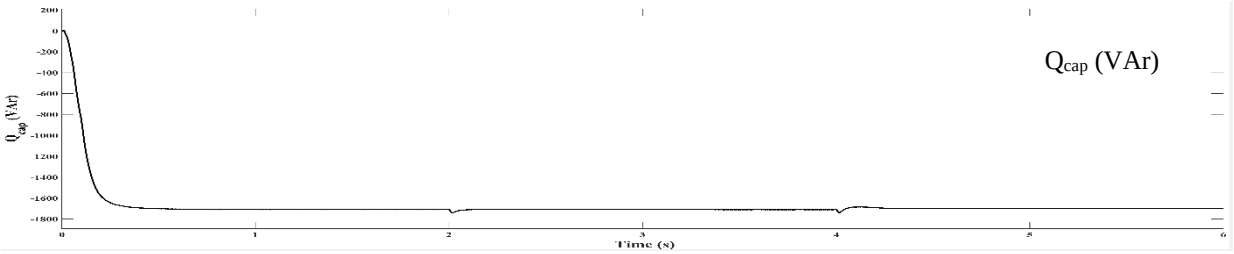
(c)

Fig. 6.57 Waveforms of load, 50 Hz inverter and SCIG (a) Load real power (b) Inverter real power (c) SCIG real power

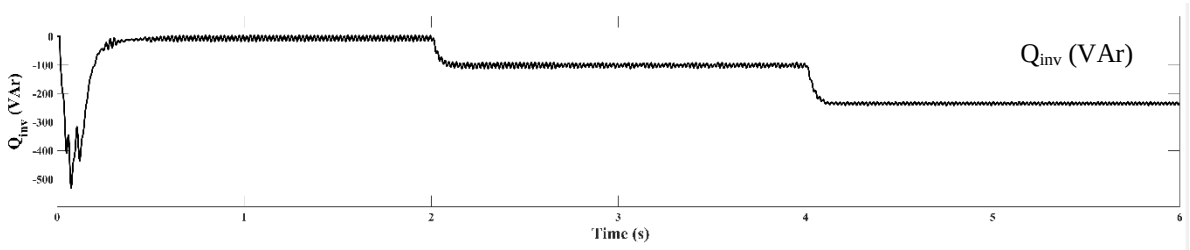
The reactive absorbed by the SCIG is proportional to its rotor speed. The reactive power absorbed by the SCIG from 1520 rpm to 1560 rpm and reactive power supplied by inverter and capacitor given in Fig 6.58 (a) to (c)



(a)



(b)



(c)

Fig. 6.58 Waveforms of load, 50 Hz inverter and SCIG (a) SCIG reactive power (b) Capacitor reactive power (c) Inverter reactive power

System Design Documents for 10 kW Hybrid system

Total capacity of the hybrid system = 10 kW

Total load to be supplied = 10 kW at 0.8 lagging power factor

Battery

Design 1 : 3 kW critical load should be supplied with 3 days of autonomy

The battery bank is designed to meet 3 kW of critical load with 3 days of autonomy in the absence of other energy sources. Under normal operating days, the battery bank is used to support the smooth function of system.

Total Wh required = 3 kW x 3 x 24h = 216 kWh

Considering the battery efficiency of 85% & depth of discharge of 60%, the kWh required for the battery is 216 kWh/(0.85 x 0.6) = 423.53 kWh

Considering the terminal voltage of battery as 440 V, which is the input to the inverter connected at WRIG rotor and also to the DSTATCOM.

Then the required Ah of the battery = $(423.\ 53 \times 10^3)/440 = 962$ Ah

i.e. approximately 1000 Ah.

Nominal voltage of the commercially available battery = 12 V

Hence, 37 batteries are needed to be connected in series to obtain 440 V.

So by choosing commercially available 12 V, 250 Ah battery,

Total number of batteries required = 148 (37 in series and 4 such series combinations in parallel)

Design 2 : 2 kW critical load should be supplied with 2 days of autonomy

The battery bank is designed to meet 2 kW of critical load with 2 days of autonomy in the absence of other energy sources. Under normal operating days, the battery bank is used to support the smooth function of system.

Total Wh required = 2 kW x 2 x 24h = 96 kWh

Considering the battery efficiency of 85% & depth of discharge of 60%, the kWh required for the battery is 96 kWh/(0.85 x 0.6) = 188.23 kWh

Considering the terminal voltage of battery as 440 V, which is the input to the inverter connected at WRIG rotor and also to the DSTATCOM.

Then the required Ah of the battery = $(188.23 \times 10^3)/440 = 427$ Ah

i.e. approximately 440 Ah.

Nominal voltage of the commercially available battery = 12 V

Hence, 37 batteries are needed to be connected in series to obtain 440 V.

So by choosing commercially available 12 V, 220 Ah battery,

Total number of batteries required = 74 (37 in series and 2 such series combinations in parallel)

Solar PV 3 kW

Solar PV panel is expected to supply 9 hours daily. However, the peak sun shine hours vary from 4.5 – 5 hours in south India. Considering the peak sun shine hours of 5 h, the required peak power of solar PV panel capacity is (3 kW x 9 h)/5 = 5.4 kW_p.

Consider a typical 200 W_p panel with (V_{oc} = 33 V, I_{sc} = 8.08 A and V_m = 27 V, I_m = 7.4 A), then

Number of PV panels needed = $(5.4 \times 10^3)/200 = 27$

These panels shall be connected as follows:

14 panels in series and two such combination in parallel (in total 28 panels). This gives an output dc voltage of (350 - 380) V at peak power point. So a boost converter is proposed to connect at the output of PV array to step up the voltage and maintain at 440 V, the battery terminal voltage. Further a closed loop controller is used to extract the maximum power from solar PV array by sensing the output power/current from the boost converter.

Wound Rotor Induction Generator (WRIG) based Wind Generator 3.75 kW

Specification: 5 kVA (3.75 kW), 3 phase, 50 Hz, 4 pole WRIG

Stator Line Voltage: 415 V, Rotor Line voltage: 200 V,

Considering the efficiency of 85%, the wind turbine rating should at least be 3.75/0.85 = 4.5 kW at rated wind velocity.

kVA rating of rotor side inverter

For the typical rating considered for the WRIG, the reactive power requirement of the machine is approximately 40% of its rating at 30 % operating slip for supplying full load at stator side at unity power factor.

Hence to have the safe operation of the system, a 5 kVA 440 V, 3-phase VSI is recommended at the rotor side. Further, it is recommended to connect a 3-phase 2 kVAr capacitor at the stator side for the improved operation of WRIG and also to have the reduced burden on the rotor side converter of WRIG. Any change in the load side reactive power is proposed to compensate with the DSTATCOM.

DSTATCOM

Considering the total system load of 10 kW at 0.8 lagging power factor, the reactive power requirement is 7.5 kVAr. The reactive power required by the SCIG is also proposed to compensate through DSTATCOM. In addition DSTATCOM is expected to provide the path for the real power transfer from the solar PV system to the load. When the WRIG is not functioning (because of low or no wind speed), the DSTATCOM will be operated as a 50 Hz voltage source inverter for supplying the isolated loads from the solar PV system and SCIG. So, with above all consideration, the rating of the DSTATCOM is chosen as 3-phase, 10 kVA. The AC output voltage of the DSTATCOM is decided by the battery bank voltage. In the present case it is 440 V. Hence, to connect the DSTATCOM with a 3-phase, 415 AC system, a 3-phase transformer is interfaced between the DSTATCOM and AC supply point.

Further in real time implementation of the system, if reactive power requirement of the load is more than 5 kVAr, switched capacitor/ fixed capacitor of 3 kVAr may be connected and only the variable reactive power will be supplied by DSTATCOM.

A DC capacitor is also recommended to be connected at the DC side of inverter to reduce the burden on battery for reactive power supply by DSTATCOM.

Squirrel Cage Induction Generator (SCIG) based Diesel Generator 3.75 kW

Specification: 5 kVA (3.75 kW),

3 phase, 50 Hz, 4 pole SCIG

Stator Line Voltage: 415 V

Considering the efficiency of 80%, the wind turbine rating should at least be 3.75/0.85 = 5 kVA.

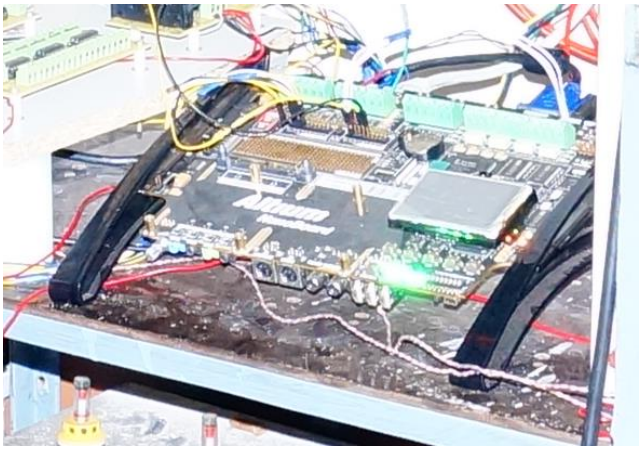
Technical Specifications of Experimental Setup used in the Laboratory

For demonstrating the proof of concept of the proposed hybrid system and developed algorithms, the commercially available equipments / components are employed. The specifications of the major components of the experimental set-up are given below:

Sl. No.	Component	Ratings
1.	Wound Rotor Induction Machine	3-phase, 4-pole, 3 HP; Stator: 415 V and 4.7 A, star-connection; Rotor : 185 V and 7.5 A, , star-connection.
2.	DC motor	220 V, 19 A, 5 HP and 1500 rpm
3.	SPWM Inverter (For Rotor side inverter of WRIG & DSTATCOM)	SEMIKRON make :V_{dc}= 750V, f = 20 kHz, output : 415V and 30A, 6 IGBT(SKM100GB12V) switches Filter inductance = 10 mH/ph DC Capacitor = 3000μF Maximum switching frequency of operation 10 kHz for WRIG inverter and 5 kHz for DSTATCOM
4.	PV panel	P_{max}= 200W, V_{oc} =33V, I_{sc}=8.08A
5.	PV array	10 panels (arranged in 2 parallel paths, 5 panels in each path) P_{max}=2 kW, V_{oc}=165V, I_{sc}=16.16A)
6.	Boost converter	IGBT(IRGTI090U06): V_{CE}=600V, I_C=90 A, V_{CE}(ON)<3.0V & 25 kHz ; Diode (DSEI3006A):$I_{F(AV)}$ = 37A, V_{RRM} = 600V, trr = 35ns, Inductor: 10mH, 20A and Capacitor: 470 μF/450V
7.	Battery bank	17 batteries are connected in series. Each rated for a nominal voltage of 12 V and 100 Ah.
8.	PI Controller for WRIG	K_P : 0.09 to 0.5 and K_I : 2.5 to 5.1
9.	Hysteresis band for DSTATCOM	0.02 A

FPGA Board (NB3000)

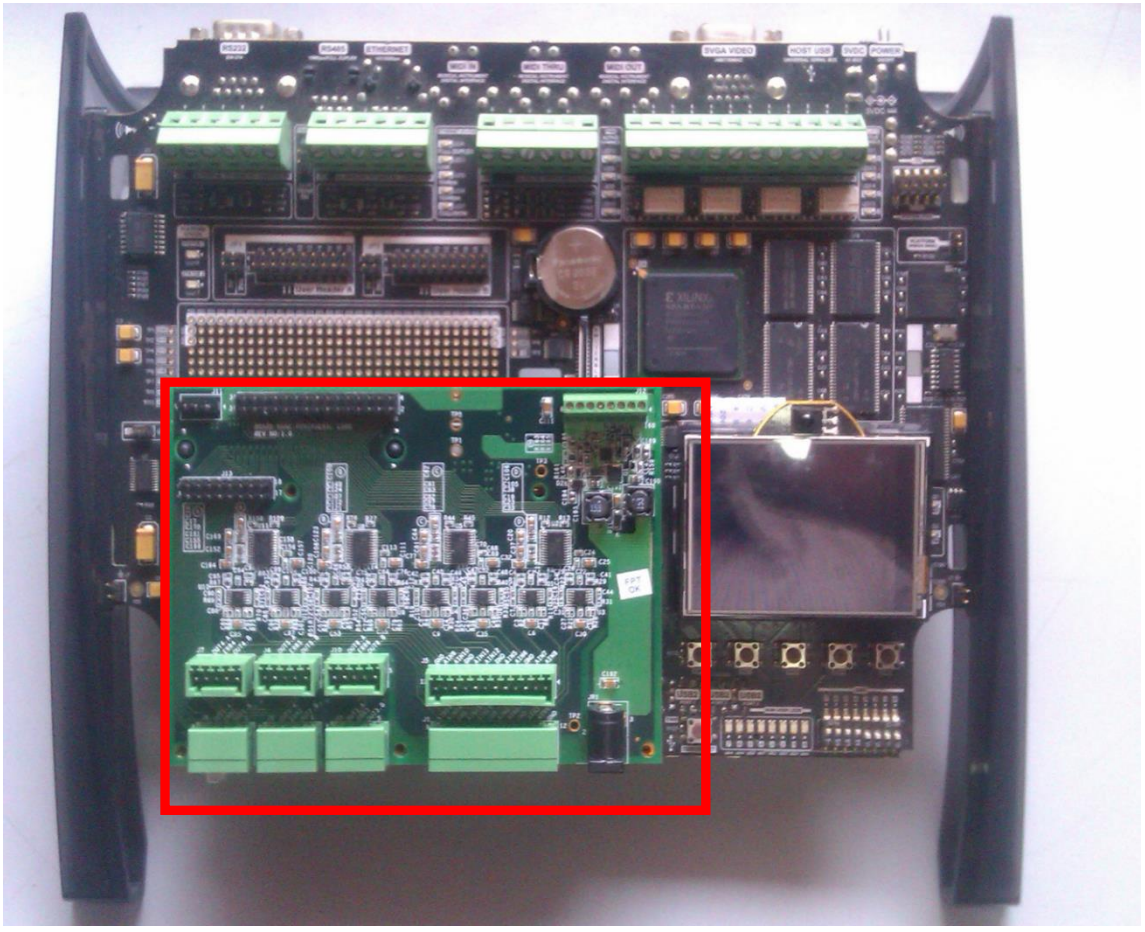
FPGA - Board – with fixed Xilinx Spartan 3 AN device
Variety of standard communications interfaces: RS-232, RS-485, PS/2, 10/100 Fast Ethernet, USB 2.0, S/PDIF, MIDI
Dual SD card readers – for use by user FPGA and Host Controller respectively
Programmable clock (6 to 200MHz) and fixed clock (20MHz) – both available to user FPGA
4-channel 8-bit ADC, SPI-compatible – providing maximum sample rate ≥ 200ksps
4-channel 8-bit DAC, SPI-compatible – operating at clock rates ≥ 40MHz
4x isolated IM Relay channels
4x PWM power drivers
8-way general purpose DIP-Switch, 8 RGB LEDs, 5 PDA-style push button switches and a Test/Reset button – all wired directly to the user FPGA
User prototyping area
On-board memories accessible by user FPGA
– 256KB x 32-bit common-bus SRAM (1MB), 16M x 32-bit common-bus SDRAM (64MB), 8M x 16-bit common-bus 3.0V Page Mode Flash memory (16MB), dual 256KB x 16-bit independent SRAM (512KB each)
Four 8Mbit SPI flash memory devices – one containing Primary boot image for Host Controller, one containing golden boot image for Host Controller, two for use by user FPGA (for boot/embedded purposes)
SPI Real-Time Clock with 3V battery backup
5V DC power connector with power switch, plus test points for all major supplies on the board (and GND)
High-speed PC interconnection through USB 2.0 for fast downloading and debugging



On-board ADC interface card (<u>Accessory for NB3000</u>)

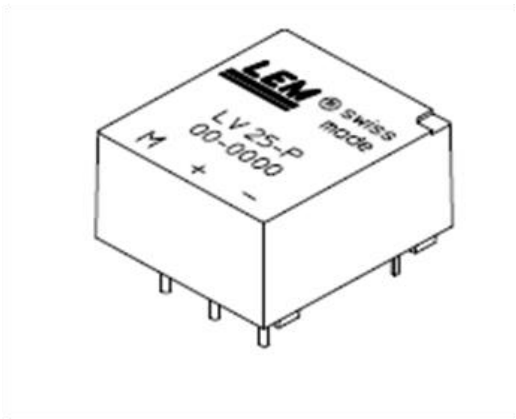
Contains four number of AD7367 ADCs

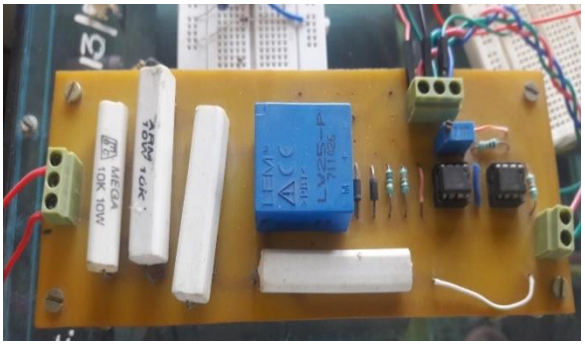
Each AD7367 contains Dual 14 Bit Signed 2 Channel ADC (total 4 input channels).
16 Channel Analog Inputs (8 Simultaneous conversation)
Sampling rate upto 1 MSPS
+/- 10V input range
12 Dedicated PWM Outputs , with 30V as collector value, in an open collector arrangement with a 10k load resistor
Ref voltage can be 3.3 V and 5 V



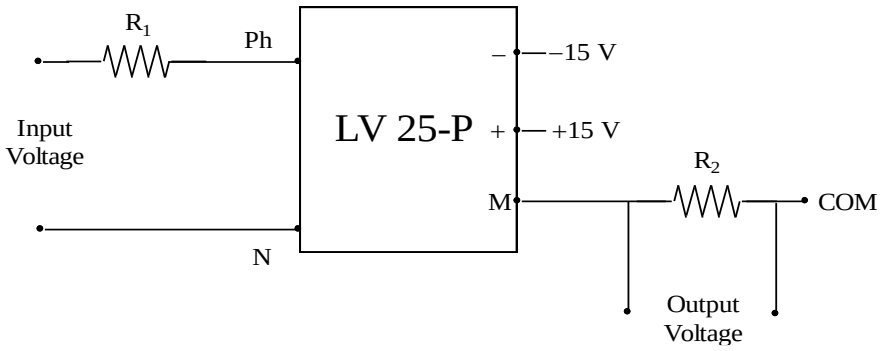
Voltage Sensor LEM LV 25-P

Primary nominal r.m.s. voltage	:	10 - 500 V
Primary nominal r.m.s. current	:	10 mA
Secondary nominal r.m.s. current	:	25 mA
Conversion ratio (KN)	:	2500:1000
Supply voltage (VC)	:	±12 - 15 V





For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R2 shown in figure below, which is selected by the user and installed in series with the secondary circuit of the transducer, so that the amplitude of voltage signal fed to the ADC does not exceed its limit (3.3 V). R1 is selected in such a way that the input current should not exceed 10 mA.



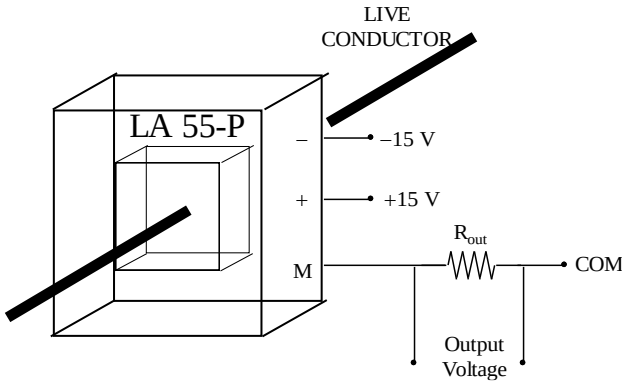
Current Sensor LEM LA 55-P

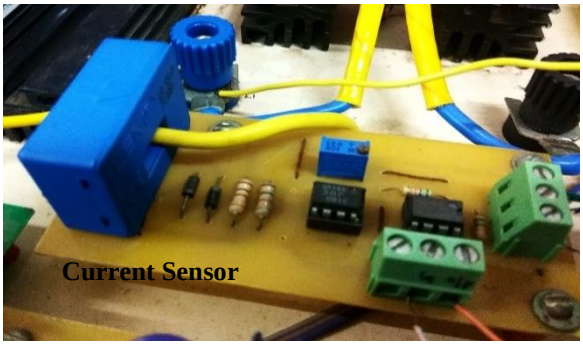
Primary nominal r.m.s. current : 50 A

Secondary nominal r.m.s. current : 50 mA

Conversion ratio : 1:1000

Supply voltage : ±12 - 15 V





Software Programs of Real Time Controller

CLOSED LOOP COTROLLER CODE

```
#include <stdlib.h>
#include "hardware.h"
#include <stdio.h>
#include <time.h>
#include <math.h>
#include <devices.h>
#include <drv_dac084s085.h>
#include <timing.h>
#include <drv_adc084s021.h>
#include <drv_ioport.h>

static void init( void );
static int next_channel(uint8_t channels, uint8_t
current_channel, uint8_t max_channels);
dac084s085_t    *dac;
adc084s021_t    *adc;
ioport_t        *ioport;

/*****************************************************************
*******
|*
|*  Function    : main
|*
|*  Parameters  : None
|*
|*  Returns     : None
|*
|*  Description : Continuously read and display the contents of
the ADC */
void main( void )
{
    float samp=60,period,MI,amp,freq,st=0,N,VOL;
    float t=0.0,a,b,c,dif,Mdif;

    int sinx,siny,sino,i=0,MF=0;
    float pi=3.1416,Vref=1.05,Vmeas,E=0.03,m=250;//653589793 ;

    int *i1= Base_WB_PRTIO_1;
    int *i2= Base_WB_PRTIO_2;
    int *i3= Base_WB_PRTIO_3;
    //char ch;

   init();  //for opening adc / dac drivers
```

```
    for (;;)
    {
        /* read dip switches */


//modulation index and modulation frequency
    MF= adc084s021_read( adc, 0);

    MI = adc084s021_read( adc, 1);


   VOL=MF*0.012890625;

   N=VOL*1000/1.5;
   freq=(1500-N)/30;

   Vmeas=(MI*3.3)/255;

   Mdif=(Vmeas-Vref);
   dif=Mdif;
   if(dif<0)
     Mdif=-1*Mdif;
   printf("Vmeas= %f\n",dif);

   if(Mdif >= E)
   {
      if(dif>=0)
     {
        m=m-0.02;
     }

      else if(dif<0)
       {
          m=m+0.02;
       }
   else if(Mdif <= E)
      m=m;
   }

//upper and lower limits of amplitude
    if(m>250)
    m=250;
    if(m<15)
    m=15;
    amp=m;
//amp=MI;
```

```
    samp=3600/freq;
// 0-60hz                                1000samp=>3hz
     period=samp/2;
//57hz==60samples without any change
     *i1= sino;
     *i2= sinx;
     *i3= siny;
     a=sin(t*pi/period);
     b=sin((t/period+0.66)*pi);
     c=-(a+b);
     sino=amp*.5+ amp*a*0.5;
     sinx=amp*.5+ amp*b*0.5;
     siny=amp*.5+ amp*c*0.5;
     t=t+1;
     if(t>=samp)
     t=1;

//showing the sine wave through DAC
//dac084s085_write(dac,DAC084S085_OUTA,(uint8_t)vp_use,true );
//dac084s085_write(dac,DAC084S085_OUTB,(uint8_t)vp_use,true );

dac084s085_write( dac, DAC084S085_OUTC,(uint8_t)sino,true );
//dac084s085_write( dac, DAC084S085_OUTD,(uint8_t)tri,true );

 }

}
```

```
/*************************************************************
*******
|*
|*  Function    : init
|*
|*  Parameters  : None
|*
|*  Returns     : None
|*
|*  Description : Initialize the hardware
 */

static void init( void )
{

    // ...and finally open the device driver
    printf( "Opening ADC:  ");
    adc = adc084s021_open( DRV_ADC084S021_1 );
    puts ( adc ? "OK" : "Fail" );
     dac = dac084s085_open( DRV_DAC084S085_1 );
    puts ( dac ? "dac_OK" : "dac_Fail" );
    ioport = ioport_open( DRV_IOPORT_1 );

}




static int next_channel(uint8_t channels, uint8_t
current_channel, uint8_t max_channels)
{
    uint8_t mask;
    int     i;

    /* check if bit is set in bits for higher channel numbers */
    mask = ~( ((int)1 << (current_channel + 1)) -1 );
    if (mask & channels)
    {
        for (i = current_channel + 1; i < max_channels; i++)
        {
            if (channels & (1 << i))
            {

                return i;
            }
        }
    }
```

```
    /* check if bit is set in bits for lower channel numbers */
    mask = (1 << current_channel) - 1;
    if (mask & channels)
    {
        for (i = 0; i < current_channel; i++)
        {
            if (channels & (1 << i))
            {
                return i;
            }
        }
    }

    return current_channel;
}
```

DSTATCOM CODE:

Hysteresis Controller Code:

```
1. library ieee;
2. use ieee.std_logic_1164.all;
3. use ieee.numeric_std.all;
4.
5. entity hys is
6. port (       clk : in std_logic ;
7.              ia_ref  : in std_logic_vector(7 downto 0);
8.              ia_act  : in std_logic_vector(7 downto 0);
9.              ib_ref  : in std_logic_vector(7 downto 0);
10.             ib_act  : in std_logic_vector(7 downto 0);
11.             ic_ref  : in std_logic_vector(7 downto 0);
12.             ic_act  : in std_logic_vector(7 downto 0);
13.             phb : out std_logic_vector(7 downto 0);
14.             nhb : out std_logic_vector(7 downto 0);
15.             pula  : out std_logic;
16.             pulb  : out std_logic;
17.             pulc  : out std_logic
18.             );
19.end entity hys;
20.
21. architecture hyst of hys is
22. constant hb : integer := 5;
23. constant hba : integer := 110;
24. constant hbb : integer := 110;
25. constant hbc : integer := 110;
26.
27. signal  ref1: std_logic_vector(7 downto 0) := (others => '0');
28. signal  act1 : std_logic_vector(7 downto 0) := (others => '0');
29. signal  phba : std_logic_vector(7 downto 0) := (others => '0');
30. signal  nhba : std_logic_vector(7 downto 0) := (others => '0');
31. signal  phbb : std_logic_vector(7 downto 0) := (others => '0');
32. signal  nhbb : std_logic_vector(7 downto 0) := (others => '0');
33. signal  phbc : std_logic_vector(7 downto 0) := (others => '0');
34. signal  nhbc : std_logic_vector(7 downto 0) := (others => '0');
35. signal  refa: std_logic_vector(7 downto 0) := (others => '0');
36. signal  refb: std_logic_vector(7 downto 0) := (others => '0');
37. signal  refc: std_logic_vector(7 downto 0) := (others => '0');
38. signal  ia_act1: std_logic_vector(7 downto 0) := (others => '0');
39. signal  ib_act1: std_logic_vector(7 downto 0) := (others => '0');
40. signal  ic_act1: std_logic_vector(7 downto 0) := (others => '0');
41.
42. begin
43.
44.A_proc: process (clk) begin
45.
46. if rising_edge(clk) then
47.  ia_act1 <= std_logic_vector((unsigned(ia_act)));
48.  refa <= std_logic_vector((signed(ia_ref))+hba);
49.  phba <= std_logic_vector((signed(refa) + hb));
50.  nhba <= std_logic_vector((signed(refa)-hb));
51.
52.  if((ia_act1 <  nhba)) then
53.
54. pula <= '1';
55.
56. elsif ((ia_act1> phba))  then
```

```
57.
58. pula <= '0';
59.
60. elsif(( ia_act1> nhba) and (  ia_act1 < phba)) then
61.
62. pula<= '1';

63. end if;
64. end if;
65.
66. end process A_proc;
67.
68. B_proc: process (clk) begin
69.
70. if rising_edge(clk) then
71.
72.  ib_act1 <= std_logic_vector((unsigned(ib_act)));
73.  refb <= std_logic_vector((signed(ib_ref))+hbb);
74.  phbb <= std_logic_vector((signed(refb) + hb));
75.  nhbb <= std_logic_vector((signed(refb)-hb));
76.
77.  if((ib_act1 <  nhbb)) then
78.
79. pulb <= '1';
80.
81. elsif ((ib_act1> phbb))  then
82.
83. pulb <= '0';
84.
85. elsif(( ib_act1> nhbb) and (  ib_act1 < phbb)) then
86.
87. pulb<= '1';
88.
89. end if;
90. end if;
91.
92. end process B_proc;
93.
94.  C_proc: process (clk) begin
95.
96. if rising_edge(clk) then
97.
98.  ic_act1 <= std_logic_vector((unsigned(ic_act)));
99.  refc <= std_logic_vector((signed(ic_ref))+hbc);
100.        phbc <= std_logic_vector((signed(refc) + hb));
101.        nhbc <= std_logic_vector((signed(refc)-hb));
102.
103.       if((ic_act1 <  nhbc)) then
104.
105.      pulc <= '1';
106.
107.      elsif ((ic_act1> phbc))  then
108.
109.      pulc <= '0';
110.
111.      elsif(( ic_act1> nhbc) and (  ic_act1 < phbc)) then
112.
113.      pulc<= '1';
114.
115.      end if;
116.      end if;
117.
118.      end process C_proc;
```

```
119.        end architecture hyst;
```

INVERSE PARK TRANSFORMATION:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity inverse_park is

    Port ( vd_act : in std_logic_vector(7 downto 0);
           vd_fil : in std_logic_vector(20 downto 0);
           v_q  : in std_logic_vector(7 downto 0);
           sine    : in std_logic_vector(15 downto 0);
           i_la  : in std_logic_vector(7 downto 0);
           i_lb  : in std_logic_vector(7 downto 0);
           i_lc  : in std_logic_vector(7 downto 0);
           i_0  : out std_logic_vector(7 downto 0);

           cosi    : in std_logic_vector(15 downto 0);
           Clk   :     in std_logic;
           v_alp  :    out std_logic_vector(7 downto 0);
           va  :    out std_logic_vector(7 downto 0);
           vb  :    out std_logic_vector(7 downto 0);
           vc  :    out std_logic_vector(7 downto 0);
           v_bet :    out std_logic_vector(7 downto 0);
           v_fil  :    out std_logic_vector(7 downto 0));


end inverse_park;

architecture rtl of inverse_park is

signal     v1 : std_logic_vector(15 downto 0) := (others => '0');
signal     v2 : std_logic_vector(15 downto 0) := (others => '0');
signal     sin : std_logic_vector(7 downto 0) := (others => '0');
signal     cos : std_logic_vector(7 downto 0) := (others => '0');
signal     alp : std_logic_vector(15 downto 0) := (others => '0');
signal     bet : std_logic_vector(15 downto 0) := (others => '0');
signal     v3 : std_logic_vector(15 downto 0) := (others => '0');
signal     v4 : std_logic_vector(15 downto 0) := (others => '0');
signal     v_d : std_logic_vector(7 downto 0) := (others => '0');
signal     v_d_fil : std_logic_vector(7 downto 0) := (others => '0');
signal     v_d_fil1 : std_logic_vector(15 downto 0) := (others => '0');
signal     v_q1 : std_logic_vector(7 downto 0) := (others => '0');
signal     i_n : std_logic_vector(7 downto 0) := (others => '0');
signal     i_n1 : std_logic_vector(15 downto 0) := (others => '0');
signal     i_n2 : std_logic_vector(7 downto 0) := (others => '0');

begin

process (clk) begin
if rising_edge(clk) then
sin<= sine(7 downto 0) ;
cos<= cosi(7 downto 0);
v_d_fil<= vd_fil(19 downto 12);
v_d_fil1<= std_logic_vector(signed(vd_fil(19 downto 12))*140);
v_d <=std_logic_vector(signed(vd_act)- signed(v_d_fil1(13 downto 6)));
v_q1<= v_q;
```

```
v1 <= std_logic_vector((signed(v_d)* signed(cos))  - (signed(v_q1)* signed(sin)));
v2 <= std_logic_vector((signed(v_q1)* signed(cos))  + (signed(v_d)* signed(sin)));
 v_alp<= v1(13 downto 6);
 v_bet<= v2(13 downto 6);
 v3 <= std_logic_vector((-signed(v1(13 downto 6))*30)+(signed(v2(13 downto 6))*52));
 v4 <= std_logic_vector((-signed(v2(13 downto 6))*52)- (signed(v1(13 downto 6))*30));

  i_n<=  std_logic_vector(unsigned(i_la)+  unsigned(i_lb) + unsigned(i_lc)-200-100);
 i_n1<= std_logic_vector(signed(i_n)*(0));
 i_n2<=i_n1(13 downto 6);

  i_0<=v_d;
  v_fil <= v_d_fil1(13 downto 6);



 va <= std_logic_vector(signed(v1(13 downto 6)));
 vb <= std_logic_vector(signed(v3(13 downto 6)));
 vc<=  std_logic_vector(signed(v4(13 downto 6)));
end if;
 end process;

 end architecture rtl;
```

CURRENT-CLARKE TRANSFORMATION:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity clarki is

    Port ( ia : in std_logic_vector(7 downto 0);
           ib  : in std_logic_vector(7 downto 0);
           ic    : in std_logic_vector(7 downto 0);
           ialpha    : out std_logic_vector(7 downto 0);
           id    : out std_logic_vector(7 downto 0);
           iq    : out std_logic_vector(7 downto 0);
           sine    : in std_logic_vector(15 downto 0);
           cosi    : in std_logic_vector(15 downto 0);
           clk   :     in std_logic;
           ibeta :    out std_logic_vector(7 downto 0);
           sin_0    : out std_logic_vector(7 downto 0);
           cos_0   : out std_logic_vector(7 downto 0));

end clarki;

architecture rtl of clarki is

signal     ialpha1 : std_logic_vector(15 downto 0) := (others => '0');
signal     ibeta1 : std_logic_vector(15 downto 0) := (others => '0');
signal     sin : std_logic_vector(7 downto 0) := (others => '0');
signal     cos : std_logic_vector(7 downto 0) := (others => '0');
signal     i_alp : std_logic_vector(7 downto 0) := (others => '0');
signal     i_bet : std_logic_vector(7 downto 0) := (others => '0');
signal     i1 : std_logic_vector(15 downto 0) := (others => '0');
signal     i2 : std_logic_vector(15 downto 0) := (others => '0');
signal     i3 : std_logic_vector(15 downto 0) := (others => '0');
signal     i4 : std_logic_vector(15 downto 0) := (others => '0');
begin
       process(clk) begin

       if rising_edge(clk) then
       sin<= sine(7 downto 0) ;
       cos<= cosi(7 downto 0);

        ialpha1 <= std_logic_vector((unsigned(ia)*44)- (unsigned(ib)*22)-
(unsigned(ic)*22));
        ibeta1 <= std_logic_vector((unsigned(ib)*38) - (unsigned(ic)*38));
        i_alp<= ialpha1(13 downto 6);
        i_bet <= ibeta1(13 downto 6);

        i1 <= std_logic_vector((signed(i_alp)* signed(cos))  + (signed(i_bet)*
signed(sin)));
        i2 <= std_logic_vector((signed(i_bet)* signed(cos))  - (signed(i_alp)*
signed(sin)));


        id<= i1(13 downto 6);

        iq<= i2(13 downto 6);
        ialpha<= ialpha1(13 downto 6);
         ibeta<= ibeta1(13 downto 6 );
         sin_0 <= sin;
         cos_0<= cos;
       end if;
       end process;
       end architecture rtl;
```

CLARKE'S TRANSFORMATION:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity clark is

    Port ( va : in std_logic_vector(7 downto 0);
           vb  : in std_logic_vector(7 downto 0);
           vc    : in std_logic_vector(7 downto 0);
           valpha    : out std_logic_vector(7 downto 0);
           valphabeta    : out std_logic_vector(15 downto 0);
           v_alpha    : out std_logic_vector(15 downto 0);
           v_beta    : out std_logic_vector(15 downto 0);
           clk   :     in std_logic;
           vbeta :    out std_logic_vector(7 downto 0));

end clark;

architecture rtl of clark is

signal     valpha1 : std_logic_vector(15 downto 0) := (others => '0');
signal     vbeta1 : std_logic_vector(15 downto 0) := (others => '0');
signal     valpha2 : std_logic_vector(15 downto 0) := (others => '0');
signal     vbeta2 : std_logic_vector(15 downto 0) := (others => '0');
signal     valpha3 : std_logic_vector(15 downto 0) := (others => '0');
signal     vbeta3 : std_logic_vector(15 downto 0) := (others => '0');
signal     valpha_beta : std_logic_vector(15 downto 0) := (others => '0');
begin
       process(clk) begin

       if rising_edge(clk) then

        valpha1 <= std_logic_vector((unsigned(va)*44)- (unsigned(vb)*22)-
(unsigned(vc)*22));
        vbeta1 <= std_logic_vector((unsigned(vb)*38) - (unsigned(vc)*38));
        valpha2<=std_logic_vector(signed(valpha1(13 downto 6)) * 48);
         vbeta2 <=std_logic_vector(signed(vbeta1(13 downto 6)) *48);
         valpha3<= std_logic_vector(signed(valpha1(13 downto 6)) * signed(valpha1(13
downto 6)));
        vbeta3 <=std_logic_vector(signed(vbeta1(13 downto 6)) *signed(vbeta1(13 downto
6)));
       valpha_beta <= std_logic_vector( signed(valpha3) + signed(vbeta3));

       end if;

       end process;

       valpha<= valpha1(13 downto 6);
       vbeta<= vbeta1(13 downto 6);
       valphabeta<= valpha_beta;
       v_alpha<= valpha2;
       v_beta<= vbeta2;


       end architecture rtl;
```

DAC_TOP CODE:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity dac_top is
  port ( mclk : in std_logic;
         rst : in std_logic;
         dat_valid : in std_logic;

 -- Interfacing signal to DAC084S045
         dac_sclk : out std_logic;
         dac_sync_n : out std_logic;
         dac_sout : out std_logic;
        --
        in1 : in std_logic_vector(7 downto 0);
        in2 : in std_logic_vector(7 downto 0);
        in3 : in std_logic_vector(7 downto 0);
        in4 : in std_logic_vector(7 downto 0)
        );
end entity dac_top;

architecture str of dac_top is

component dac084s085_interface
  port (-- Global Clock and Reset
         mclk : in std_logic;
         mrst : in std_logic;
        -- Interface signals to module interacting with DAC
            dac_data : in  std_logic_vector(7 downto 0);
              dac_ch : in  std_logic_vector(1 downto 0);
             dac_cmd : in  std_logic_vector(1 downto 0);
              dac_wr : in  std_logic;
         dac_wr_done : out std_logic;
        -- Interfacing signal to DAC084S085
           sclk : out std_logic;
         sync_n : out std_logic;
           sout : out std_logic
       );
end component;

signal dac_data : std_logic_vector(7 downto 0) := (others => '1');
signal dac_channel : std_logic_vector(1 downto 0) := "00";
signal inp1 : std_logic_vector(7 downto 0) := (others => '1');
signal inp2 : std_logic_vector(7 downto 0) := (others => '1');
signal inp3 : std_logic_vector(7 downto 0) := (others => '1');
signal inp4 : std_logic_vector(7 downto 0) := (others => '1');

begin

inst_dac084s085_interface : dac084s085_interface port map (
         mclk => mclk,
         mrst => rst,
     dac_data => dac_data,
       dac_ch => dac_channel,
      dac_cmd => "01",
```

```
     dac_wr => dat_valid,
dac_wr_done => open,
       sclk => dac_sclk,
     sync_n => dac_sync_n,
       sout => dac_sout
);

dac_read_proc: process (mclk) begin

inp1 <= std_logic_vector((unsigned(in1))+110);
inp2 <= std_logic_vector((unsigned(in2))+110);
inp3 <= std_logic_vector((unsigned(in3))+110);
inp4 <= std_logic_vector((unsigned(in4))+100);
if rising_edge(mclk) then
  if (dat_valid = '1') then

          if(dac_channel = "00") then
             dac_data <=inp1;
            dac_channel <= "01"  ;
            elsif (dac_channel = "01") then                //selecting dac channel
           dac_data<= inp2;
            dac_channel <= "10";
           elsif (dac_channel = "10") then
             dac_data <= inp3;
           dac_channel <= "11" ;
           elsif (dac_channel = "11") then
             dac_data <= inp4;
           dac_channel <= "00" ;
           end if;
   end if;
   end if;

end process;

end architecture str;
```

DAC INTERFACE:

```
library ieee;
use ieee.std_logic_1164.all;

--------------------------------------------------------------------------------
entity dac084s085_interface is
  port (-- Global Clock and Reset
         mclk : in std_logic;
         mrst : in std_logic;
        -- Interface signals to module interacting with DAC
          dac_data : in  std_logic_vector(7 downto 0);
            dac_ch : in  std_logic_vector(1 downto 0);
           dac_cmd : in  std_logic_vector(1 downto 0);
            dac_wr : in  std_logic;
         dac_wr_done : out std_logic;
        -- Interfacing signal to DAC084S085
           sclk : out std_logic;
         sync_n : out std_logic;
           sout : out std_logic
       );
end entity dac084s085_interface;
--------------------------------------------------------------------------------

--------------------------------------------------------------------------------
architecture rtl of dac084s085_interface is

-- DAC MAX Clock Rate is 40MHz. Here it is set to 25MHz
signal     sync_n_int : std_logic := '1';
signal       sclk_int : std_logic := '1';
signal    dac_wr_busy : std_logic := '0';
signal     dac_wr_reg : std_logic := '0';
signal        sout_sr : std_logic_vector(11 downto 0) := (others => '0');
signal dac_wr_done_sr : std_logic_vector(31 downto 0) := (others => '0');
--------------------------------------------------------------------------------
--
-- Format of Data Input to DAC
--
--  |15| |14| |13| |12| |11| |10| |09| |08| |07| |06| |05| |04| |03| |02| |01| |00|
--
--  15 & 14 => selects DAC Channel. Mapped to dac_ch input
--  00 -> DAC A
--  01 -> DAC B
--  10 -> DAC C
--  11 -> DAC D
--
--  13 & 12 => selects DAC mode. Mapped to dac_cmd input
--  00 -> Write to specified register but do not update outputs
--  01 -> Write to specified register and update outputs
--  10 -> Write to all register and update outputs
--  11 -> power down outputs
--
--  11 to 4 => 8 Data Bits MSB First. Mapped to dac_data input
--
--  3 to 0 => Dont Care
--------------------------------------------------------------------------------

begin

--------------------------------------------------------------------------------
-- data_proc:
```

```
-------------------------------------------------------------------------------
data_proc: process(mclk) begin
  if rising_edge(mclk) then
    --
    if (mrst = '1') then
      sclk_int <= '1';
    else
      sclk_int <= not sclk_int;
    end if;
    --
    dac_wr_reg <= dac_wr;
    dac_wr_done_sr <= dac_wr_done_sr(30 downto 0) & (sclk_int and (dac_wr or
dac_wr_reg));
    if ((mrst or dac_wr_done_sr(31)) = '1') then
      dac_wr_busy <= '0';
    elsif ((sclk_int and (dac_wr or dac_wr_reg)) = '1') then
      dac_wr_busy <= '1';
    end if;
    --
    if (mrst = '1') then
         sout_sr <= (others => '0');
      sync_n_int <= '1';
    elsif ((sclk_int and (dac_wr or dac_wr_reg)) = '1') then
      sout_sr <= dac_ch & dac_cmd & dac_data;
      sync_n_int <= '0';
    elsif(dac_wr_done_sr(31) = '1') then
      sync_n_int <= '1';
    elsif ((sclk_int and dac_wr_busy) = '1') then
         sout_sr <= sout_sr(10 downto 0) & '0';
      sync_n_int <= '0';
    end if;
  -- Registering outputs
      sclk <= not sclk_int;
      sout <= sout_sr(11);
    sync_n <= sync_n_int;
  end if;
end process data_proc;
dac_wr_done <= dac_wr_done_sr(31);
-------------------------------------------------------------------------------

end architecture rtl;
```

ADC_TOP CODE:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity adc_top is
  port ( mclk : in std_logic;
         rst : in std_logic;
       -- Interfacing signal to ADC084S085
         adc_sclk : out std_logic;
         adc_cs_n : out std_logic;
         adc_sout : out std_logic;
          adc_sin : in  std_logic;
         data_valid : out  std_logic;

        --
        ch0 : out std_logic_vector(7 downto 0);
        ch1 : out std_logic_vector(7 downto 0)
        );
end entity adc_top;

architecture str of adc_top is

component dac084s085_interface
  port (-- Global Clock and Reset
         mclk : in std_logic;
         mrst : in std_logic;
        -- Interface signals to module interacting with DAC
            dac_data : in  std_logic_vector(7 downto 0);
              dac_ch : in  std_logic_vector(1 downto 0);
             dac_cmd : in  std_logic_vector(1 downto 0);
              dac_wr : in  std_logic;
         dac_wr_done : out std_logic;
        -- Interfacing signal to DAC084S085
           sclk : out std_logic;
         sync_n : out std_logic;
           sout : out std_logic
       );
end component;

component adc084s021_interface
  port (-- Global Clock and Reset
         mclk : in std_logic;
         mrst : in std_logic;
        -- Interface signals to module interacting with ADC
               adc_data : out std_logic_vector(7 downto 0);
         adc_data_valid : out std_logic;
                 adc_ch : in  std_logic_vector(1 downto 0);
              adc_rd_en : in  std_logic;
        -- Interfacing signal to ADC084S085
         sclk : out std_logic;
         cs_n : out std_logic;
         sout : out std_logic;
          sin : in  std_logic
       );
end component;

signal adc_data : std_logic_vector(7 downto 0) := (others => '0');
signal adc_data_ch0 : std_logic_vector(7 downto 0) := (others => '0');
signal adc_data_ch1 : std_logic_vector(7 downto 0) := (others => '0');
```

```
signal adc_data_valid : std_logic := '0';
signal adc_rd_en : std_logic;
signal adc_channel : std_logic_vector(1 downto 0) := "00";


begin


inst_adc084s021_interface : adc084s021_interface port map (
            mclk => mclk,
            mrst => rst,
        adc_data => adc_data,
  adc_data_valid => adc_data_valid,
         adc_ch => adc_channel,
      adc_rd_en => adc_rd_en,
           sin => adc_sin,
            sclk => adc_sclk,
            cs_n => adc_cs_n,
            sout => adc_sout
  );



adc_read_proc: process (mclk) begin
  if rising_edge(mclk) then
    if (rst = '1') then
      adc_rd_en <= '1';
    else
      adc_rd_en <= adc_data_valid;
    end if;

    if (adc_data_valid = '1') then
            if (adc_channel = "00") then
            adc_data_ch0 <=  adc_data;
            adc_channel <= "01";
            elsif (adc_channel = "01") then
             adc_data_ch1 <=  adc_data;
              adc_channel <= "00";
              end if;
              end if;


data_valid<= adc_data_valid;
end if;


end process adc_read_proc;
   ch0 <= adc_data_ch1;
   ch1 <= adc_data_ch0;

end architecture str;
```

ADC INTERFACE:

```
library ieee;
use ieee.std_logic_1164.all;

-------------------------------------------------------------------------------
entity adc084s021_interface is
  port (-- Global Clock and Reset
         mclk : in std_logic;
         mrst : in std_logic;
        -- Interface signals to module interacting with ADC
               adc_data : out std_logic_vector(7 downto 0);
         adc_data_valid : out std_logic;
                 adc_ch : in  std_logic_vector(1 downto 0);
             adc_rd_en : in  std_logic;
        -- Interfacing signal to ADC084S085
         sclk : out std_logic;
         cs_n : out std_logic;
         sout : out std_logic;
          sin : in  std_logic
       );
end entity adc084s021_interface;
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
architecture rtl of adc084s021_interface is

-------------------------------------------------------------------------------
--
-- Format of Data Input to ADC
--
--  |07| |06| |05| |04| |03| |02| |01| |00|
--
--  7 to 6 and 2 to 0 => Dont Care
--  5 => ADD2 -> Dont Care
--  4 & 3 -> selects input channel
--  00 -> IN1 (default)
--  01 -> IN2
--  10 -> IN3
--  11 -> IN4
--
--  Next 8 bits Dont Care
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
--
-- Format of Data Output of ADC
--
--  |15| |14| |13| |12| |11| |10| |09| |08| |07| |06| |05| |04| |03| |02| |01| |00|
--
--  15 to 12 => High Impedence - Dont Care
--
--  11 to 4 => Data output of ADC. MSB First
--
--  3 to 0 => Zeros - Dont Care
--
-------------------------------------------------------------------------------

-- ADC MAX Clock Rate is 3.2 MHz. Here it is set to 2.5 MHz
signal clk_en : std_logic_vector(7 downto 0) := "00000001";
signal sclk_int : std_logic := '1';
signal cs_n_int : std_logic := '1';
```

```
signal cs_n_int_sr : std_logic_vector(4 downto 0) := (others => '1');

signal sout_sr : std_logic_vector( 5 downto 0) := (others => '0');
signal  sin_sr : std_logic_vector(15 downto 0) := (others => '0');

signal   adc_rd_en_reg : std_logic := '0';
signal     adc_rd_busy : std_logic := '0';
signal adc_rd_valid_sr : std_logic_vector(16 downto 0) := (others => '0');


begin

--------------------------------------------------------------------------------
--data_proc:
--------------------------------------------------------------------------------
data_proc: process(mclk) begin
  if rising_edge(mclk) then
    --
    if (adc_rd_busy = '1') then
      adc_rd_en_reg <= '0';
    elsif (adc_rd_en = '1') then
      adc_rd_en_reg <= '1';
    end if;
    --
    if ((mrst or adc_rd_valid_sr(16)) = '1') then
      adc_rd_busy <= '0';
    elsif (((adc_rd_en or adc_rd_en_reg) and (clk_en(7) and (not sclk_int))) = '1')
then
      adc_rd_busy <= '1';
    end if;
    --
    if (((clk_en(7) and (not sclk_int)) or adc_rd_valid_sr(16)) = '1') then
      adc_rd_valid_sr <= adc_rd_valid_sr(15 downto 0) & (adc_rd_en or adc_rd_en_reg);
    end if;
    --
    if (mrst = '1') then
      cs_n_int <= '1';
       sout_sr <= "0000" & adc_ch;
    elsif (((adc_rd_en or adc_rd_en_reg) and (clk_en(7) and (not sclk_int))) = '1')
then
       sout_sr <= "0000" & adc_ch;
      cs_n_int <= '0';
    elsif(adc_rd_valid_sr(16) = '1') then
      cs_n_int <= '1';
    elsif ((clk_en(7) and sclk_int and adc_rd_busy) = '1') then
       sout_sr <= sout_sr(4 downto 0) & '0';
      cs_n_int <= '0';
    end if;
    --
    if ((adc_rd_busy and clk_en(2) and sclk_int) = '1') then
      sin_sr <= sin_sr(14 downto 0) & sin;
    end if;
    --
    cs_n_int_sr <= cs_n_int_sr(3 downto 0) & cs_n_int;
    cs_n <= cs_n_int_sr(4);
    sclk <= sclk_int;
    sout <= sout_sr(5);
    --
    if (adc_rd_valid_sr(16) = '1') then
      adc_data <= sin_sr(10 downto 3);
      adc_data_valid <= '1';
    else
      adc_data_valid <= '0';
```

```
    end if;
  end if;
end process data_proc;
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
-- sclk_proc: generates 2.5 MHz serial clock 50/50 Duty Cycle
-------------------------------------------------------------------------------
sclk_proc: process (mclk) begin
  if rising_edge(mclk) then
    clk_en <= clk_en(6 downto 0) & clk_en(7);
    if (mrst = '1') then
      sclk_int <= '1';
    elsif (clk_en(7) = '1') then
      sclk_int <= not sclk_int;
    end if;
  end if;
end process sclk_proc;
-------------------------------------------------------------------------------

end architecture rtl;
-------------------------------------------------------------------------------
```

ANALOG MULTIPLEXER 1ST SET:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all ;

entity mux1 is
    Port (
           clk : in std_logic;
           data_in : in std_logic_vector(7 downto 0);
           v_a : out std_logic_vector(7 downto 0);
           v_b : out std_logic_vector(7 downto 0);
           v_c : out std_logic_vector(7 downto 0);
           il_a : out std_logic_vector(7 downto 0);
           il_b : out std_logic_vector(7 downto 0);


           cntr1 : out std_logic_vector(2 downto 0)
           );
end mux1;

architecture Behavioral of mux1 is
signal cntr : std_logic_vector(2 downto 0):= "000";
signal data : std_logic_vector(7 downto 0) := (others => '0');
constant const : std_logic_vector(3 downto 0) := "0000";

begin
process(clk)

begin
 if rising_edge(clk) then
 if( cntr = "000") then
           il_b<= data_in;
           cntr<= "001";
        elsif( cntr = "001") then
           v_a<= data_in;
           cntr<= "010";
        elsif( cntr = "010") then
           v_b<= data_in;
           cntr<= "011";
        elsif( cntr = "011") then
           v_c<= data_in;
           cntr<= "100";
        elsif( cntr = "100") then
           il_a<= data_in;
           cntr<= "000";

         end if;
         cntr1 <= cntr;
end if;
end process;

end Behavioral;
```

ANALOG MULTIPLEXER 2ND SET:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all ;

entity mux2 is
    Port (
            clk : in std_logic;
            data_in1 : in std_logic_vector(7 downto 0);
            il_c : out std_logic_vector(7 downto 0);
            iinj_a : out std_logic_vector(7 downto 0);
            iinj_b : out std_logic_vector(7 downto 0);
             iinj_c : out std_logic_vector(7 downto 0);

            cnt1 : out std_logic_vector(2 downto 0)
            );
end mux2;

architecture Behavioral of mux2 is
signal cnt : std_logic_vector(2 downto 0):= "000";
signal data : std_logic_vector(7 downto 0) := (others => '0');
signal data2 : std_logic_vector(7 downto 0) := (others => '0');
constant const : std_logic_vector(3 downto 0) := "0000";

begin
process(clk)

begin
 if rising_edge(clk) then
 if( cnt = "000") then
            data2<= data_in1;
            cnt<= "001";
        elsif( cnt = "001") then
            il_c<= data_in1;
            cnt<= "010";
        elsif( cnt = "010") then
            iinj_a<= data_in1;
            cnt<= "011";
            elsif( cnt = "011") then
            iinj_b<= data_in1;
            cnt<= "100";
            elsif( cnt = "100") then
            iinj_c<= data_in1;
            cnt<= "000";


         end if;
         cnt1 <= cnt;
end if;
end process;

end Behavioral;
```

LOAD CONTROLLER CODE:

```
module algo(
input  mclk,
input reg[7:0]vl,
input reg[7:0]il,
input reg[7:0]vpv,
input reg[7:0]ipv,
input reg[7:0]rs,
input reg[7:0]pb,
input reg[7:0]vb,
output reg[7:0]y
) ;

 assign reg[7:0]Pl=vl*il;
 assign reg[7:0]Ppv=vpv*ipv;
 assign reg[7:0]Pdfig=8'd20;
 assign reg[7:0]Ps=8'd23 ;
 assign reg[7:0]e=8'd3;
 assign reg [7:0]Vbmin= 8'd24;

 if(Pdfig > Pl)
  trip[0] = 1'd1;                    // trip[0]='1': addition of more loads
is possible.
  else
   begin
         if(Ppv-Ps > Pl-Pdfig)
         begin
            Ps=Ps+Pl-Pdfig;
            trip[0]=1'd1;
         end
         else
         begin
            Ps=Ppv;
            trip[1]=1'd1;          // trip[1]='1': operate statcom to
supply
            pb=Pl-Pdfig-Ps;
            if(Pb>e or vb<Vbmin)
            begin
               trip[3] = 1'd1;     //trip[3]='1': no more load can be
added
            end
              else
              begin
               trip[2]=1'd1;       //trip[2]='1': switch off low priority
load
               trip[3]=1'd1;
              end
         end

   end


   endmodule
```

Challenges faced and Lessons Learnt during the implementation of the project

1. Identifying manufacturers of low power wind turbines with wound rotor induction generator.

2. The proper field survey (assessment of wind and solar potential and nature of consumer load requirement) is essential for designing the proposed system with optimal sizing of the components. This will also ensure the reliable and continuous power supply to the consumers.

3. Lack of skilled technician/personnel has been the major bottleneck in the practical implementation of the proposed system.

4. Selection of suitable DC voltage level of the system. Higher DC voltage leads series connection of many solar panels and battery banks which is not preferable. If the DC voltage is less, then need of transformer at the output of the DSTATCOM is required. With less DC voltage, it is poor performance is experienced during the transfer of real and reactive power transfer through the inverter. This also restricts the operating speed range for the WRIG.

5. Design of sensors, suitable interface circuits and data acquisition system to feed the digital input to the FPGA controllers for the field implementation. Calibration plays a major role for designing such controller to be operated with intermittent nature of energy resources. The calibration takes several iterations and more time for validating its proper operation.

6. Lack of commercial availability of diesel engine coupled with squirrel cage induction generation.

7. Establishing a reliable communication for effective load and generator control.

8. NIT Tiruchirappalli being the educational institution will be ready to design and demonstrate the proof of concept through laboratory experimentation and simulation. However, for scaling up to the level of field implementation, an appropriate industry partner is mandatory. NIT Tiruchirappalli may offer the technical expertise learnt out of this project as consultancy services for field implementation.

9. NIT Tiruchirappalli would like to place on record that the Ph.D., M.Tech. and B.Tech. scholars who have contributed to this project have been placed in high profile companies/technical institutions.

10. Two Ph.D. and one M.Tech. theses based on this project have been awarded the prestigious POSOCO Power Systems Award.

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