STUDY AND CONTROL OF WEAK GRID CONNECTED MATRIX CONVERTER BASED DFIG SYSTEMS

PHASE -I

A REPORT - REVISED

Submitted to

NATIONAL INSTITUTE OF WIND ENERGY, CHENNAI

MINISTRY OF NEW AND RENEWABLE ENERGY, GOVERNMENT OF INDIA

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NOVEMBER 2016

ACKOWLEDGEMENT

We would like to express my deepest gratitude to the Centre of Wind Energy Technology (C-WET), Ministry of New and Renewable Energy, Government of India for funding the Project. Without the fund, it would not have been possible to carry out research in the developing area of Matrix Converters. This fund was very useful for PhD research of Dr. M. Senthil Kumaran (Project Co-Investigator) and about 10 M.E. and B.E. students. Our particular thanks to the **Dr. S. Gomathinayagam**, Executive Director of NIWE, **Mr. Rajesh Katyal**, Scientist and Unit Chief of NIWE, and all others in NIWE for all the help and service provided by them for the Project.

We would also like to thank **Dr. V. Kamaraj,** Professor & Head, Department of Electrical and Electronics Engineering (EEE), SSN College of Engineering, for his support and direction. Our special thanks to the **Management and the Principal** of SSN College of Engineering for providing the opportunity and all the help for completing the Project.

We greatly appreciate the help from the faculty, students and non-teaching staff of the Department of Electrical and Electronics Engineering for their support for this Project.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbols

d_{ij}	-	Duty cycle of the switch
f_i	-	Input frequency
f_o	-	Output frequency
Fs	-	Sampling frequency
I	-	Current
μ	-	Modulation function
P	-	Power
P	-	Number of poles
φ_i	-	Input power factor
φ_o	-	Output power factor
Ψ	-	Flux
S_{ij}	-	Switch function
T	-	Torque
T_s	-	Sampling time
V	-	Voltage

Abbreviations

AC	-	Alternating Current
ADC	-	Analog to Digital Converter
CMC	-	Conventional Matrix Converter
DC	-	Direct Current
FPGA	-	Field Programmable Gate Array
IGBT	-	Insulated Gate Bipolar Transistor
MI	-	Modulation Index
PWM	-	Pulse Width Modulation
RSVM	-	Rotating Space Vector Modulation
THD	-	Total Harmonic Distortion
VHDL	-	Very high speed integrated circuit Hardware Description Language
VFD	-	Variable frequency Drive

Study and Control of Weak Grid Connected Matrix Converter based DFIG System

PHASE - I

DELIVERABLES

S.No.	Project Phase	Time frame (Months)	Deliverables	Chapter
1	I	6^{th}	1. Simulation Results of MATRIX Converter Controlled DFIG Systems 2. Hardware power module development	1, 2 &4 10
2	I	12^{th}	1. Complete hardware development of power module. (Driver Circuit, FPGA and DSP interfacing). 2. Motor - Generator set and interface with Power converter setup	10 3 & 10
3	I	18^{th}	1. Simulation of VHDL and DSP Coding 2. Hardware implementation of Space Vector coding. 3. Submission of Hardware Results	5 , 6 , 7, 8 & 9 10

CHAPTER 1

DIRECT AC TO AC CONVERTER FOR VARIABLE SPEED WIND ENERGY SYSTEMS

1.1 INTRODUCTION

Variable-speed wind turbines are gaining more prominence due to their ability to generate power for a wide range of wind speeds. This class of turbines requires a fraction of the power to be drawn from the grid in order to compensate for the deficiency in the wind speed below the synchronous speed. Conventionally a Doubly-Fed Induction Generator (DFIG) with a bidirectional converter (AC-DC-AC) in the rotor side is employed, as shown in Figure 1.1.

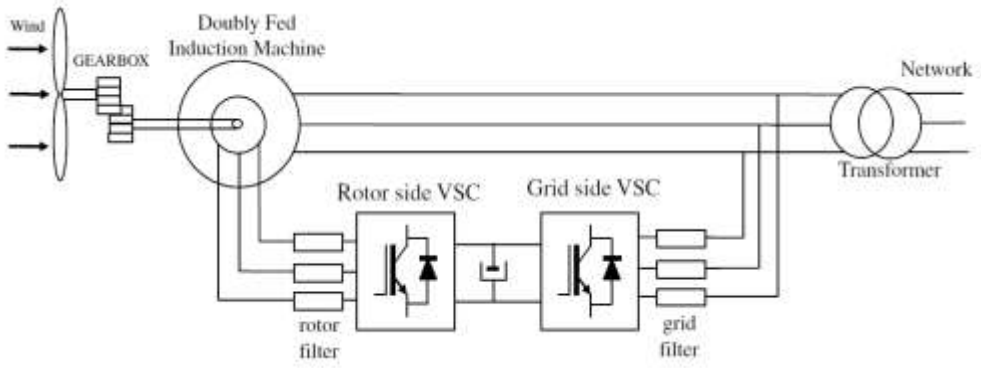


Figure 1.1 Conventional variable speed wind energy conversion system

The back-to-back converter controls the flow of energy from the machine to the grid as well as the energy drawn by the rotor in order to sustain the power generation. The grid-side and the rotor-side converters have different degrees of freedom due to the presence of the DC-link capacitor.

1.2 GRID SIDE CONTROL

The grid-side converter exchanges the active power extracted or injected by the rotor side converter with the grid and maintains the DC-link voltage constant. Figure 1.2 shows the block diagram for the control of the grid-side converter and Figure 1.3 presents the control scheme. The pulses for the controlled switches (S_{a_g}, S_{b_g}, S_{c_g}) of the two-level VSC, which is function of the output voltage of the converter, are generated in order to control the DC bus voltage (V_{bus}).

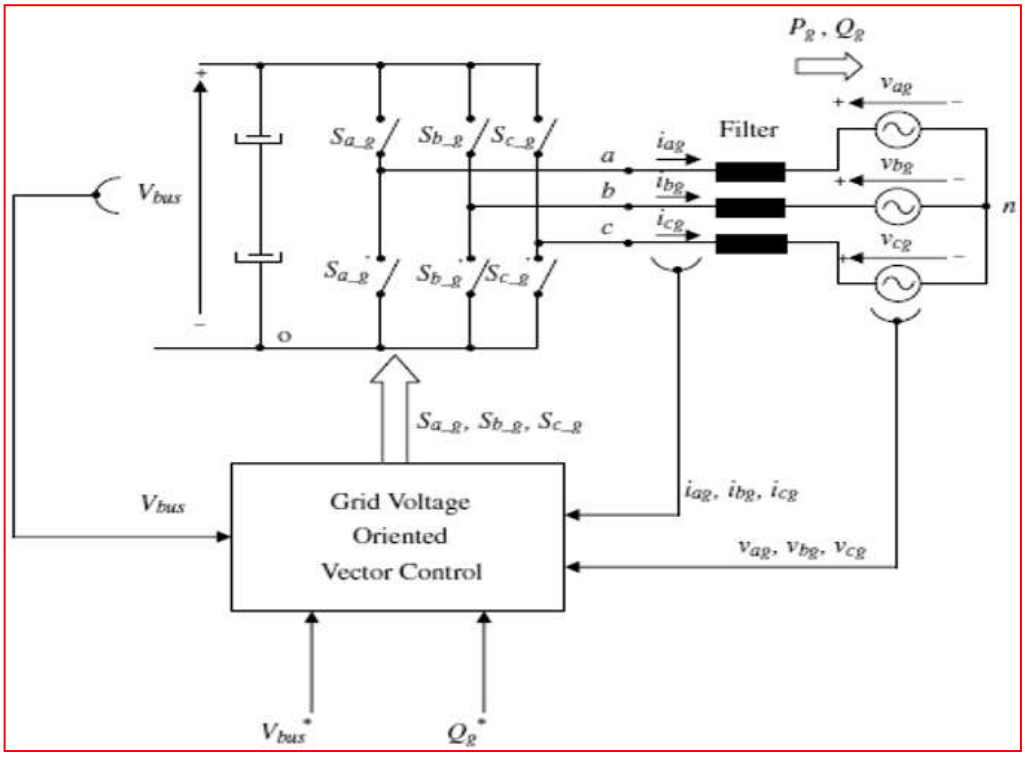


Figure 1.2 Grid side control scheme for the conventional back-to-back converter

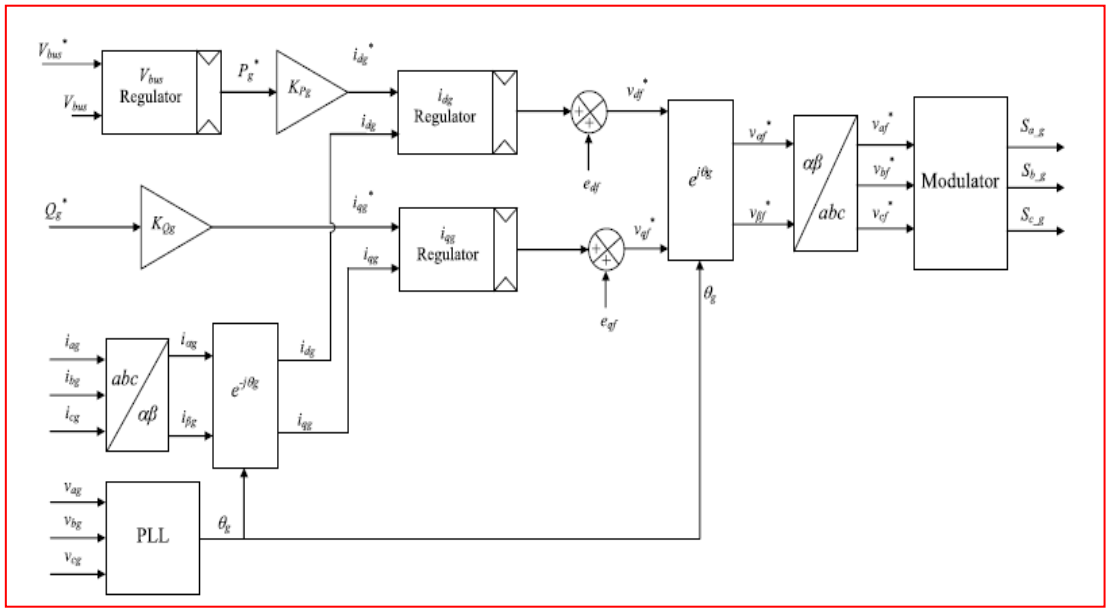


Figure 1.3 Grid voltage oriented vector control scheme for the grid side controller

1.3 ROTOR SIDE CONTROL

The rotor side converter generates a three-phase voltage with variable amplitude and variable frequency in order to control the generator torque and the power exchanged between the stator and the grid. Figure 1.4 gives the block diagram of the rotor side control scheme.

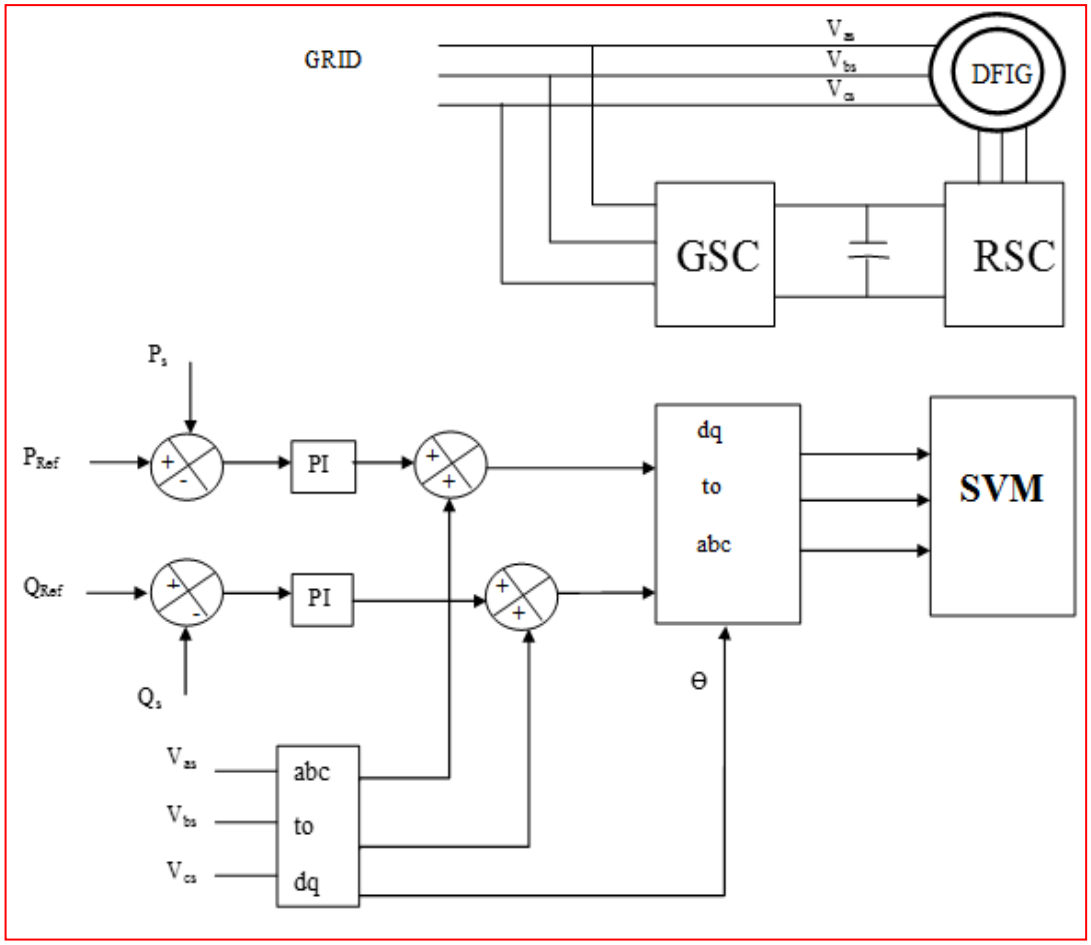


Figure 1.4 Rotor side control scheme for the conventional back-to-back converter

1.4 NEED FOR DIRECT AC-TO-AC CONVERTER

The basic function of a power converter in the variable speed wind energy conversion system (WECS) is to process the energy using the power switches. AC power conversion can be classified as (i) direct AC-to-AC power conversion and (ii) indirect AC-to-DC-to-AC power conversion. At present, voltage source back-to-back converters (AC-DC-AC) are widely used in the AC conversion systems. These converters require bulky storage electrolytic capacitors. The operation of these converter stages (stage-1: AC-DC) and (stage-2: DC-AC) is controlled independently since they are decoupled by means of an energy storage element. Therefore, the instantaneous input power need not be equal to the instantaneous output power. The difference between the instantaneous input power and the instantaneous output power is absorbed or

delivered by an energy storage element within the converter. The storage element is the bulky storage electrolytic capacitor prone to poor performance at high temperatures and susceptible to failures (Hitachi inverter instruction manual). Therefore, the use of the storage capacitor not only increases the system weight and volume, but also reduces the reliability of the system.

In this project, the conventional back-to-back converter is replaced with a direct AC-to-AC converter, thereby eliminating the energy storage element (DC-link) and its associated control.

1.5 STATE-OF-THE-ART REVIEW OF THE THREE-PHASE AC-TO-AC CONVERTER

Figure 1.5 shows the classification of the direct AC-to-AC converter into three distinct topological approaches. The first approach is the AC voltage regulator that changes the amplitude of the AC waveform (Hashem & Darwish 2004). The second approach is the cyclo-converter, which is used if the required output frequency (Maamoun 2003) is much lower than the input source frequency. The third approach is the matrix converter, which is the most versatile and has no limits on the output frequency and the amplitude. In other words, the input may be three-phase AC and the output DC, both may be DC, or both may be AC (Mohan et al 2003).

Therefore, the matrix converter topology is promising for the universal power conversion, such as the AC-to-DC, DC-to-AC, DC-to-DC and the AC-to-AC. The matrix converter offers some significant advantages such as the adjustable power factor, inherent four-quadrant operation, high quality sinusoidal input/output waveforms and high power density. Hence, it has received extensive attention in research as a replacement for the traditional AC-DC-AC converter for variable-voltage and variable-frequency AC drive applications.

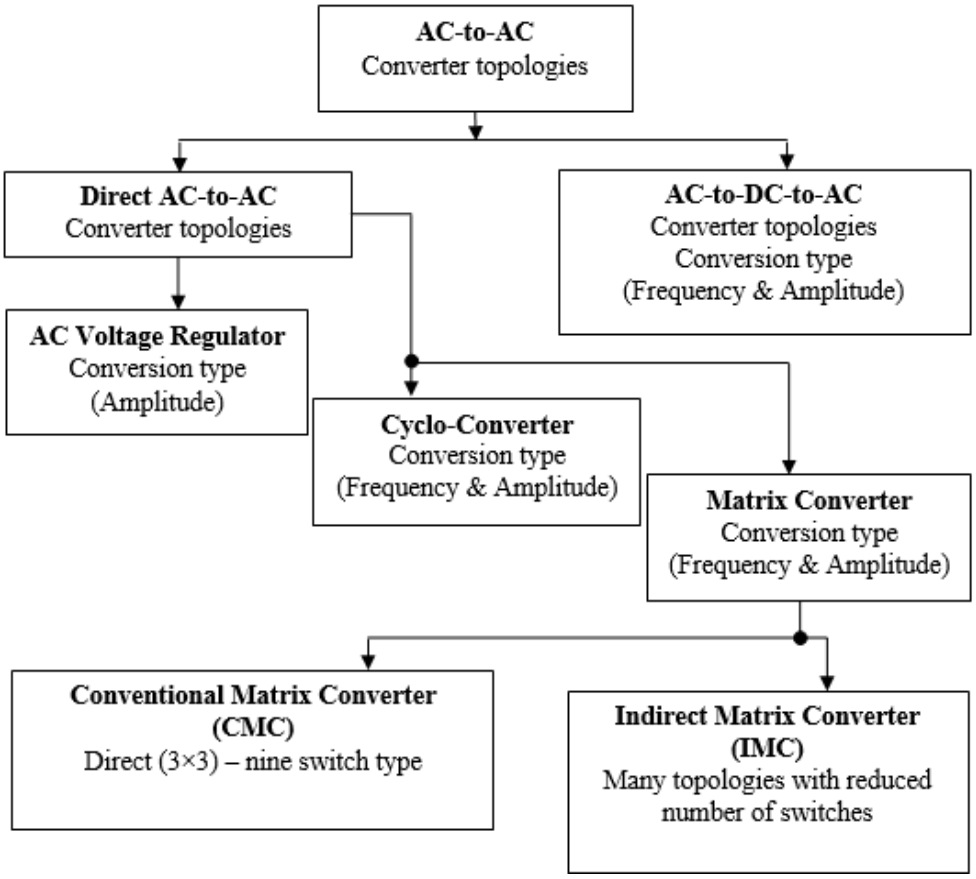


Figure 1.5 AC-to-AC converter topologies

1.6 STRUCTURE OF THE MATRIX CONVERTER

The matrix converter is the force-commutated version of the cyclo-converters (Huber & Borojevic 1989), which overcomes the disadvantage of the conventional cyclo-converter such as the limitations in the frequency conversion, rich output voltage harmonics and increased number of switches (Rashid 2005 and Fa-Hai Li et al 1994). The matrix converters can be classified as direct and indirect type matrix converters. Figure 1.6 shows the direct or the conventional matrix converter (CMC) that is an array of 3×3 bidirectional switches. The indirect or the sparse matrix converter is the cascade of the controlled rectifier and the inverter topologies without the DC-link in between (Ziogas et al 1986). Both the topologies directly interconnect two independent multi-phase voltage systems at different frequencies. In this research, the CMC topology is chosen and is analyzed for changes in its topology with different pulse width modulation (PWM) techniques.

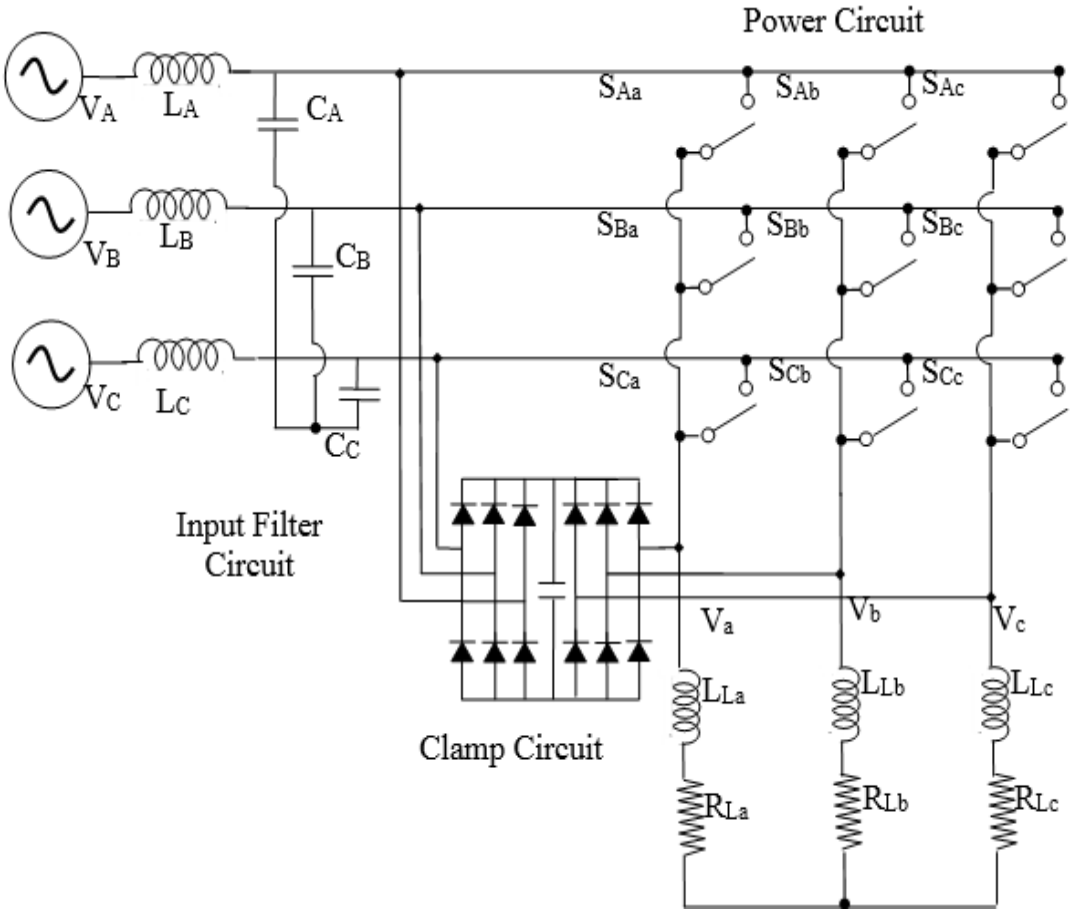


Figure 1.6 Structure of the conventional matrix converter

The matrix converter is connected to a stiff voltage source at the input and a stiff current source at the output. These externally connected voltage and current sources impose constraints on the switching of the matrix converter. At any instant, the voltage source should not be short-circuited and the current source should not be open circuited. Equation (1.1) gives the switching function of the switch S_{ij} in Figure 1.6.

$$S_{ij}(t)=1,\ S_{ij}=\text{closed}$$

$$S_{ij}(t)=0,\ S_{ij}=\text{open},\quad \text{where } i\in\{A,B,C\}\ \&\ j\in\{a,b,c\} \qquad (1.1)$$

Equation (1.2) gives the constraints namely that the inputs are not short-circuited and the outputs are not open-circuited

$$d_{Aj}+d_{Bj}+d_{Cj}=1 \tag{1.2}$$

where, d_{ij} is the duty-cycle of the switch S_{ij}. Equation (1.2) being less than one indicates an open-circuit of the current source and Equation (1.2) being greater than one indicates a short-circuit of the voltage source.

Therefore, Equations (1.3) and (1.4) represents the switching function T of the matrix converter for the output voltages and the input currents

$$V_{out} = T \times V_{in}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \times \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{1.3}$$

where,

$$V_{out}= \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix},\ T= \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \text{ and } V_{in}= \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

$$I_{in} = T^T \times I_{out}$$

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \times \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{1.4}$$

where,

$$I_{in}= \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix},\ T^T= \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \text{ and } I_{out}= \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}.$$

and V_A, V_B, V_C and V_a, V_b, V_c are the input and the output phase voltages respectively and I_A, I_B, I_C and I_a, I_b, I_c are the input and the output currents respectively.

1.6.1 Basic Components of a Practical Matrix Converter

Figure 1.6 shows the design of a practical matrix converter circuit, which involves the development of three essential circuits (i) the power circuit, (ii) the input filter circuit and (iii) the clamp circuit.

Figure 1.6 shows the power circuit consisting nine bi-directional switches with 2^9 (512) possible switching states. However, only 27 switching states are used because of the limitations imposed on the power circuit by the Equation (1.2).

The input filter is necessary to reduce the switching harmonics in the input currents (Wheeler et al 2002a). Figure 6 shows the input filter consisting of the source inductances L_A, L_B, L_C and the source capacitors C_A, C_B, C_C.

The interruption of the inductive current during commutations leads to high voltage spikes appearing across the switches. These high voltage spikes damage the switches, and therefore a clamp circuit, shown in Figure 1.6, is required to store the inductive energy (Klumpner and Blaabjerg 2002). The clamp circuit transfers the inductive energy from the load to the clamp capacitor during the turning OFF the converter.

1.6.2 Bidirectional Switch Configurations

The power electronics realization of the matrix converter in Figure 1.6 requires four quadrant bidirectional switches. Due to the lack of semiconductor devices capable of operating in four quadrants, a four-quadrant switch is constructed from two two-quadrant switches (Dynex Semiconductor 2007), as shown in Figure 1.7.

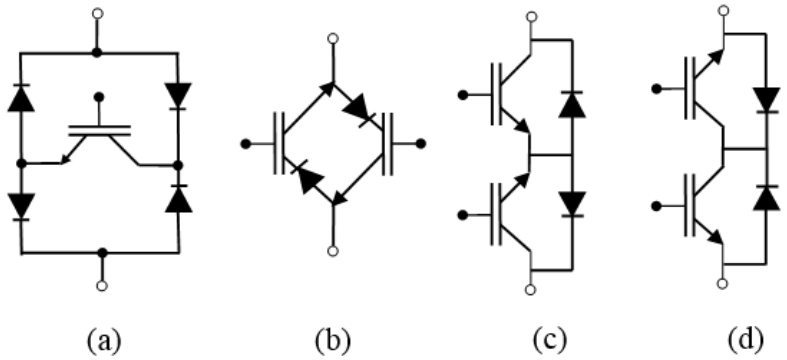


Figure 1.7 Four-quadrant bidirectional switches (a) diode-embedded switch (b) reverse blocking IGBT (c) common emitter IGBT and (d) common collector IGBT

The main advantage of the diode-embedded switch is its simple configuration when compared to other bi-directional switch structures, but the main disadvantage of this configuration is the high conduction loss. The other configurations have lower conduction losses than the diode-embedded switch. The reverse blocking IGBTs are not often used as bidirectional switches since, in practice, the IGBT has poor reverse recovery characteristics that increases the switching losses and hence the overall system efficiency decreases. Amongst the other two configurations, the common emitter configuration is widely used for high power applications (Semikron-SK60GM123 2007). Common collector configuration, although requiring a reduced number of isolated power supplies for generating the switching signals is not much preferred for high power applications (Imayavaramban 2008).

1.7 COMMUTATION TECHNIQUES FOR THE MATRIX CONVERTERS

With the constraints imposed on the matrix converter, as explained in Equation (1.2), it is found that each output phase of the matrix converter must always be connected to one and only one input phase even during the commutation. Since the matrix converter does not have an inherent freewheeling path, the commutation of its bidirectional switches is much more difficult than the commutation of switches in an inverter.

Various commutation techniques have been proposed for matrix converters namely (i) the dead-time commutation, (ii) the soft switching technique, (iii) the multi-step current commutation and (iv) the multi-step voltage commutation.

The implementation of the dead-time commutation in matrix converters leads to the interruption of inductive currents due to the absence of a freewheeling path. Use of such technique in matrix converters requires snubber circuits to provide an alternate path to the inductive currents (Sunter and Clare 1996), which increases the complexity and the size of the converters.

Soft switching techniques have been investigated in many converter topologies for reducing the switching losses. However, the implementation of soft switching techniques in matrix converters (Marcks 1995) increases the component count and complexity of the converters.

At present, the most popular methods of commutation are the multi-step current and multi-step voltage commutations. The idea of such multi-step commutations techniques first appeared in Oyama et al (1989) and Burany (1989).

1.7.1 The Four-Step Current Commutation

To determine the commutation sequence, this method relies on the direction of the load current. The bidirectional switch (BS) that will stop conducting after the commutation is known as the outgoing BS and the BS that will start conducting after the commutation is known as the incoming BS. Each BS consists of two switches, named as S^+ and S^-, indicates the direction of the current flow through the respective switches.

Before the commutation process starts, both the switches S^+, S^- of the outgoing BS are ON. With this condition, the safe commutation sequence of the BS to transfer the load current from one phase to another phase is explained below.

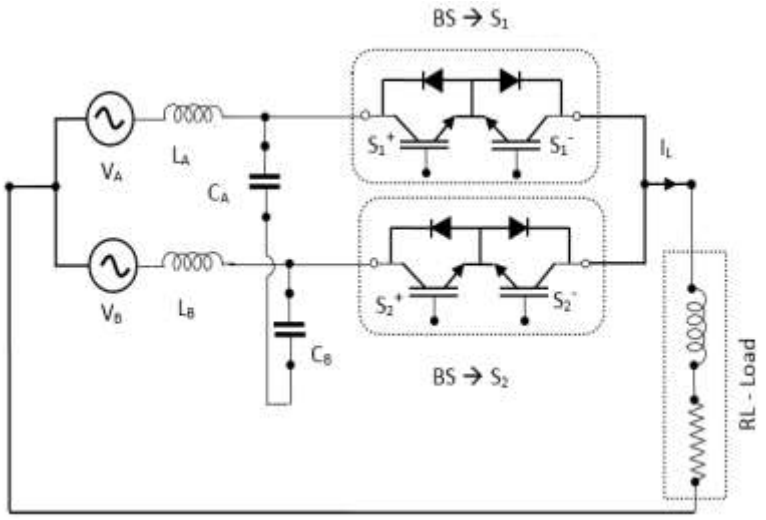


Figure 1.8 Commutation of the bidirectional switches between the two input phases

Step 1 **:** When the commutation to an incoming BS is required, the current direction is used to determine the non-conducting switch in the outgoing BS. This switch is first turned OFF.

Step 2 **:** Then, the switch in the incoming BS that would conduct the current in the same direction is turned ON. This is done to form a path for the load current to continue flowing either at the point when the next switch of the incoming BS is gated ON or when the conducting switch of the outgoing BS is turned OFF.

Step 3 **:** The conducting switch of the outgoing BS can now be turned OFF safely, since a new path is made available for the current to flow as in Step 2.

Step 4 **:** Finally, the other switch of the incoming BS is switched ON to complete the sequence of commutation.

For Example, in the Figure 1.8, when the $i_L > 0$,

(i) Switch S_1^- is turned OFF, (ii) Switch S_2^+ is turned ON, (iii) Switch S_1^+ is turned OFF, and (iv) Switch S_2^- is turned ON.

Similarly, the four-step current commutation sequence of switching can be formulated for other cases and is given in Figure 1.9.

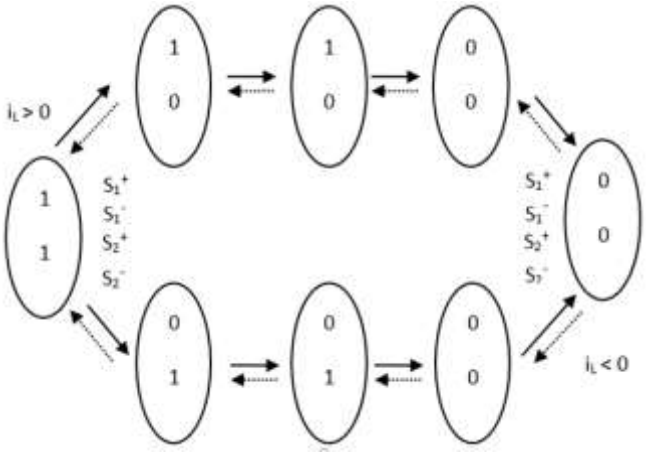


Figure 1.9 State diagram of the four-step current commutation

Since the commonly used Hall effect sensors are prone to produce uncertain results in high power and low current applications, as it is difficult to reliably determine the direction of current for commutation. To avoid this problem, a technique named as voltage commutation that uses the voltage across the bidirectional switch for measurement of the direction of current (Wheeler et al 2002b) has been developed. Later, a technique utilizing the zero vectors (Mahlein et al 2002) to avoid commutation error, when the line voltage is zero, was proposed for robust commutation. However, the input current in this technique was found distorted compared to the voltage and current commutation techniques because of utilizing a different switching sequence.

1.8 MODULATION TECHNIQUES FOR THE MATRIX CONVERTERS

Several modulation algorithms are reported for matrix converters in Wheeler (2002a) to achieve different control objectives; basic classifications of these modulation techniques are shown in Figure 1.10.

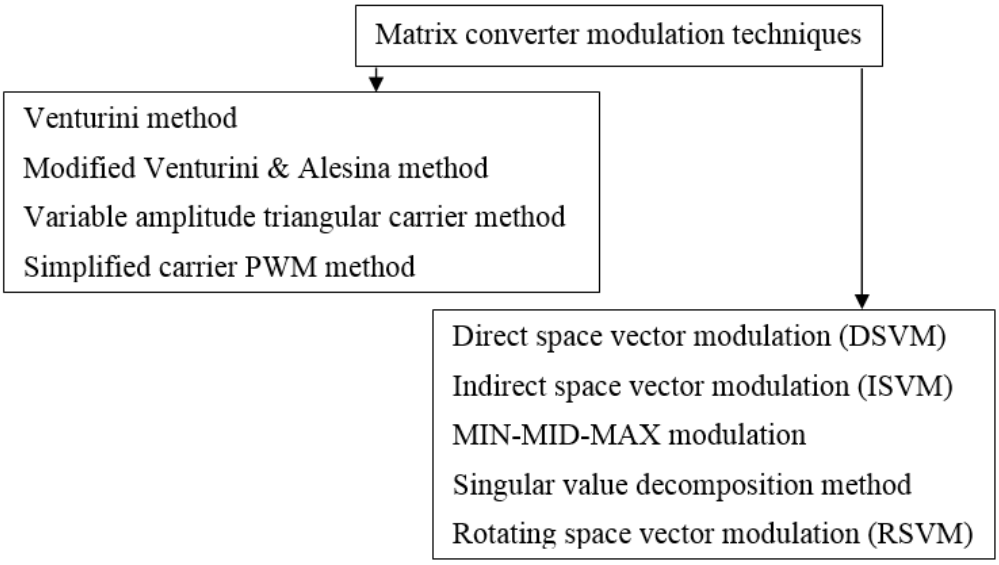


Figure 1.10 Classification of the matrix converter modulation techniques

The development of this converter and its modulation techniques started three decades back based on the complex mathematical formulation by Venturini and Alesina (1980) with the voltage transfer ratio of 0.5. Later, the Optimum Alesina Venturini (OAV) method (Alesena and Venturini 1989) was proposed, in which the modulation index was extended from 0.5 to 0.866 by using the third harmonic injection technique. It was also proved that the modulation index of 0.866 is the physical limitation for the matrix converter. The carrier based PWM technique with varying amplitude triangular carrier was proposed by Yoon and Sul (2006). Later, Thuta (2007) proposed a simplified carrier PWM technique. The control technique for space vector control of the matrix converter was proposed by Huber and Borojevic (1995). Using the idea of the 'fictitious DC Link', a conceptually different idea (Casadei et al 2002), decoupled the control into smaller independent units. Researchers of the matrix converter now predominantly use this technique. The modulation algorithm like MAX-MID-MIN technique (Oyama et al 1989) use the relative magnitudes of the input line or phase voltages for generating the switching signals. Gupta et al (2010) proposed the use of rotating space vectors for synthesizing the required outputs of the matrix converter for the elimination of the common mode voltage in the matrix converter fed induction machines. A generalized technique for modelling, analysis and control of a matrix converter using the singular value decomposition method was proposed recently by

Hojabri et al (2011), which leads to a unified modulation technique that achieves the full capability for a matrix converter. In general, many of the modulation methods, established for the matrix converter, are specific cases of this technique.

1.9 CERTAIN ISSUES IN THE MATRIX CONVERTERS

1.9.1 Over Modulation Operation of the Matrix Converter

The over modulation operation has been described as a nonlinear operation (Holtz et al 1993) since the output waveform of the converter does not follow the original sinusoidal reference waveform in the regions of higher magnitudes. The over-modulation in the DC-link converters has been widely described in the literature (Bolognani and Zigliotto 1996) but only a few papers describe the detailed effects of over modulation operation of the matrix converter (Thuta 2007). The paper discusses four ways of operating the matrix converter under over modulation (i) output side over modulation, (ii) input side over modulation with power factor control, (iii) input side over modulation without power factor control and (iv) simultaneous output side and input side over modulation. Using the over modulation technique, the theoretical voltage limit of the converter can be increased to 105 % of the input voltage. It has been proved in Mahlein et al (1999) that some lower order harmonics are generated at the output voltage and the input current by the over modulation operation (Wiechmann et al 1997). Over modulation operation of the matrix converter might cause the resonance of the line side filter. This might damage the converter if not controlled properly. Thus, it was concluded in Wiechmann et al (2002) that it is not advisable to operate the matrix converter under over modulation for a long time, but for a short period, if demanded, for the ride-through operation.

1.9.2 Ride-Through Capability of the Matrix Converter

One of the desirable characteristics of a modern drive is its ride-through capability. This is a common solution for the drives during power loss. During ride-through, to magnetize the motor windings and to feed the control circuits, the drive utilizes the energy from the load inertia. This is achieved by maintaining a constant voltage in the DC-link

capacitor in the AC-DC-AC converters (Narayanan and Tanganathan 2002, Kim and Sul 2001 and Jounne et al 1999). However, the matrix converters are an array of controlled bidirectional switches without the DC-link capacitor and these are highly susceptible to voltage disturbances such as voltage sags, voltage swells and momentary power interruption. A new ride-through strategy for the matrix converter developed by Klumpner et al (2001) uses the zero vectors of the matrix converter and the clamp circuit to ride-through small interruptions. In Wiechmann et al (2002), an alternative strategy was presented that enables the converter to ride-through the voltage sags and enforce constant V/f operation with the minimum reduction in the speed. Later, a new approach was presented in Cha (2004) that modified the topology of the matrix converter with three additional unidirectional switches and a ride-through capacitor.

1.9.3 Unbalanced Operation and Control of the Matrix Converter

The effect of the unbalance on the converter performance is a vital aspect in determining the overall performance of the variable speed drive, which is fed by a converter. The matrix converter, being a direct frequency conversion system, the unbalance at the utility side is immediately reflected on the load side and generates unwanted lower order input/output harmonic currents (Enjeti and Wang 1990) that may resonate with the input filter causing damage to the converter, if uncontrolled. Therefore, research has been directed to investigate and compensate for these effects of input voltage disturbance. In Nielsen et al (1996), balanced and sinusoidal output voltages were produced even when the input voltages were unbalanced. In Casadei et al (1998) and Blaabjerg et al (2002), the input current harmonic content and the limits of the voltage transfer ratio of matrix converter under unbalanced conditions were determined analytically for different operating conditions. In Zhang et al (2001) and Sunter et al (2002), the line side voltage conditions with high order voltage harmonic components are analyzed. However, it was concluded in all these techniques that the input current harmonics could not be reduced when compensated for the output harmonics under abnormal conditions of the input voltage.

1.9.4 Common Mode Effects of the Matrix Converter

The high frequency common mode voltage generated in the power converters is reported to cause potential damage to the shaft and the bearings of the electric motors. The reduction of the common mode voltage in matrix converters using proper switching sequence has been reported in Nguyen and Lee (2012) and Cha and Enjeti (2003). Recently, Gupta et al (2010) presented the elimination of the common mode voltage in the matrix converter fed open-ended induction machine.

1.10 REVIEW OF THE MATRIX CONVERTER APPLICATIONS

Neft and Schauder (1992) experimentally confirmed that a matrix converter with only nine switches can be effectively used in the vector control of an induction motor with high quality input and output currents. The compactness of the matrix converter suggested the possibility of integrating the converter and the motor in a single unit, in order to reduce the cost and increase the overall efficiency (Klumpner et al 2002, Itoh et al 2005). Casadai et al (2001) used the matrix converter in the direct torque control (DTC) of the induction machines. Podlesak et al (2005) presented the field oriented-control of the matrix converter fed induction machine.

Matrix converters find their application in the field of wind power generation in full power converter topologies and partial converter topologies for the doubly fed induction generator control (Zhang et al 1997 and Lie Xu & Cartwright 2006). Research on modelling and analysis of the matrix converter based wind energy systems was carried out in Barakathi (2008). Control of the reactive power supplied by a WECS based on the induction generator fed by a matrix converter was presented in Cardenas et al (2009). An increasing number of papers (Imayavaramban & Wheeler 2007, Wheeler et al 2003 and Lillo 2006) investigating the advantages/ limitations of the use of matrix converters in aircrafts are also being reported.

Today, research in matrix converter is in the advanced technology and the application issues such as the reliable implementation of the modified topologies, operation under abnormal conditions and the design of matrix converter for control of machines with more number of phases. However, industrial applications of the converter are still limited because of some

practical issues such as difficulty in implementing complex switching methods, common mode voltage effects, high susceptibility to input power disturbances and low voltage transfer ratio.

1.11 OBJECTIVES

The main objectives of this project work are as follows:

(i) To study, develop and simulate the switching control technique for the matrix converter –simulation in Matlab / Simulink environment.

(ii) Parameter estimation for the DFIG used for prototype development.

(iii) To study, develop and simulate the control strategy for stator power for DFIG and integrate the matrix converter and stator power controller with the DFIG – simulation in Matlab / Simulink environment.

(iv) Generation of the VHDL code for the switching algorithm of the matrix converter using System Generator-Matlab (interface).

(v) Generation of the VHDL code for the stator power controller using the System Generator- Matlab (interface).

(vi) Design and generation of the VHDL code for peripherals (ADC, speed sensing, ZCD (current reference generation)) using the System Generator- Matlab (interface).

(vii) Development of the hardware prototype – testing and validation.

CHAPTER 2

DIRECT SPACE VECTOR MODULATION TECHNIQUE FOR MATRIX CONVERTER

The Space Vector Modulation (SVM) techniques are the extension of the theory of flux in multi-phase rotating machines (Bose 2004) to the field of static power converters. Space Vector PWM (SVPWM) techniques are well known for the Voltage Source Inverters (VSI). The idea of Direct Space Vector Modulation (DSVM) for the matrix converter, unified representation of the current and the voltage space vectors is presented.

2.1 INTRODUCTION TO DSVM

Let us assume that the MC input phase voltages are given by Equation (2.1) and the reference input currents are given by Equation (2.2).

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = V_m \begin{bmatrix} \sin \omega_i t \\ \sin\left(\omega_i t - \frac{2\pi}{3}\right) \\ \sin\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = I_m \begin{bmatrix} \sin(\omega_i t - \varphi_i) \\ \sin\left(\omega_i t - \frac{2\pi}{3} - \varphi_i\right) \\ \sin\left(\omega_i t + \frac{2\pi}{3} - \varphi_i\right) \end{bmatrix} \tag{2.2}$$

where, v_j and i_k are the input phase voltages and currents respectively, ω_i is the frequency of the input system, V_m and I_m are the peak values of the input voltages and currents respectively, and φ_i is the input phase angle.

In an output αβ reference frame, the instantaneous voltage space vector of the output is given by Equation (2.3). In an input αβ reference frame, the instantaneous current space vector is given by Equation (2.4).

$$\overrightarrow{V_o} = \frac{2}{3}(v_{AB} + a v_{BC} + a^2 v_{CA}) = V_o e^{j\alpha_o} \tag{2.3}$$

$$\vec{I_i} = \frac{2}{3}(i_a + a i_b + a^2 i_c) = I_i e^{j\beta_i} \tag{2.4}$$

where, $\alpha = e^{j2\pi/3}$, V_o and α_o are the amplitude and angle of the voltage vector and I_i and β_i are the amplitude and angle of the current space vector.

A switching state of the MC is defined as a condition where a set of switches is ON and the rest is OFF, subject to the constraints below, which are represented in Figure 2.1.

a. No two input terminals can be shorted at any instant of time.
b. No output terminal can be open circuited at any instant of time.

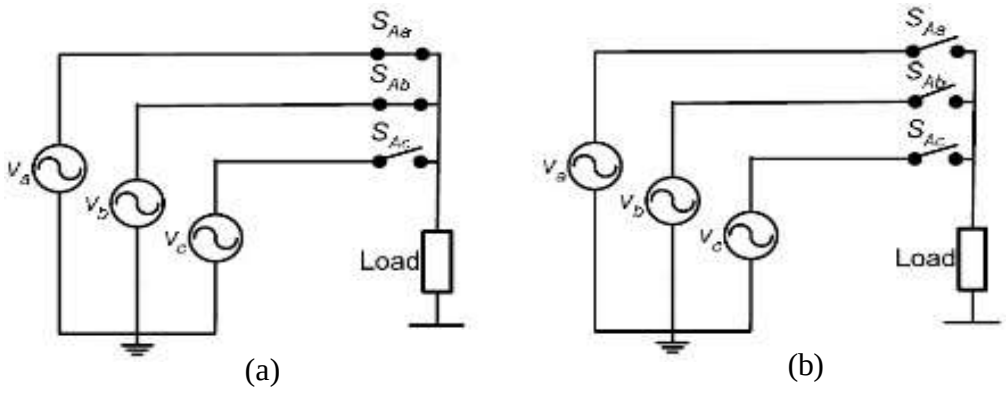


Figure 2.1 Non-Acceptable switch states in MC

Thus, each MC switching state represents a specific topology for connections between input and output terminals, that do not violate the above two constraints. For any switching state, we can express the output voltage and input current vectors by the instantaneous values of the input voltage and output current vectors respectively. An example is shown for a clear understanding of the computation of the space vectors. Consider the switch state [acc], shown in Figure 2.2.

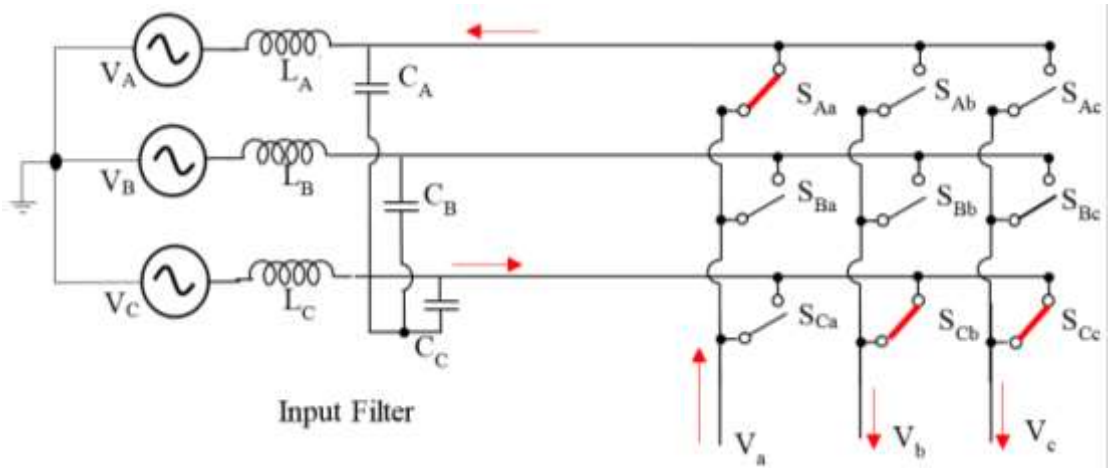


Figure 2.2 Switch state [acc] in the MC

For example, consider the switch state [acc] in Figure 2.2. The output terminal 'A' is connected to input terminal 'a', output terminal 'B' to input terminal 'c' and output terminal 'C' to input terminal 'c'. Hence, the switches S_{aA}, S_{cB} and S_{cC} are ON and all other switches are OFF.

From Figure 2.2, it can be inferred that $V_{AB} = -V_{ca}$, $V_{BC} = 0$, $V_{CA} = V_{ca}$, $i_a = i_A$, $i_b = 0$, $i_c = -i_A$, and the corresponding output voltage and input current vectors computed using EquationS (2.3) and (2.4) are given by Equation (2.5).

$$\overrightarrow{V_o} = -\frac{2}{\sqrt{3}} v_{ca} e^{j0} \; ;$$

$$\vec{I}_i = \frac{2}{\sqrt{3}} i_A e^{j\frac{\pi}{6}} \qquad (2.5)$$

These two vectors can be graphically represented in the αβ reference frame, as in Figure 2.3.

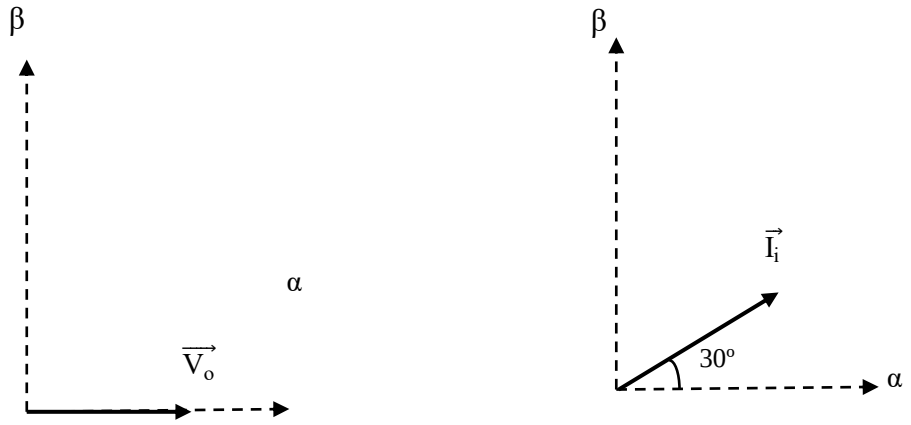


Figure 2.3 Voltage and current Space Vectors for the switch state [acc]

2.2 SWITCHING STATES OF MC

The MC has 27 such switching states, and each state specifies one SSV. They are classified into 3 groups. Each switching state specifies one output voltage and one input current switching vector (SSV) respectively. They are classified into 3 groups.

Group I:

Each output terminal is connected to a different input terminal. Six such states exist, and they are called Rotating Space Vectors. Each SSV has a constant amplitude, the voltage SSVs rotate at the output frequency ω_0, and the current SSVs rotate at the input frequency ω_i. These vectors are not used as switching vectors.

Group II:

Two output terminals are connected to a common input terminal and the third terminal is connected to one of the other two input terminals. These SSVs have time varying amplitude and stationary directions, occupying one of the six positions, spaced 60º apart in the αβ frame. The SSVs belonging to this group are generally called the "allowable switching states" of the MC. Each state is assigned a state number. Two switching states with the same number and opposite signs have two voltage/current SSVs with the same magnitude, but opposite directions, as can be seen in Figure 2.6. The 18 SSVs are tabulated in Table 2.1. The switch state ABC denotes the input terminal that is connected to the output terminals A, B and C. This has already been illustrated for the example switch state [acc].

Group III:

All input terminals are connected to one input terminal. Thus, the three SSVs are zero space vectors. These states are called zero switching states and are used along with the Group II vectors.

The DSVM algorithm selects the switching states and calculates the duty cycle for each switching state. During one switching period T_s, the switching states whose SSVs are adjacent to the desired output voltage (input current) vector, should be selected, and the zero switching states are applied to complete the switching period to provide maximum output to input voltage transfer ratio. For this, we first find the location of the reference output voltage vector and input current vector in the αβ reference plane.

For example, consider that $\overrightarrow{V_0}$ and $\vec{I}_i$ both lie in sector 1in the αβ reference plane as shown in Figure 2.7. $\overrightarrow{V_0}$ is resolved into two components $\overrightarrow{V_0^1}$ and $\overrightarrow{V_0^2}$ along the two adjacent voltage SSVs as in Figure 2.6(a). $\vec{I}_i$ is resolved into two components $\vec{I}_i^1$ and $\vec{I}_i^2$ along the two adjacent current SSVs as in Figure 2.6(b). Possible switching states that can be utilized for state [acc] to synthesize the resolved voltage and current vectors are shown in Table 2.2, which is obtained from Figure 2.6.

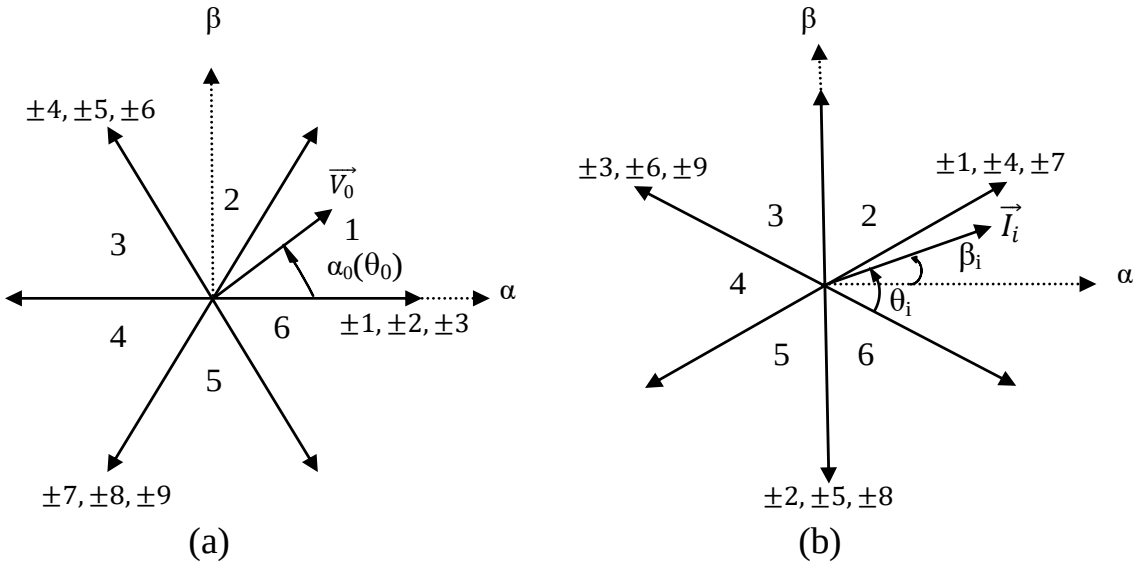


Figure 2.6 (a) Output voltage SSVs (b) Input current SSVs

Table 2.1 Switching states (Group II) of MC

Switch States ABC	Output SSVs		Input SSVs		State No.
	V_0	α_0	I_i	β_i	
caa	$\frac{2}{\sqrt{3}} v_{ca}$	0	$\frac{2}{\sqrt{3}} i_A$	$\frac{\pi}{6}$	1
acc	$-\frac{2}{\sqrt{3}} v_{ca}$	0	$-\frac{2}{\sqrt{3}} i_A$	$\frac{\pi}{6}$	-1
bcc	$\frac{2}{\sqrt{3}} v_{bc}$	0	$\frac{2}{\sqrt{3}} i_A$	$\frac{\pi}{2}$	2
cbb	$-\frac{2}{\sqrt{3}} v_{bc}$	0	$-\frac{2}{\sqrt{3}} i_A$	$\frac{\pi}{2}$	-2
abb	$\frac{2}{\sqrt{3}} v_{ab}$	0	$-\frac{2}{\sqrt{3}} i_A$	$\frac{5\pi}{6}$	3
baa	$-\frac{2}{\sqrt{3}} v_{ab}$	0	$\frac{2}{\sqrt{3}} i_A$	$\frac{5\pi}{6}$	-3
aca	$\frac{2}{\sqrt{3}} v_{ca}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}} i_B$	$\frac{\pi}{6}$	4
cac	$-\frac{2}{\sqrt{3}} v_{ca}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}} i_B$	$\frac{\pi}{6}$	-4
cbc	$\frac{2}{\sqrt{3}} v_{bc}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}} i_B$	$\frac{\pi}{2}$	5
bcb	$-\frac{2}{\sqrt{3}} v_{bc}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}} i_B$	$\frac{\pi}{2}$	-5
bab	$\frac{2}{\sqrt{3}} v_{ab}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}} i_B$	$\frac{5\pi}{6}$	6
aba	$-\frac{2}{\sqrt{3}} v_{ab}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}} i_B$	$\frac{5\pi}{6}$	-6
aac	$\frac{2}{\sqrt{3}} v_{ca}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}} i_C$	$\frac{\pi}{6}$	7
cca	$-\frac{2}{\sqrt{3}} v_{ca}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}} i_C$	$\frac{\pi}{6}$	-7
ccb	$\frac{2}{\sqrt{3}} v_{bc}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}} i_C$	$\frac{\pi}{2}$	8
bbc	$\frac{2}{\sqrt{3}} v_{bc}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}} i_C$	$\frac{\pi}{2}$	-8
bba	$\frac{2}{\sqrt{3}} v_{ab}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}} i_C$	$\frac{5\pi}{6}$	9
aab	$-\frac{2}{\sqrt{3}} v_{ab}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}} i_C$	$\frac{5\pi}{6}$	-9

Table 2.2 Possible switching states

$\overrightarrow{V_0^1}$	±7	±8	±9
$\overrightarrow{V_0^2}$	±1	±2	±3
$\overrightarrow{I_i^1}$	±1	±4	±7
$\overrightarrow{I_i^2}$	±3	±6	±9

To simultaneously synthesize the output voltage and input current vectors, the common switching states ±7, ±9, ±1, ±3 are selected, as shown in Figure 2.7.

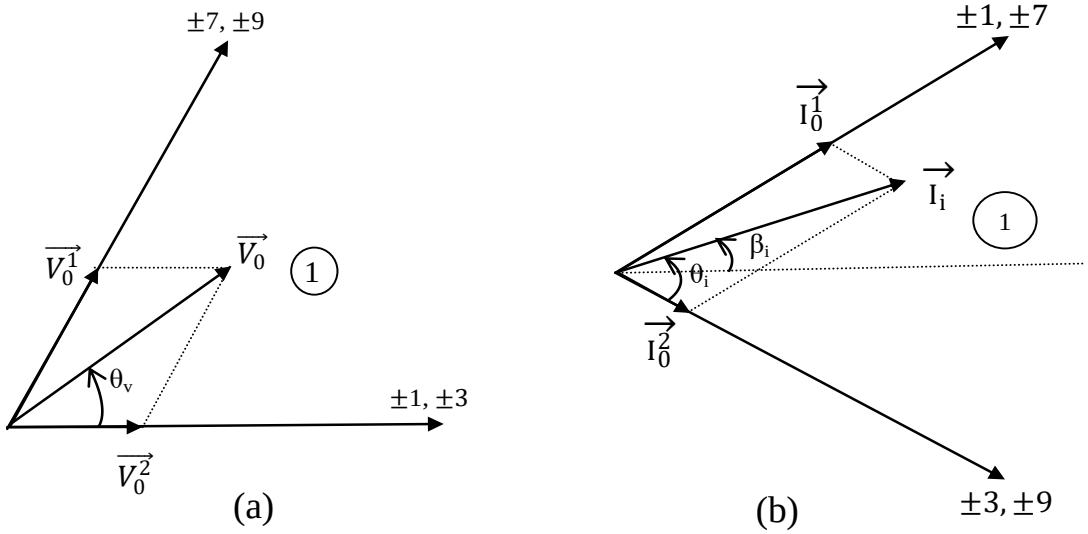


Figure 2.7 (a) Output voltage synthesis (b) Input current synthesis

From two switching states with the same number, only one should be used since the corresponding voltage or current SSVs are in opposite directions. The sign of the switch state to be selected can be found using the formula of the duty cycle ratios. If the duty cycle is positive, the switching state with a positive sign is selected, otherwise, the one with the negative sign is selected.

The same procedure that described when $\overrightarrow{V_o}$ and $\overrightarrow{I_i}$ are in Sector 1, also apply when they are located in Sector 2 to Sector 6. Each case yields four switching states to be utilized. The results for all cases are summarized in Table 2.3. For each case, symbols I, II, III, IV are used to identify the selected four switching states, shown in the last row of Table 2.3.

Table 2.3 Selection of switch states

Sector # of $\vec{I}_i$	Sector # of $\overrightarrow{V_o}$											
	1 or 4				2 or 5				3 or 6			
1 or 4	7	9	1	3	4	6	7	9	1	3	4	6
2 or 5	8	7	2	1	5	4	8	7	2	1	5	4
3 or 6	9	8	3	2	6	5	9	8	3	2	6	5
SYMBOL	I	II	III	IV	I	II	III	IV	I	II	III	IV

The position of the reference output voltage vector and input current vector with respect to the adjacent SSVs are defined as θ_v and θ_i respectively as shown in Figure 2.7, where they are given by Equation (2.6) and Equation (2.7). They are referred to as internal angle within a sector.

$$0 \le \theta_v < \frac{\pi}{3} \tag{2.6}$$

$$0 \le \theta_i < \frac{\pi}{3} \tag{2.7}$$

2.3 DUTY CYCLES

The duty cycle of each selected state id introduced to denote the on-time ratio of that particular switching state during one switching period T_s. d_I, d_{II}, d_{III} and d_{IV} are defined as the duty cycles of the four switching states I, II, III and IV respectively. K_v and K_i denote the sector in which the output voltage and input current space vectors are located in the αβ reference frame.

The duty cycle for each vector is given in Equations (2.8) to (2.11) and (2.13).

$$d_I = [(-1)^{K_v+K_i}]\frac{2}{\sqrt{3}} m_v \sin\theta_v \cdot m_i \sin\theta_i = d_\beta \cdot d_\delta \tag{2.8}$$

$$d_{II} = \left[(-1)^{K_v+K_i+1}\right] \frac{2}{\sqrt{3}} m_v \sin\theta_v \cdot m_i \sin\left(\frac{\pi}{3} - \theta_i\right) = d_\beta \cdot d_\gamma \tag{2.9}$$

$$d_{III} = \left[(-1)^{K_v+K_i+1}\right] \frac{2}{\sqrt{3}} m_v \sin\left(\frac{\pi}{3} - \theta_v\right) \cdot m_i \sin\theta_i = d_\alpha \cdot d_\delta \tag{2.10}$$

$$d_{IV} = [(-1)^{K_v+K_i}] \frac{2}{\sqrt{3}} m_v \sin\left(\frac{\pi}{3} - \theta_v\right) \cdot m_i \sin\left(\frac{\pi}{3} - \theta_i\right) = d_\alpha \cdot d_\gamma \tag{2.11}$$

The duty cycles must satisfy Equation (2.12) in order that the short circuit of any two input phases or open circuit of the load terminals does not occur.

$$|d_I|+|d_{II}|+|d_{III}|+|d_{IV}| \leq 1 \quad (2.12)$$

The duty cycle for the zero vector is calculated using Equation (2.13).

$$d_0 = 1 - \{ |d_I|+|d_{II}|+|d_{III}|+|d_{IV}| \} \quad (2.13)$$

It should be noted that two of the switching states assume negative values. A negative duty cycle indicates that a switching state with a negative sign should be selected. The magnitude alone is taken for generating the pulses.

Now, let us go back to Table 2.2. For both K_v and K_i equal to 1, we can see that d_{II} and d_{III} are negative. Hence, the switching states that are utilized to synthesize the output voltage and input currents are +7, -9, -1 and +3.

2.4 IMPLEMENTATION OF DSVM ALGORTIHM IN MATLAB-SIMULINK

So far the concept behind the DSVM algorithm has been outlined. This section presents a step-by-step detailed explanation of the implementation of DSVM for triggering the Matrix Converter with an R-L load in MATLAB/Simulink.

The block diagram of the setup is shown in Figure 2.8. The system consists of a three-phase AC source with a damped RLC filter at the input side of the converter, and a three-phase RL load connected at the output terminals of the converter. To demonstrate the direct frequency conversion capability of the MC for simulation purposes, we assume the load requires a 3-phase balanced voltage at a frequency of 25 Hz at its terminals. With a 3-phase balanced input supply frequency of 50 Hz, the MC is required to deliver a 3-phase balanced voltage at 25 Hz at its output terminals. The input terminals of the converter are connected to a 3-phase 230V, 50 Hz and an RLC-damped filter. The purpose of the filter is to obtain a sinusoidal input current waveform, thereby improving the THD of the input current. Figure 2.9 shows the source with the filter.

L_f and C_f are employed in general to smoothen the chopped waveform of the converter. In addition to these components, a resistance is connected across them. The resistor across the inductor is called a damping resistor, and that across the capacitor is termed as a discharge

resistor. As the chopping of the current drawn from the grid is done at a relatively high frequency, the inductor and capacitor have to discharge the energy stored in them at a high rate. The resistances connected across them provide a path to dissipate the energy so that when the next cycle of charging begins, the energy storing elements are fully discharged.

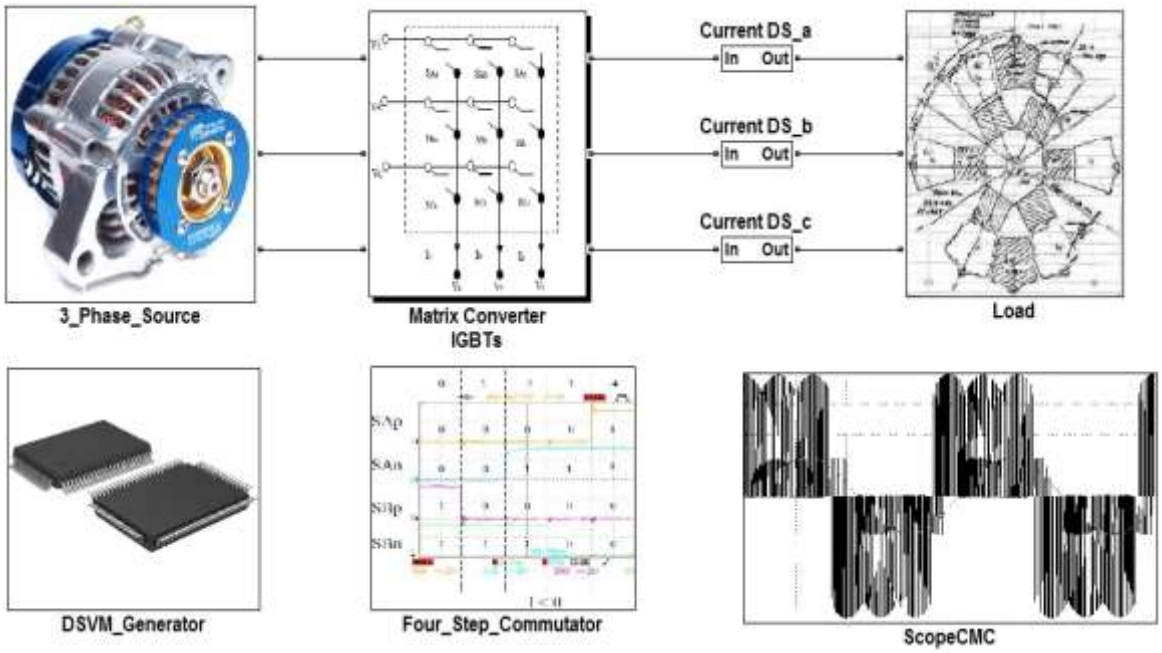


Figure 2.8 Setup of the MC triggered using DSVM

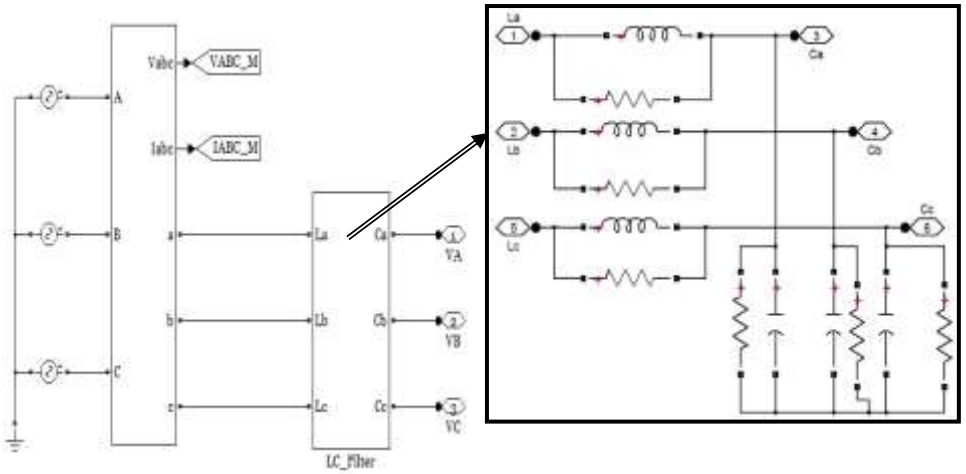


Figure 2.9 Source side of the MC

The Matrix Converter comprises of 9 bidirectional switches. Each switch consists of two IGBTs connected in Common-Emitter configuration with two feedback diodes in anti-parallel. Figure 2.10 shows the power circuit diagram of the MC, as in the Simulink environment.

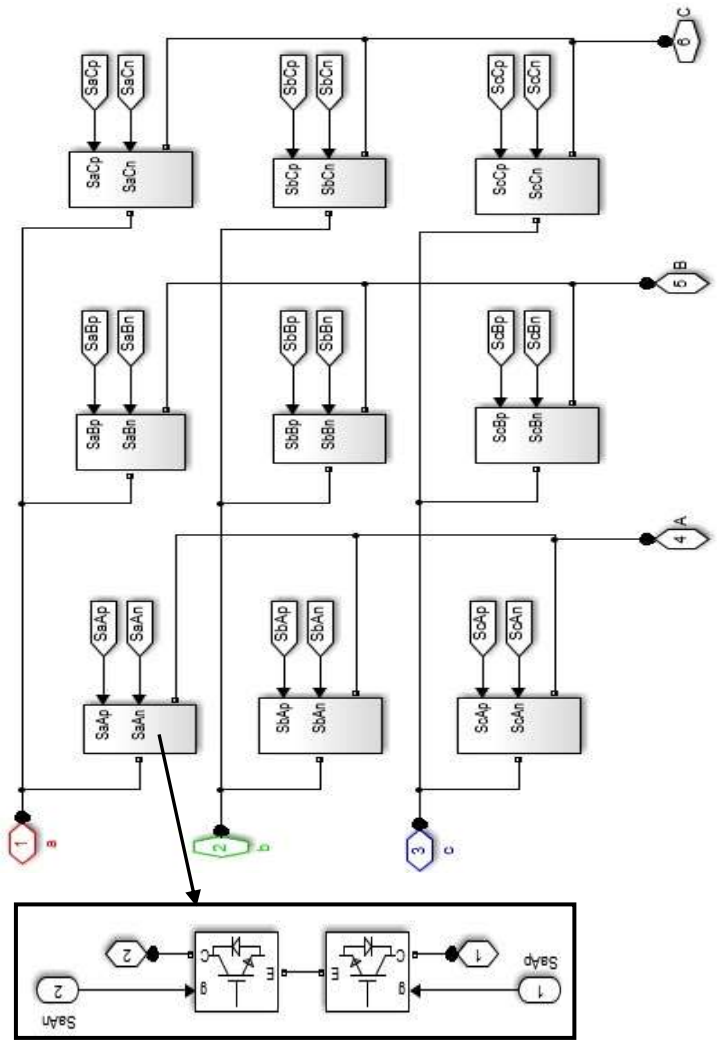


Figure 2.10 Matrix Converter Power Circuit

A simple RL load connected to the output terminals of the MC is shown in Figure 2.11.

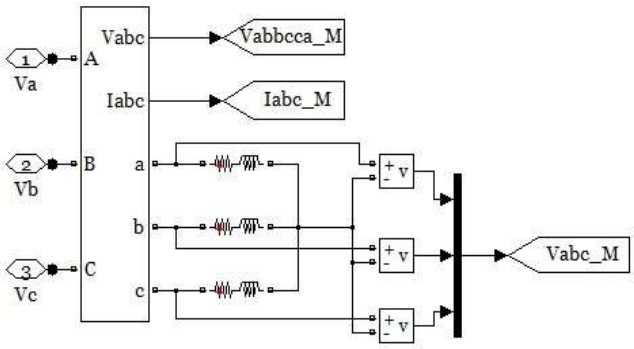


Figure 2.11 Three-phase RL load

The three-phase V-I measurement block in Simulink blockset is used to measure the line voltage (V_{abbcca}_M) at the converter output terminals and the load currents. V_{abc}_M represents the three phase to neutral voltages. Now, we go ahead with implementing the triggering circuit for the bidirectional switches using Direct Space Vector Algorithm in Simulink. It is represented as the "DSVM Generator" block in Figure 2.8. The main blocks of the DSVM Generator are shown in Figure 2.12.

So far, if one has noticed, we have been talking about an output reference voltage space vector and an input current space vector. What these exactly are, and their purposes have not been mentioned clearly. As the MC is a single stage conversion power converter, it is required that we obtain a variable-voltage, variable frequency at its output terminals from a constant voltage, constant frequency input supply.

2.4.1 Current Reference

In an inverter, the frequency of the input current drawn is not an issue at all, as it is DC. We would only have to make sure the magnitude and frequency of the load voltage is maintained at the required values. In contrast, in an MC, say the output voltage is set to 25 Hz, the load current will also be drawn at 25 Hz. But the converter input current cannot be at 25 Hz. It has to be at the grid frequency, 50 Hz, and synchronized with the grid voltage for unity power factor operation. For this purpose, the "phase voltage" of the grid itself is taken as reference for the input current. Though the magnitude of the input current will vary according to the load current drawn, the frequency and phase angle is synchronized to that of the grid phase voltage.

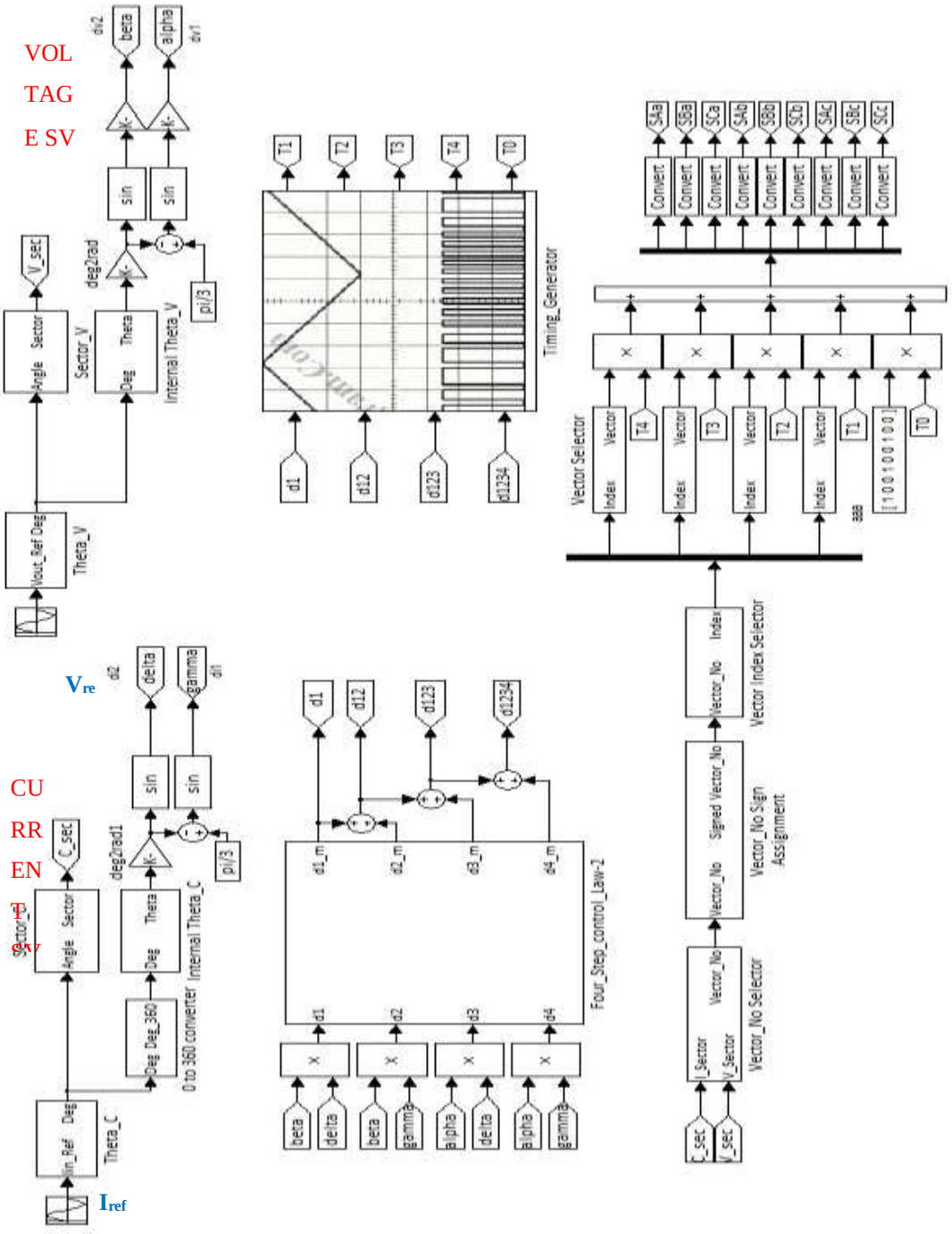


Figure 2.12 DSVM Generator

2.4.2 Voltage Reference

The voltage space vector reference is the actual voltage waveform that is desired at the output terminals of the converter. For example, in our work we are going to use the MC as the rotor side power electronic converter for controlling the stator power of the DFIG. The voltage that is injected into the rotor from the converter directly controls the stator power. The frequency

of this voltage is “slip frequency”, and varies with the speed of the rotor shaft. It is required that the converter inject a variable voltage, “slip frequency” waveform that is obtained from the controller in the rotor terminals. This waveform from the controller itself is given as the reference signal to the voltage space vector hexagon so that one can synthesize the waveform by switching the adjacent space vectors using the DSVM algorithm.

2.4.3 Synthesis of Output Voltage and Input Current

In order that the output voltage space vector and the input current space vectors be synthesized, using four switching states, we have to first determine the location of the space vectors in the corresponding αβ reference frames. The reference space vectors in the αβ plane, given by Equation (2.3) and Equation (2.4) are computed from the three-phase reference signals as outlined in Equation (2.14). The corresponding blocks are highlighted in Figure 2.12.

$$\overrightarrow{V_o} = \frac{2}{3}(v_{AB} + a v_{BC} + a^2 v_{CA})$$

$$V_\alpha + jV_\beta = \frac{2}{3}\left\{V_{AB} + \left(e^{j2\pi/3} * V_{BC}\right) + \left(e^{j4\pi/3} * V_{CA}\right)\right\}$$

$$V_\alpha + jV_\beta = \frac{2}{3}\left\{V_{AB} + \left(\left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right) * V_{BC}\right) + \left(\left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right) * V_{CA}\right)\right\}$$

$$V_\alpha + jV_\beta = \frac{2}{3}\left\{V_{AB} - \frac{1}{2}(V_{BC} + V_{CA}) + j\frac{\sqrt{3}}{2}(V_{BC} - V_{CA})\right\}$$

$$V_\alpha = \frac{2}{3}\left\{V_{AB} - \frac{1}{2}(V_{BC} + V_{CA})\right\} \quad \text{and} \quad V_\beta = \frac{1}{\sqrt{3}}(V_{BC} - V_{CA}) \qquad (2.14)$$

The same applies for the computation of I_α and I_β components for an input current reference vector $\vec{I_i}$. The equations for the real and imaginary components of the input current space vector are given directly in Equation (2.15).

$$I_\alpha = \frac{2}{3}\left\{I_a - \frac{1}{2}(I_b + I_c)\right\} \quad \text{and} \quad I_\beta = \frac{1}{\sqrt{3}}(I_b - I_c) \qquad (2.15)$$

The angular position of the reference space vectors with respect to the “α” co-ordinate axis is given by Equation (2.16).

$$\text{Angle} = \tan^{-1}\frac{\text{Imaginary } (\beta)}{\text{Real } (\alpha)} \qquad (2.16)$$

From Figure 2.6, the equations for α_o and β_i are given by Equation (2.17).

$$\alpha_o = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \text{ and } \beta_i = \tan^{-1}\left(\frac{I_\beta}{I_\alpha}\right) \qquad (2.17)$$

It has to be noted that the range of values for α_o and β_o is [-180º, 180º]. Figure 2.13 shows the implementation of Equation (2.14) and Equation (2.17) for the voltage reference alone. The same applies for the transformation of the current reference to αβ frame, and the computation of β_i.

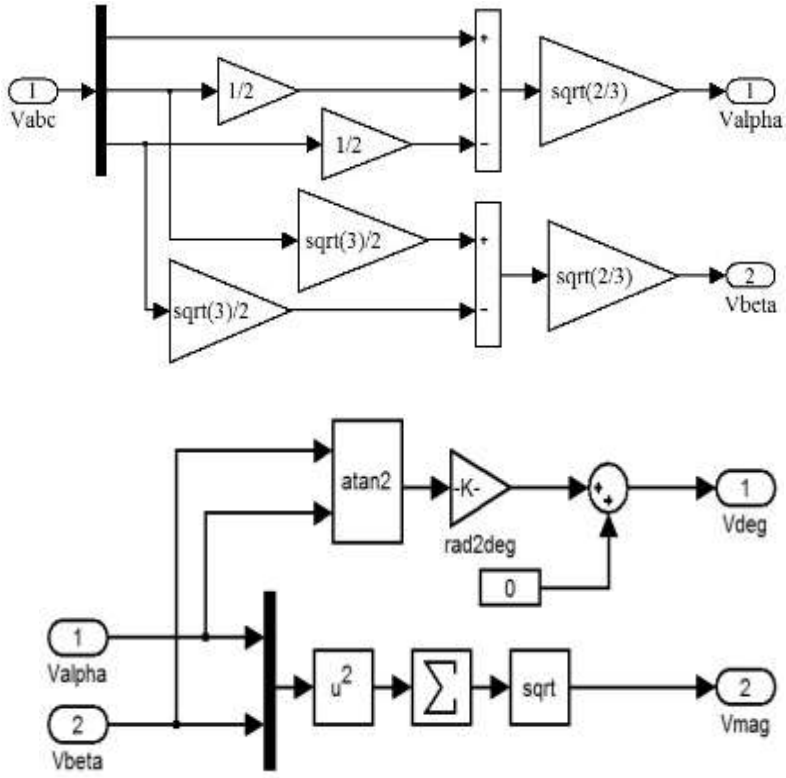


Figure 2.13 α-β Transformation of reference voltage and its angle in α-β plane

The reference voltage and its angle are graphically shown in Figure 2.14. The same for the reference current is shown in Figure 2.15. The angle of the current reference vector $\vec{I}_i$ is converted from [-180º, 180º] to [0º, 360º] for reasons that will be evident when calculating the internal theta, θ_i.

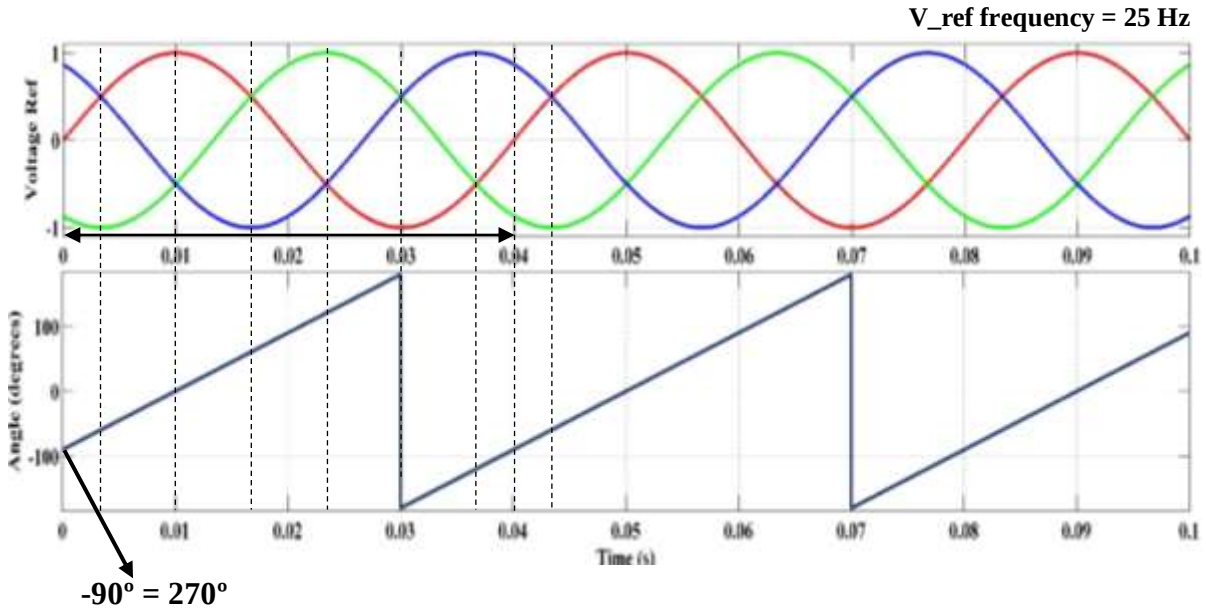


Figure 2.14 Angle of Voltage Reference with respect to "α" axis, α_o

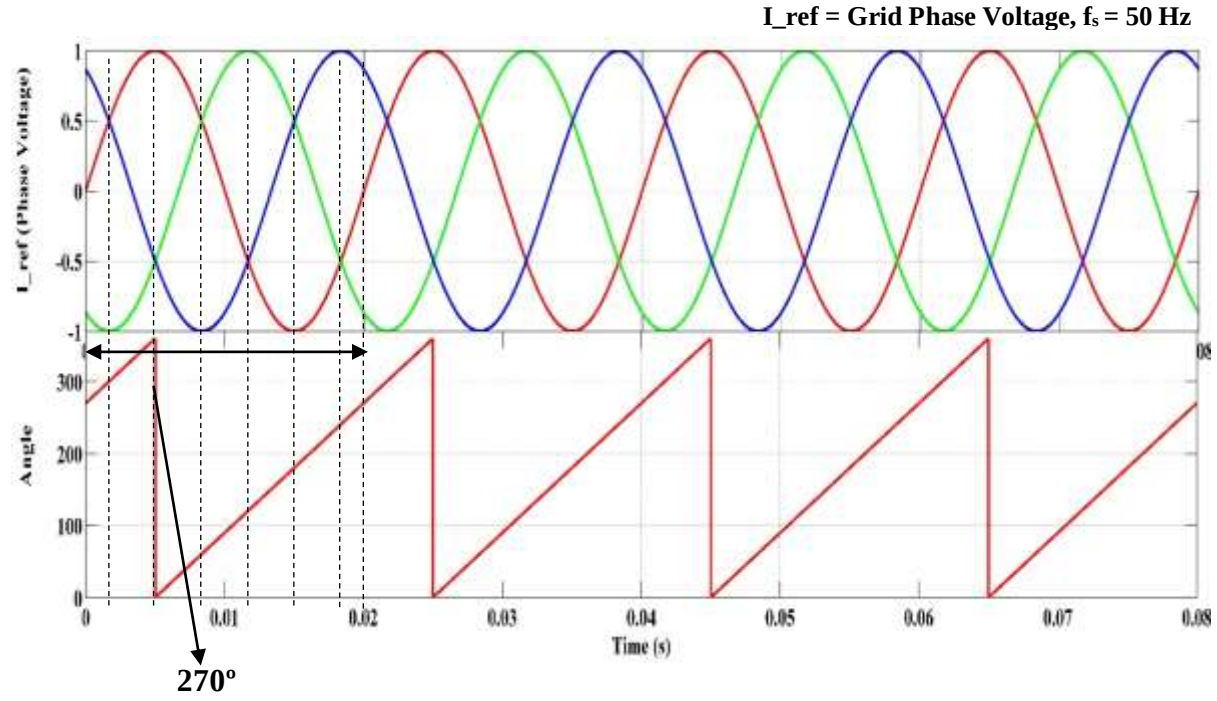


Figure 2.15 Angle of Current Reference with respect to "α" axis, β_i

The next step is to find the sector in which the reference space vectors are located. From Figure 2.6, there can be six sectors, each spanning 60º. Table 2.4 lists the sectors of the voltage and current space vectors.

Table 2.4 Sectors of the Voltage and Current space vector hexagons

VOLTAGE SV		CURRENT SV	
Sector	Angle (º)	Sector	Angle (º)
1	0-60	1	-30 to 30
2	60-120	2	30-90
3	120-180	3	90-150
4	180-240	4	150-210
5	240-300	5	210-270
6	300-360	6	270-330

For the angle obtained from the αβ block, the sector is identified using a simple logic circuit. Figure 2.16 shows the sector of the voltage reference vector, K_v, and Figure 2.17 shows the sectors obtained from the block.

Note: The voltage space vector always starts in the 5^{th} sector, corresponding to 270º when the input is a three-phase balanced sine wave. If the input is taken to be cosinusoidal, then it will start in the 1^{st} sector, corresponding to 0º.

Figure 2.18 shows the sector identification of the current space vector from the angle β_i. It is evident that the current space vector hexagon is shifted 30º with respect to the voltage space vector hexagon.

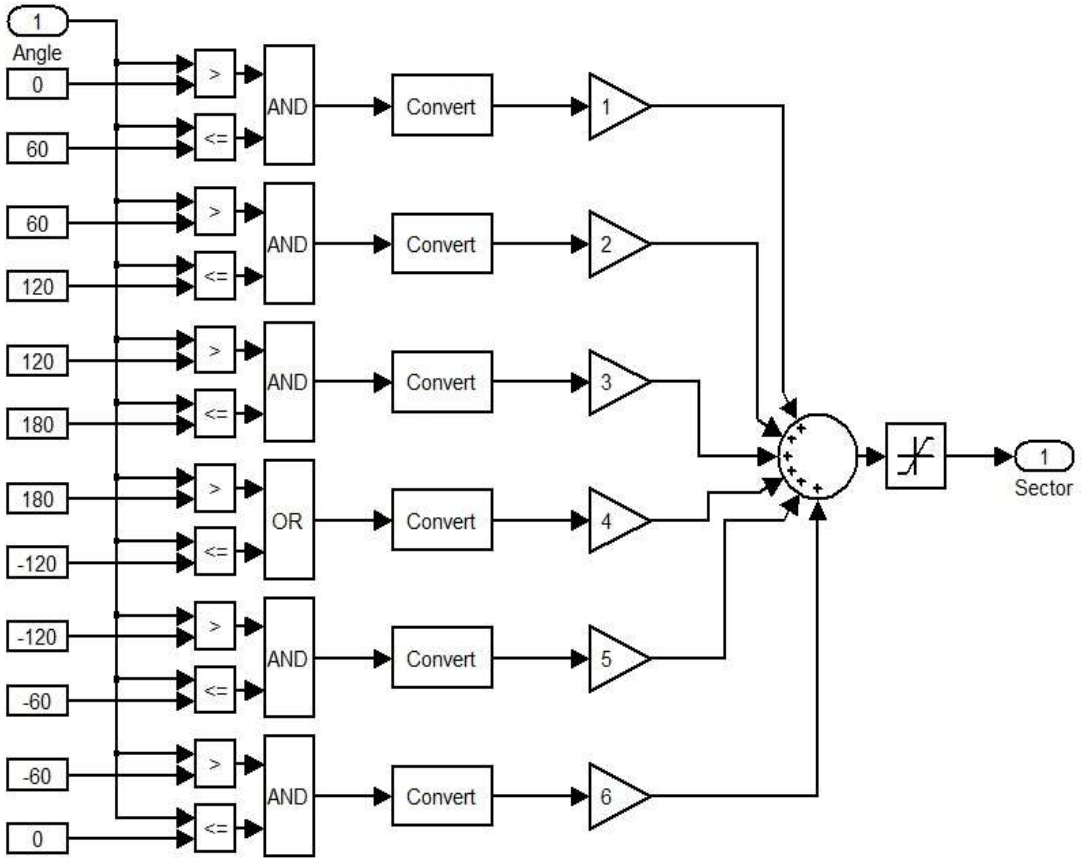


Figure 2.16 Identification of Voltage Sector

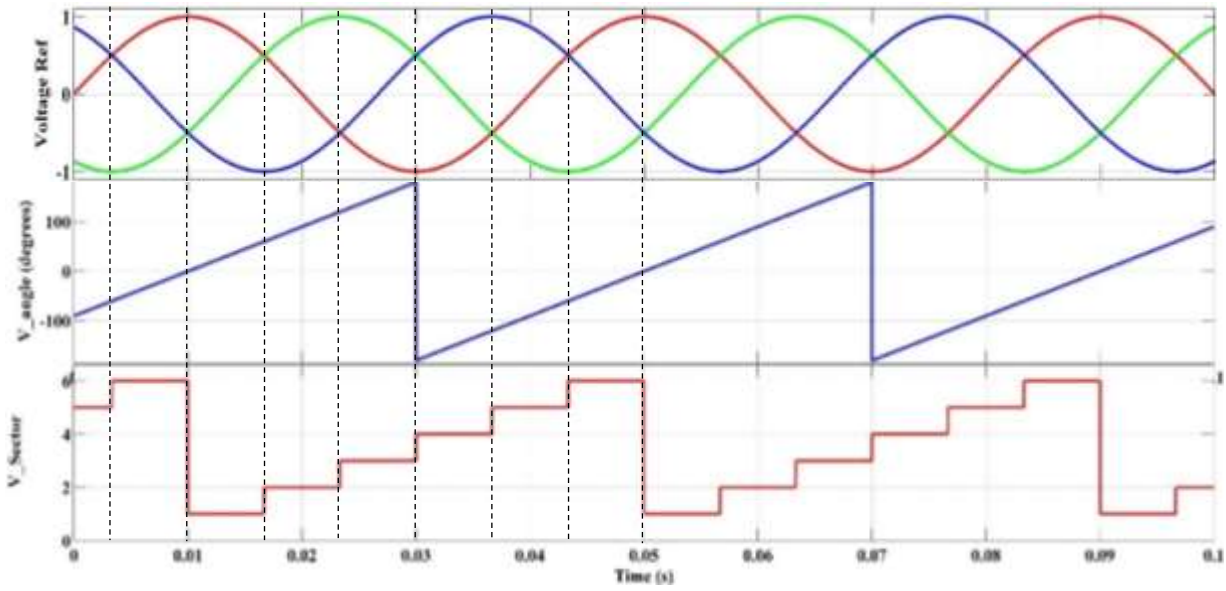


Figure 2.17 Sectors obtained from α_o

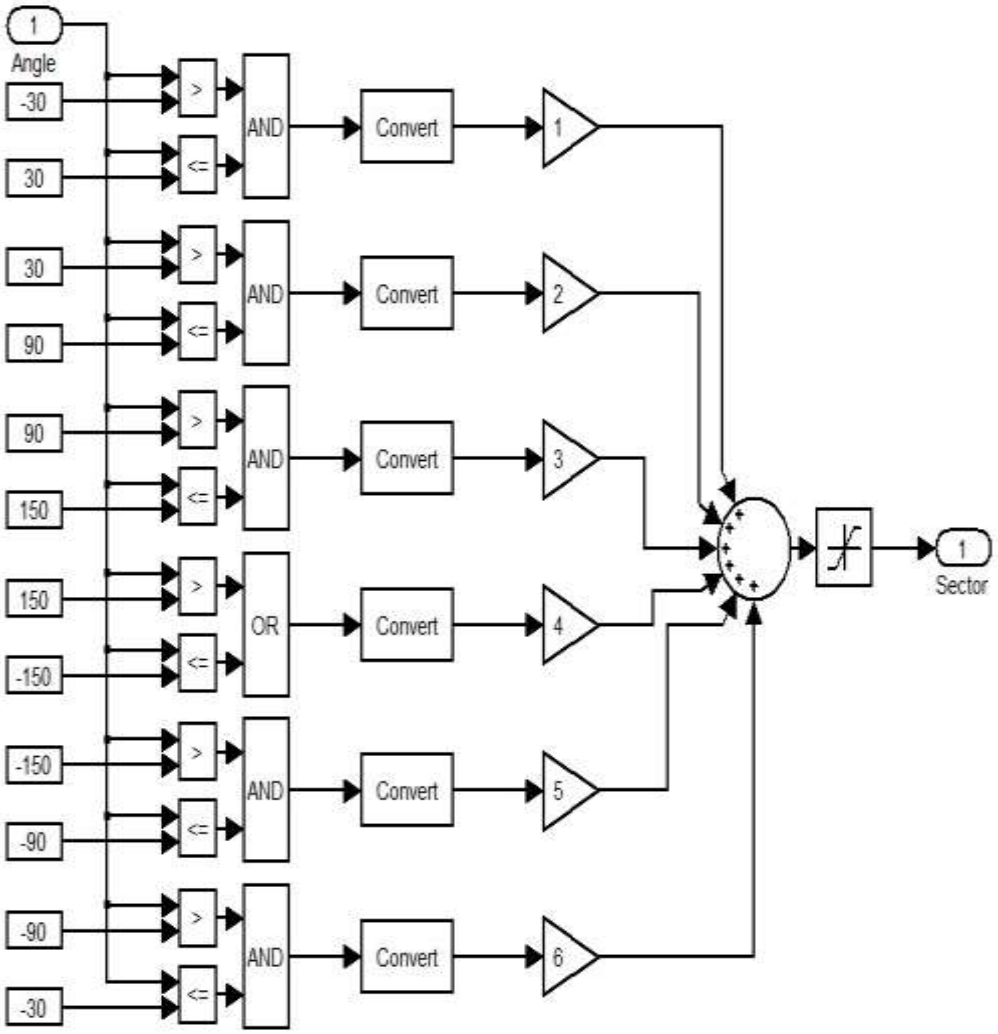


Figure 2.18 Identification of current sector K_i

Figure 2.19 shows the current sectors obtained from the angle of the current space vector. The waveform shows the angle converted to 360º.

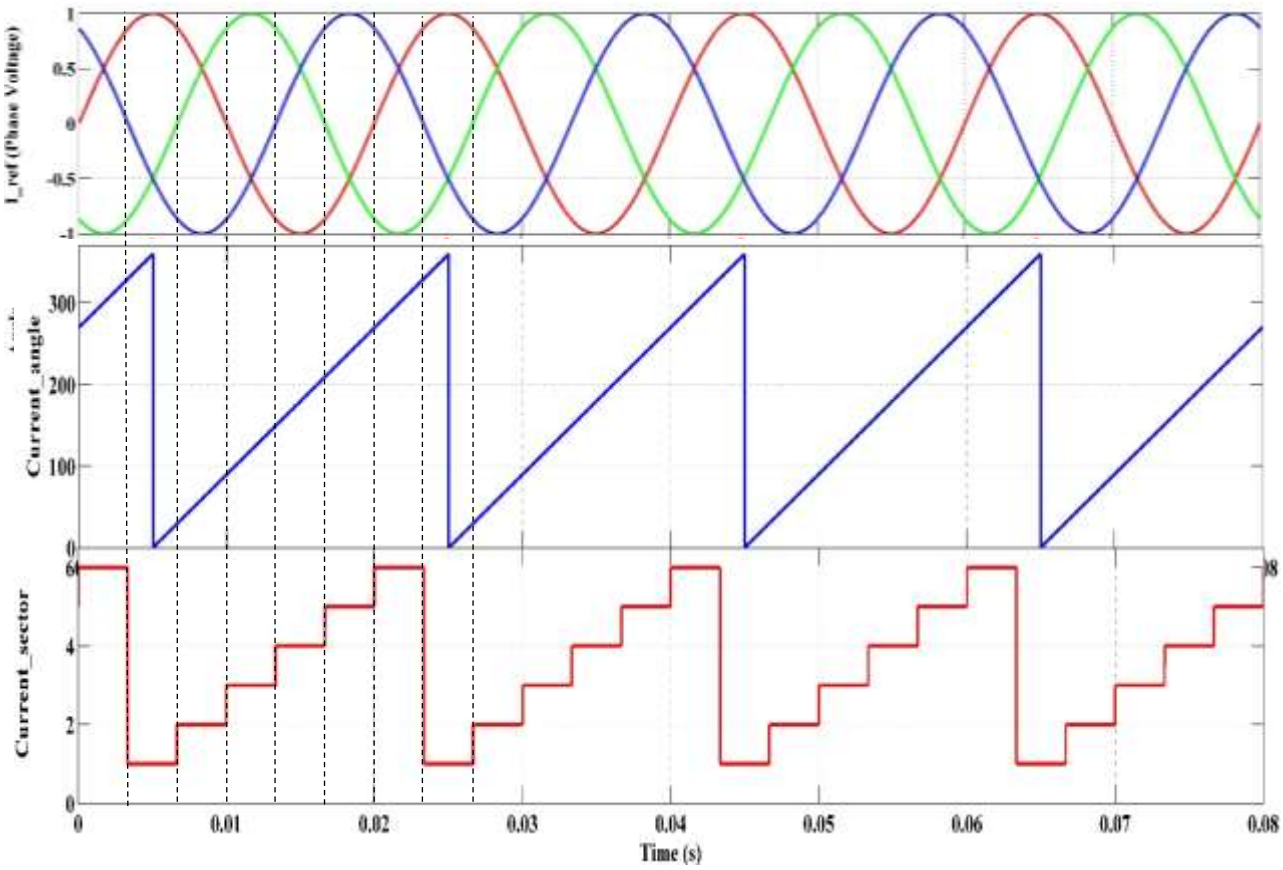
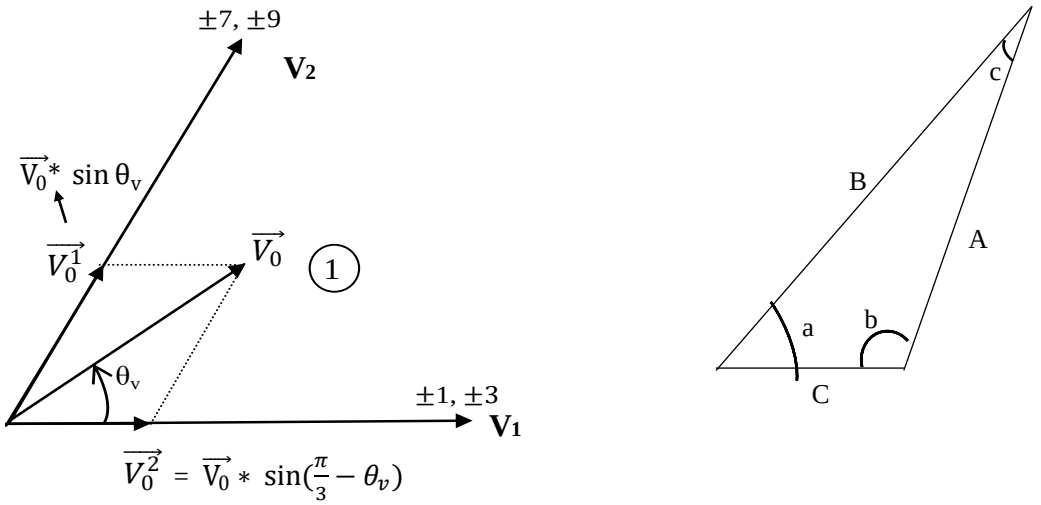


Figure 2.19 Current sector obtained from β_i

NOTE: Similar to the voltage space vector, the current space vector always starts in the 6th sector, corresponding to 270^o when the reference is taken to be a three-phase balanced sinusoidal waveform. If the reference is taken as a co-sinusoidal waveform, the current space vector will be located in the middle of the 1st sector, corresponding to 0^o at t=0.

The identification of the sector is essential for the selection of vectors to be applied for synthesizing the reference waveforms. In order to calculate the duration for which each vector is applied, the duty ratios given by Equations (2.8) – (2.12) have to be computed. The formulae for the duty ratios contain the terms θ_v and θ_i, which we have defined as the internal angle of the reference vector within a sector earlier in this chapter through Equation (2.6) and Equation (2.7). The graphical representation is shown in Figure 2.7.

The magnitude of the vectors $\overrightarrow{V_o^1}$ and $\overrightarrow{V_o^2}$ in order to synthesize $\overrightarrow{V_o}$ is obtained using the Sine Law of Triangles as demonstrated in Figure 2.20.



Sine Law of Triangles:

From the figure on the RHS, $\frac{|A|}{\sin a}=\frac{|B|}{\sin b}=\frac{|C|}{\sin c}$

On applying the above law to the space vector diagram,

$$\frac{|B|}{\sin b}=\frac{|C|}{\sin c} \Rightarrow \frac{\overrightarrow{V_o}}{\sin(120^\circ)}=\frac{\overrightarrow{V_o^2}}{\sin\left(180-(120+\theta_v)\right)}$$

$$\Rightarrow \frac{\overrightarrow{V_o}}{\sin(120^\circ)}=\frac{\overrightarrow{V_o^2}}{\sin(60-\theta_v)}$$

$$\Rightarrow \overrightarrow{V_o^2}=\frac{\overrightarrow{V_o}}{\sin(120^\circ)} * \sin(60-\theta_v)$$

$$\Rightarrow \overrightarrow{V_o^2}=\frac{2}{\sqrt{3}}\overrightarrow{V_o} * \sin(60-\theta_v)$$

$\overrightarrow{V_o^1}$ can also be found in a similar manner, and is found to be $\frac{2}{\sqrt{3}}\overrightarrow{V_o} * \sin(\theta_v)$

Figure 2.20 Derivation of the duty cycles

From the SVM for an inverter (Han Ju Cha, 2004), the duty cycles can be represented in terms of the modulation index, given by Equation (2.18).

$$m_v=\frac{\sqrt{3}\,\overrightarrow{V_o}}{V_{dc}} \qquad (2.18)$$

where, m_v is the voltage transfer ratio, also known as, the modulation index, $\overrightarrow{V_o}$ is the peak value of the reference voltage space vector and V_{DC} is the input DC voltage to the inverter. From Figure 2.20, the formula for the length of the vector to be applied is given by Equation (2.19).

$$\overrightarrow{V_o^2}=\frac{2}{\sqrt{3}}\overrightarrow{V_o} * \sin(60-\theta_v)$$

$$d_\alpha * V_1 = \frac{2}{\sqrt{3}}\overrightarrow{V_o} * \sin(60-\theta_v) \qquad (2.19)$$

where, d_α is the duration for which the vector V_1 is to be applied when the reference space vector is located in Sector 1, with an internal angle θ_v. The magnitude $d_\alpha V_1$ gives the length of the vector required to synthesize the reference vector $\overrightarrow{V_o}$, while $d_\beta V_2$ gives the length of the vector V_2 that is to be applied in conjunction with $d_\alpha V_1$ to synthesize the reference vector.

It is known that the magnitude of each space vector in the αβ reference frame is $\frac{2}{3}V_{DC}$. On substituting this value in Equation (2.19), and using Equation (2.18), we get the duty cycle d_α as given by Equation (2.20).

$$d_\alpha * \frac{2}{3}V_{DC} = \frac{2}{\sqrt{3}}\overrightarrow{V_o} * \sin(60-\theta_v)$$

$$d_\alpha = \frac{2}{\sqrt{3}} * \frac{3}{2V_{DC}}\overrightarrow{V_o} * \sin(60-\theta_v)$$

$$d_\alpha = \frac{\sqrt{3}\ \overrightarrow{V_o}}{V_{DC}} * \sin(60-\theta_v)$$

$$d_\alpha = m_v * \sin(60-\theta_v) \qquad (2.20)$$

The other duty cycles d_β, d_δ and d_γ can be derived in a similar fashion, and is given by Equations (2.21) to (2.23).

$$d_\beta = m_v \sin\theta_v \qquad (2.21)$$

$$d_\gamma = m_i \sin\left(\frac{\pi}{3}-\theta_i\right) \qquad (2.22)$$

$$d_\delta = m_i \sin\theta_i \qquad (2.23)$$

The maximum value of the reference voltage inside the space vector hexagon that can be synthesized using SVM technique is equal to the radius of the inscribed circle = 0.866. Hence, the maximum value of the modulation index of the MC is 0.866. This is one of the inherent demerits of the MC, which can be overcome using the Third Harmonic Injection Method. We will not be going into detail about it, as it is not a part of the work carried out. There are numerous literature on the improvement of the modulation index of the MC.

These duty cycles can be used directly in Equations (2.8) to (2.11) to compute the duty cycles if the MC vectors to be applied. In a sense, the inverter and rectifier space vector algorithms are inevitable for understanding the Direct Space Vector technique.

2.4.4 Control Law

It has to be ensured that the duty cycle values are not too small so that they may be missed by the controller. Also, they should be larger than the time taken for one commutation cycle. As the time taken for commutating one IGBT is 600 ns, we require 4 cycles of 600 ns to carry out the 4-step commutation process (explained in detail later). Say we fix the minimum value of the duty cycle as 5*600 ns = 3 μs. The appropriate law-II is used here, and is given by Equation (2.24).

$$d_{compensated} = \begin{cases} 0, & \text{if } d < \left(\frac{1}{2} d_{min}\right) \\ d_{min}, & \text{if } \left(\frac{1}{2} d_{min}\right) < d < d_{min} \end{cases} \quad (2.24)$$

The meaning of Equation (2.24) is

a. Any duty-cycle "lower than half the minimum duty-cycle d_{min}" is ignored
b. Any duty-cycle "greater than half the minimum duty-cycle, but less than d_{min}" is to be approximated to d_{min} itself.
c. Any duty cycle greater than d_{min} is not altered, as it is a significant pulse.

The application of the control law results in improvement in the current waveform. Figure 2.21 shows the computation of duty cycles of the MC, and the application of control law to them. Table 2.5 shows the values of the parameters in Figure 2.21.

Table 2.5 Control Law Parameters

PARAMETER	VALUE
S_f	3 kHz
f_st_Clk	$1/(5*600e-9) = 3.3333 * 10^5$ Hz

S_f is the switching frequency, and f_st_clk determines the minimum duty cycle for the Control Law. Using the values in Table 2.5, we have set d_{min} to 0.009.

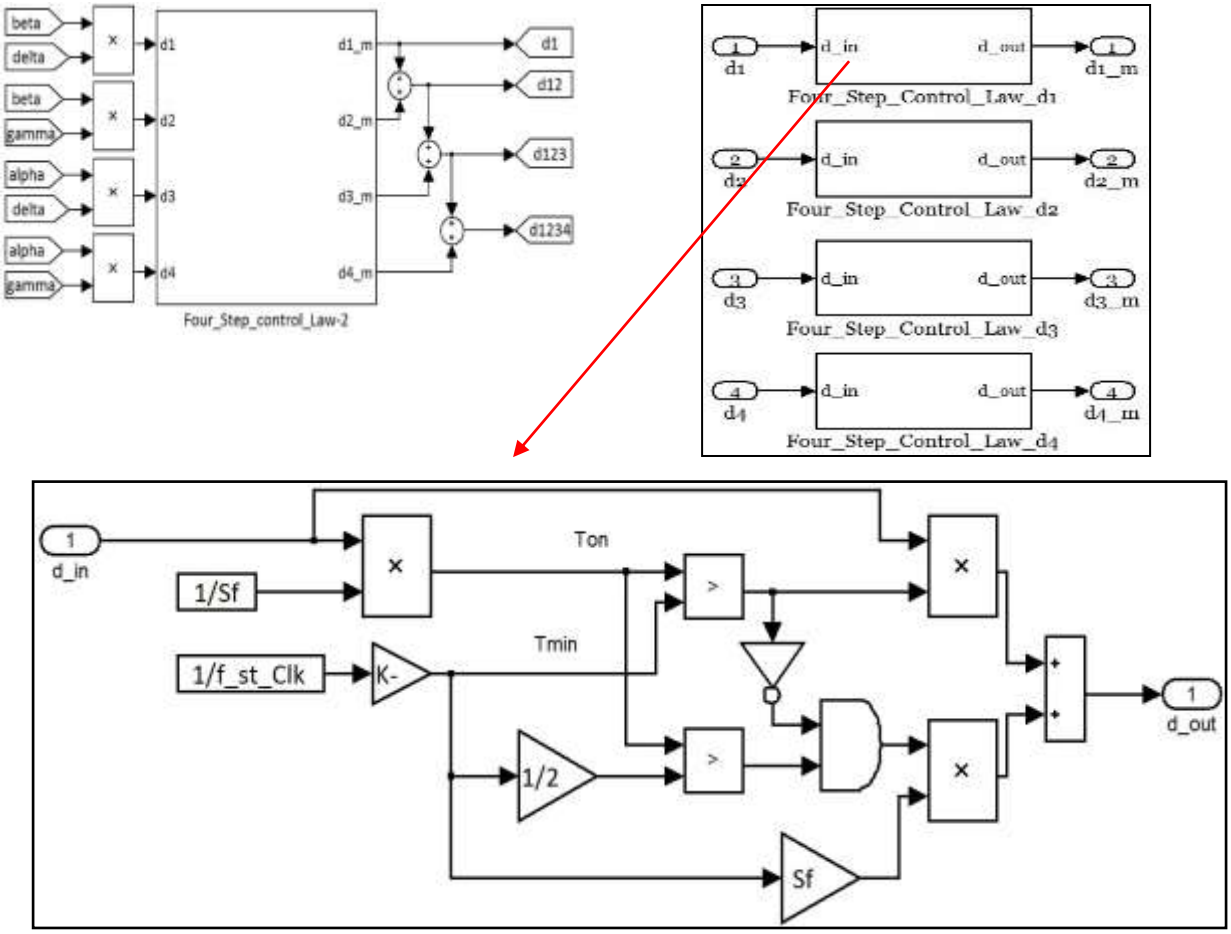


Figure 2.21 Implementation of Control Law

The computation and setting of d_{min} are shown for different values of f_st_clk for a better understanding for a fixed switching period T_s= 1/3000 = 3.3333*10^{-4} s.

1. f_st_clk=3 MHz.

$$T_{st\_clk} = 1/3*10^{6} = 3.3333*10^{-7} \text{ s.}$$

$$d_{min} = \frac{T_{st\_clk}}{T_s} = \frac{3.333 \times 10^{-7}}{3.333 \times 10^{-4}}$$

$$= 0.001$$

2. f_st_clk = 1/(600ns*5) = 3.3333 * 10^{5} Hz

$$T_{st\_clk} = 1/(600 \text{ ns} * 5) \quad = 3*10^{-6} \text{ s}$$

$$d_{min} = \frac{3\times10^{-6}}{3.333\times10^{-4}} = 0.009.$$

Case 2 is a more practical approach, keeping in mind the minimum time required for the commutation sequence. In Case 1, the minimum duty cycle is 0.001, which will result in very narrow pulses, and there is a very good chance that the pulse be missed during the commutation sequence, or by the controller itself. The recomputation of duty cycles are shown for Case 2 in Figure 2.22.

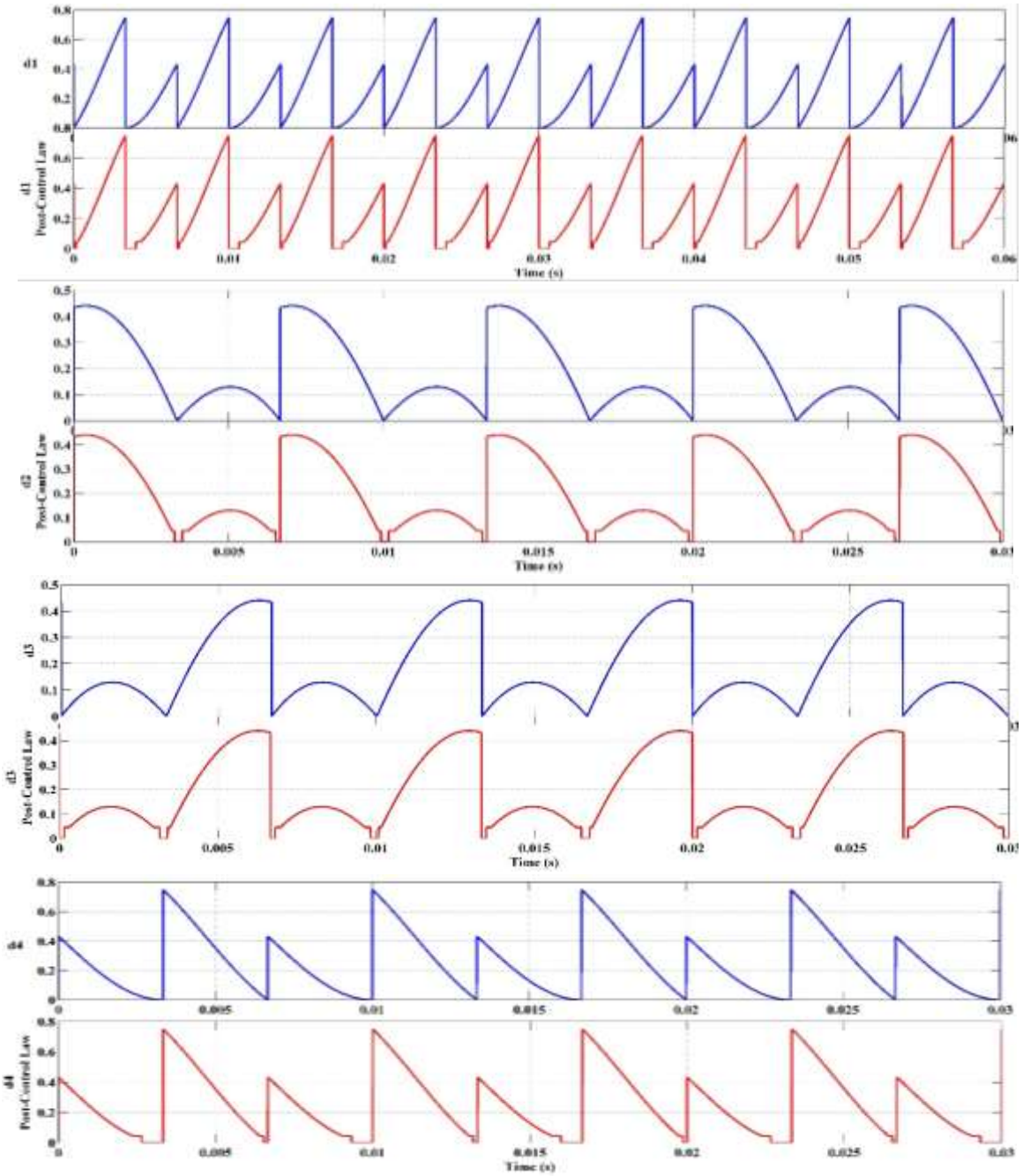


Figure 2.22 Application of Control Law

Any duty cycle value less than $\frac{3\mu}{2}$ = 1.5μs is discarded and set to zero. For values between 1.5 μ and 3 μ, the duty cycle is reset to 3μs. For values above 3 μs, the duty cycle is not altered.

2.4.5 Timing Generator

The switching frequency is set at 3 kHz. A triangular wave of frequency 3 kHz is used as the carrier wave to generate the switching pulses as shown in Figure 2.23.

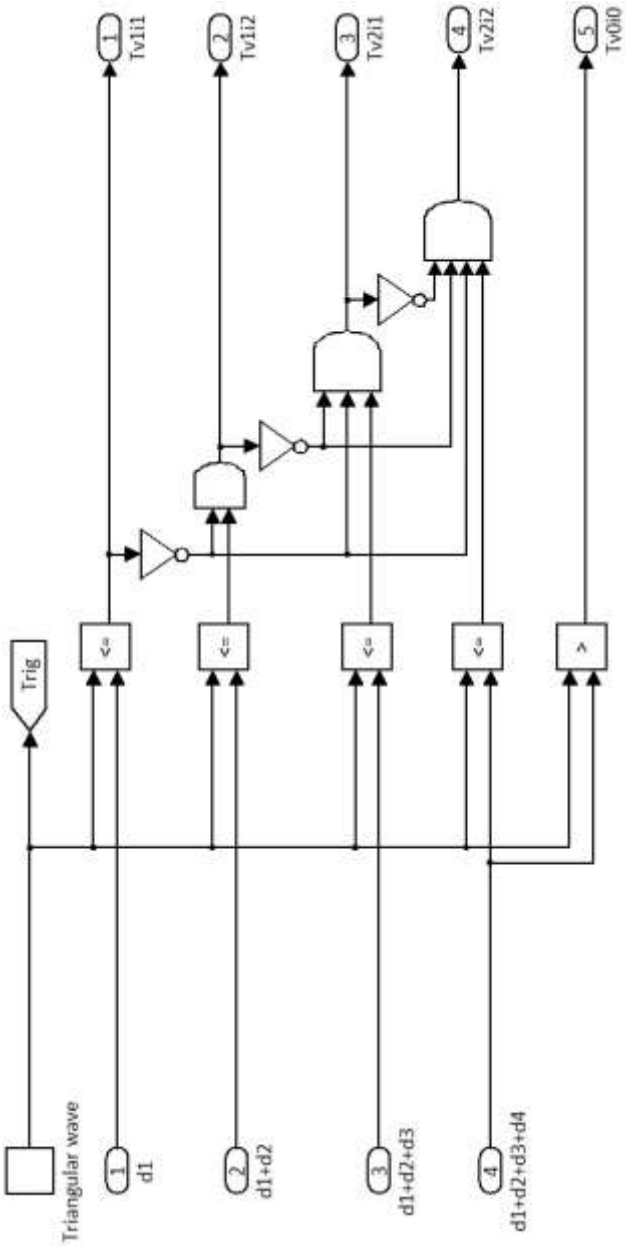


Figure 2.23 Timing Generator

The five duty cycles, including that for the zero vector are compared with the carrier wave and the pulses are generated. This is graphically shown in Figure 2.24.

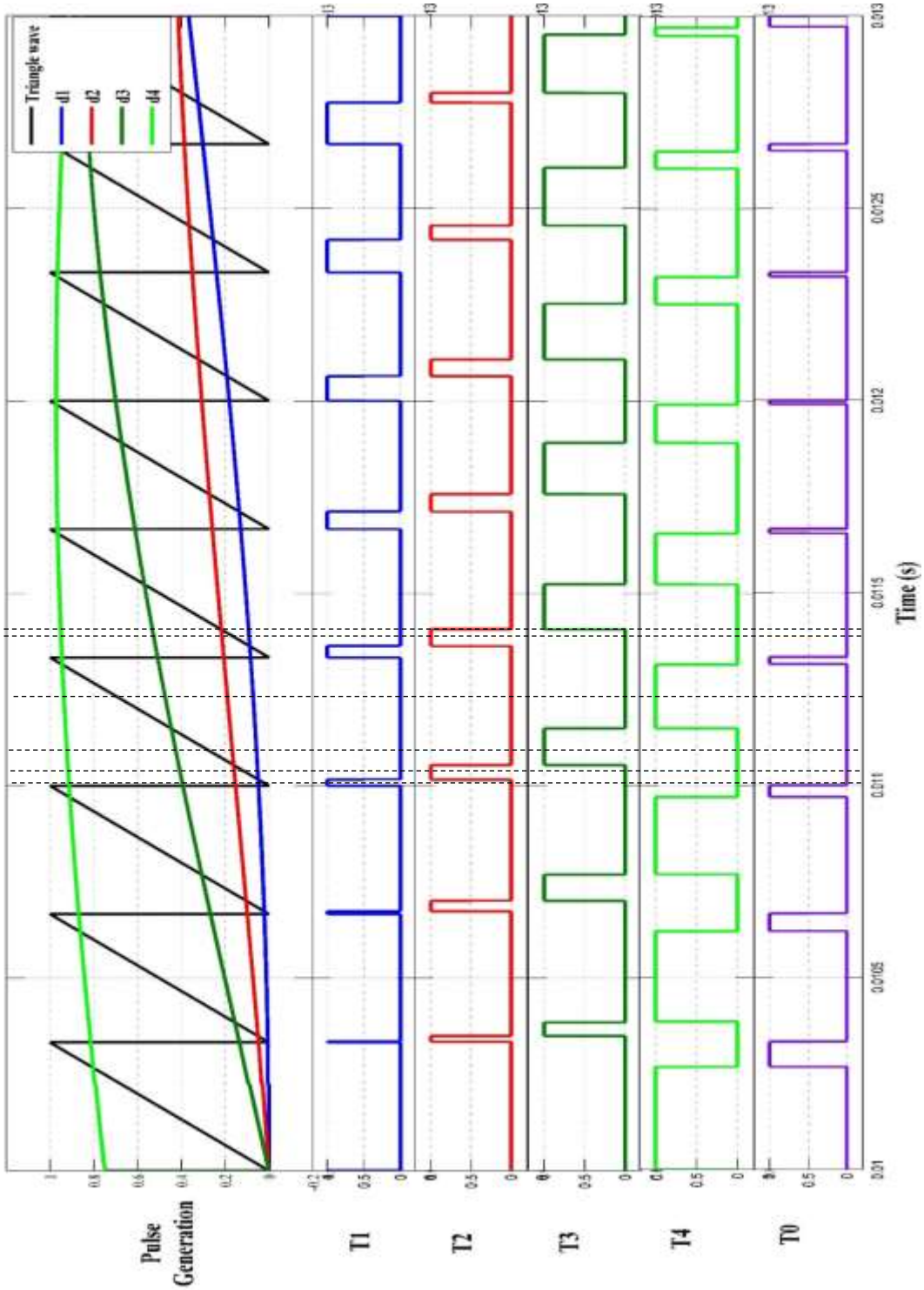


Figure 2.24 Timing pulse generation

We are yet to determine the switch states and finally generate the firing pulses for the nine bidirectional switches. Figure 2.25 shows the switching state or the vector selection from the current and voltage sectors. There are 4 blocks, and each block is explained below.

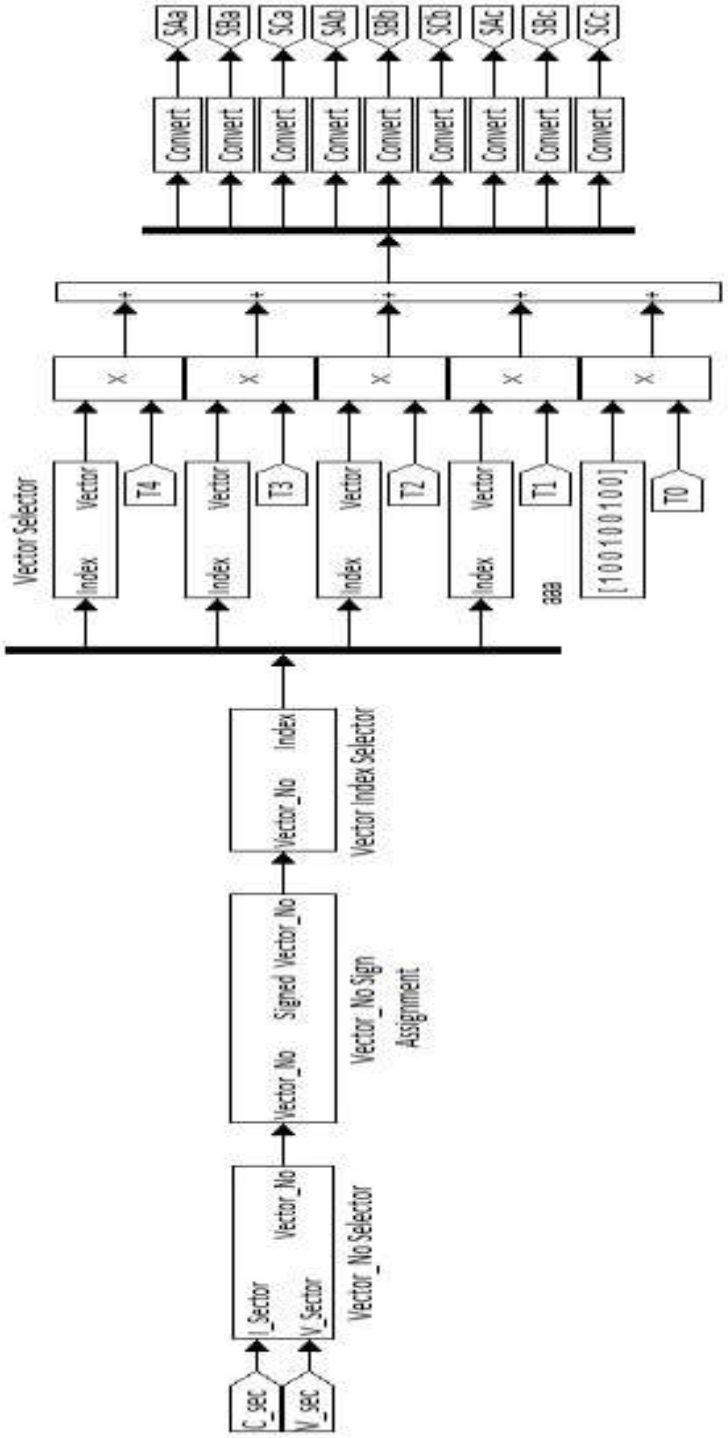


Figure 2.25 Vector selection and pulse generation

Block 1: Vector No Selector

Based on the current and voltage sector, this block determines which set of vectors are to be applied, which was shown in Table 2.3. Figure 2.26 shows how the vectors to be applied are identified.

Figure 2.26 is mostly self-explanatory. As a first step, we check for the nine possible combinations of the current and voltage vectors. One such block which checks whether the current and voltage sectors are 1 or 4 is shown as an inset. Weights are assigned for each sector identification block from 1 to 9, from top to bottom as in Figure 2.26. Finally, based on the weight that appears on the "Select" line of the multi-port switch, the 4 vectors are selected. It is best to verify with Table 2.3. Please note that a vector can be given in Simulink using the Constant block.

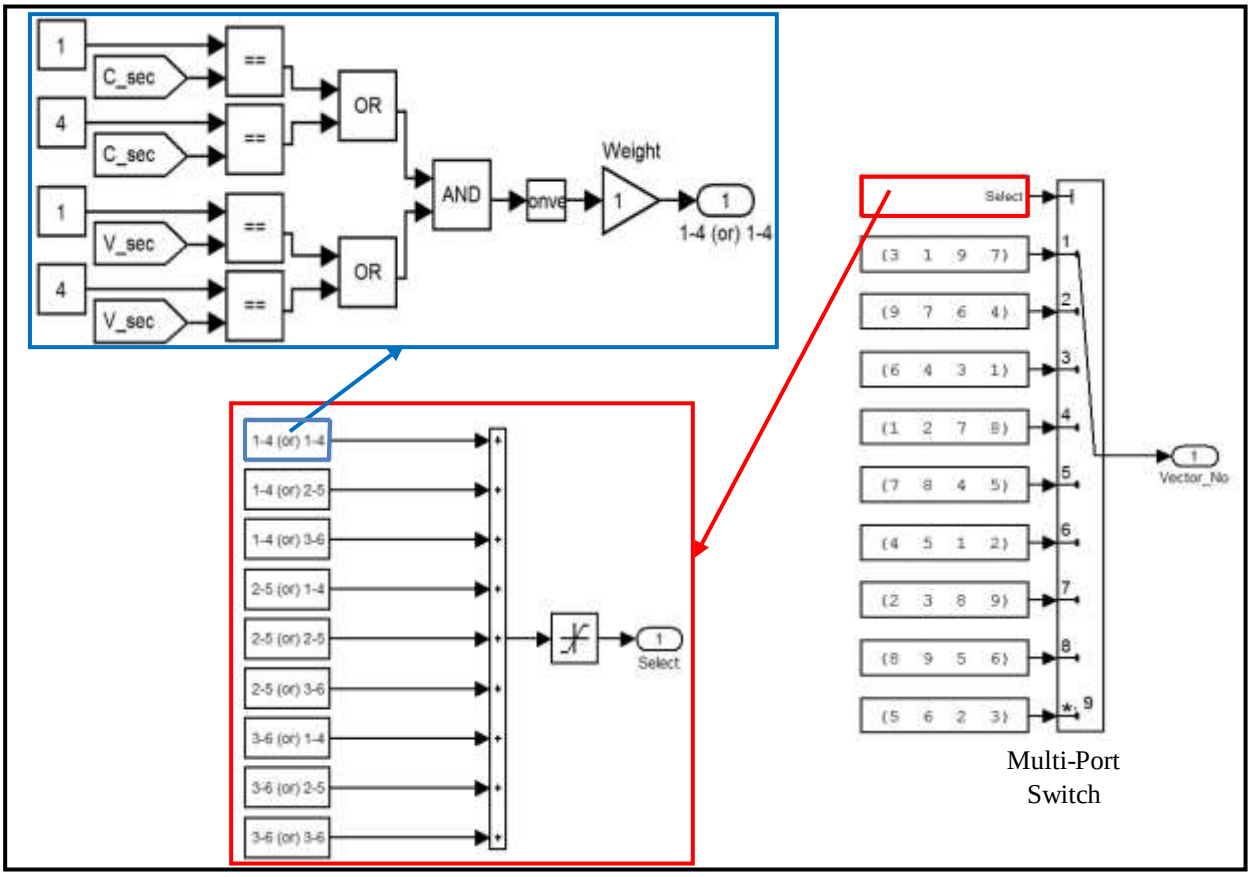


Figure 2.26 Vectors Identification (Implementation of Table 2.3)

Block 2: Vector No sign Assignment

This block assigns a positive or negative sign based on the duty cycle formulae in Equations (2.8) to (2.11). It checks for the two conditions $(-1)^{(1+ K_v + K_i)}$ and $(-1)^{(K_v + K_i)}$, and determines which vectors are to be assigned the negative sign. This is shown in Figure 2.27.

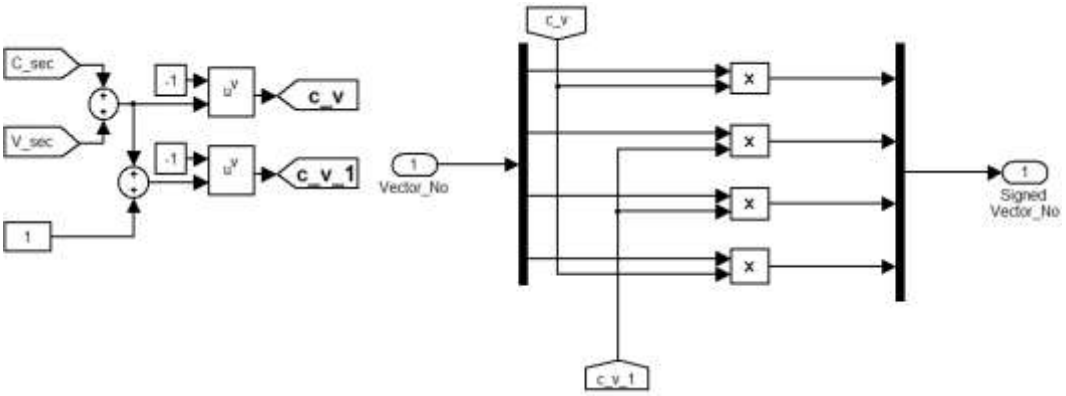
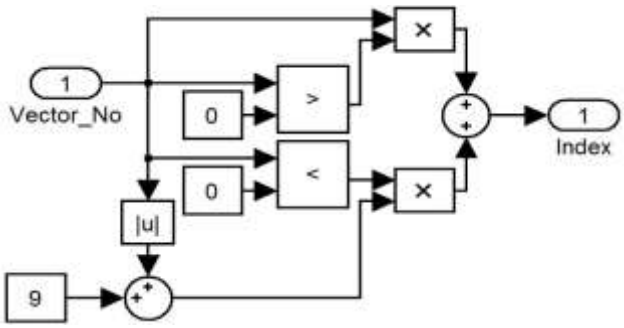


Figure 2.27 Sign Assignment for Vectors

Block 3: Vector Index Selector

This block converts the vector numbers from [±1 to ±9] to [1 to 18]. The positive numbers +1 to +9 are kept as such. The negative numbers are converted to a positive number from 10 to 18. Figure 2.28 shows the vector number conversion.



v

Figure 2.28 Convert negative vector number and obtain vector indices

Table 2.6 shows the final vector indices corresponding to the Vector Number.

Hence, we have the 18 vectors now. The purpose of converting the vector numbers to a positive integer is to use a multi-port switch to pass the corresponding switching state when the vector index appears on the “Select” line of the switch. This is done in Block 4.

Block 4: Vector Selector

Figure 2.29 shows the Vector Selector block.

Table 2.6 Index corresponding to the vector number

Vector No	Index
+1 to +9	Same
-1	10
-2	11
-3	12
-4	13
-5	14
-6	15
-7	16
-8	17
-9	18

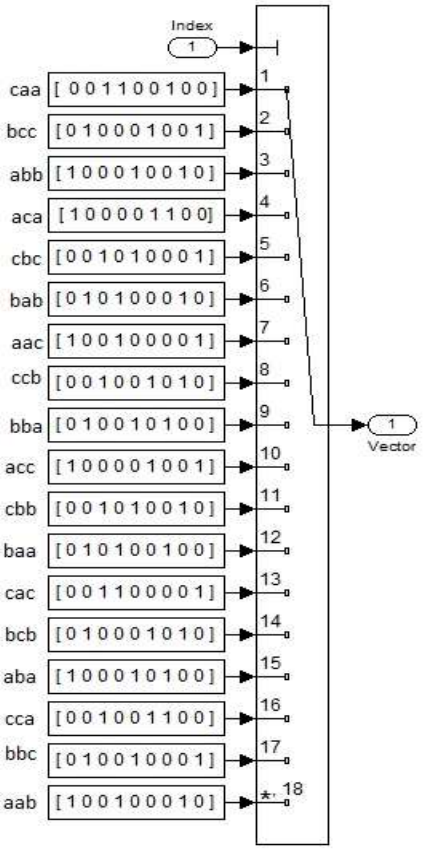


Figure 2.29 Vector Selector

Table 2.1 and Table 2.5 are required as a reference for identifying the switch state corresponding to the vector index. The switch state is denoted as a 1×9 matrix using a constant block. The 9 columns denote the pulses to the nine bidirectional switches. The order of the switching pulse has to be carefully observed. This is one place where there is a high probability of manual error. Figure 2.30 shows the order in which the pulses are mentioned in Figure 2.29. One may write the 1×9 matrix, however they want, but has to ensure extraction of data in the same order.

The switch SAa to SCc can be seen in the MC topology shown in Figure 2.2. Some use different representations where inputs are referred using small letters, and outputs using capital letters. Whatever be the case, one has to be careful and recheck this block many a time.

The pulses obtained from the DSVM Generator, as shown in Figure 2.31 are sent into a four step commutation sequencer which takes care of the commutation issues in the matrix converter.

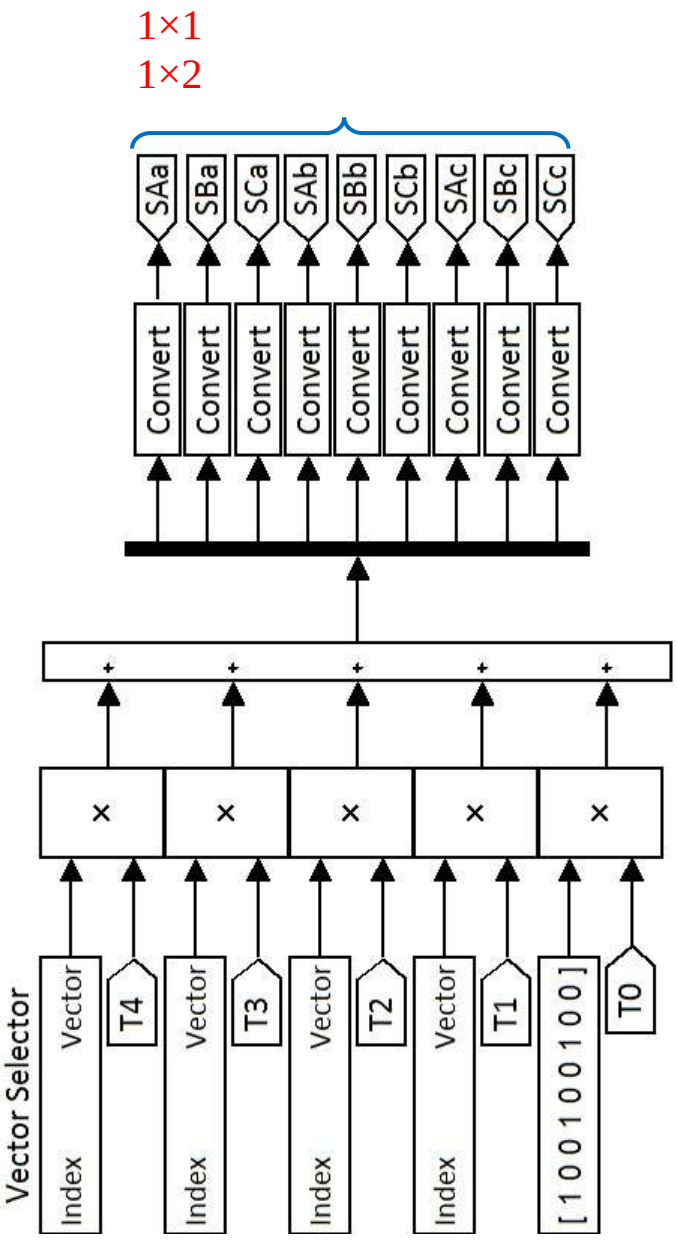


Figure 2.30 Pulses to MC switches

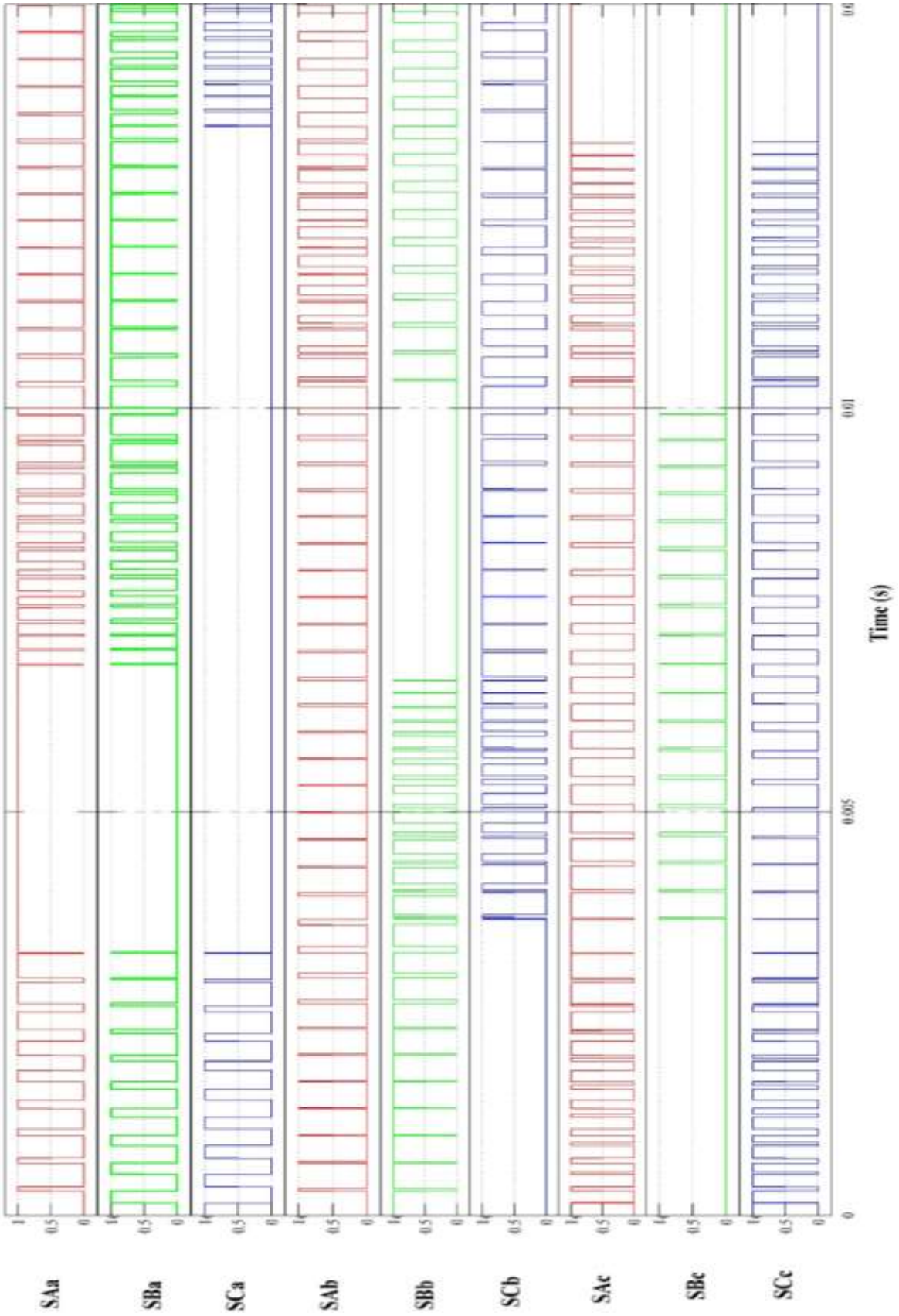


Figure 2.31 Switching Pulses to MC

2.5 IMPLEMENTATION OF FOUR-STEP COMMUTATION

This section deals with the commutation of bidirectional switches in the MC. Ideally, the switches have to be switched on/off instantaneously, which is not the case as each switch has a minimum turn-on and turn-off time. This time interval has to be specified in order to avoid a short circuit between input terminals. In full-bridge converters, free-wheeling diodes take care of the circulation of load current while the IGBTs get commutated. This is not the case in the matrix converter.

The primary difficulty in practical implementation of a matrix-converter based drive system is the absence of inherent freewheeling paths in the converter. Hence, the sequence of commutation of the load current from one input phase to the other has to be explicitly specified, and included in the DSVM algorithm itself. Otherwise, a short circuit may occur between two input phase terminals. While specifying the sequence of commutation of devices, care has to be taken to ensure that the inductive load current is not interrupted. If at any instant of time the load current is interrupted, the high $L\frac{di}{dt}$ leads to excessive voltage stress on the semiconductor devices.

There are 3 types of commutation techniques, based on the data that is required for safe commutation. The first requires only the current direction, the second requires only voltage polarity, and the last requires both, and is called mixed commutation. Here, we are concerned with the current direction-based techniques. Among the two-step and four-step techniques under this category, the four-step commutation is considered to be the safest among all the techniques available. Hence, it is used in this work, and a detailed outline of the technique is presented, along with implementation in MATLAB/Simulink and MATLAB/Xilinx.

2.5.1 Four-Step Commutation Theory

The bidirectional switches of the MC are connected in a common emitter configuration, as can be seen in Figure 2.32. The two IGBTs are connected with two diodes in anti-parallel configuration. The diodes provide the reverse-blocking capability of the IGBTs and do not behave as free-wheeling diodes, like they do in traditional inverters. The difficulty in commutation of current arises due to the absence of a freewheeling path in the converter.

In the four-step commutation technique, the load current is commutated from one phase to another in four steps. Each step involves the turning on/off the incoming and outgoing switches.

Consider the load terminal A is connected to input terminal ‘a’ initially as shown in Figure 2.32. The switches SaAp and SaAn in module SaA will be in “on” state. The switch SaAp conducts the load current when it is positive, while SaAn conducts the load current when it is negative.

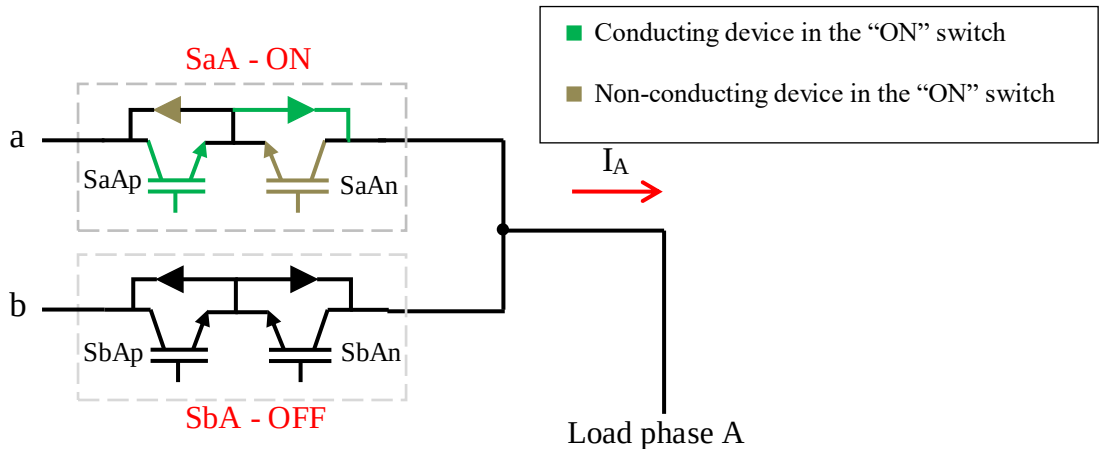


Figure 2.32 Load phase A connected to the input phase ‘a’

Say at one instant of time, the input phase b is to be connected to load terminal A. The switch SbA has to be switched on, and SaA has to be switched off. Table 2.7 gives the commutation sequence for switches when load current is positive/negative.

Table 2.7 Four-step Commutation sequence

Step No.	POSITIVE I_A	NEGATIVE I_A
I	Turn OFF non-conducting switch in the outgoing module (SaAn)	Turn OFF non-conducting switch in the outgoing module (SaAp)
II.	Turn ON the switch that will conduct the current in incoming module (SbAp)	Turn ON the switch that will conduct the current in incoming module (SbAn)
III	Turn OFF the conducting switch in outgoing module (i.e., SaAp)	Turn OFF the conducting switch in outgoing module (i.e., SaAn)
IV	Turn ON the switch that will not conduct the current in the incoming module (i.e., SbAn)	Turn ON the switch that will not conduct the current in the incoming module (i.e., SbAp)

Figure 2.33 shows the sequence of commutation when I_A is positive.

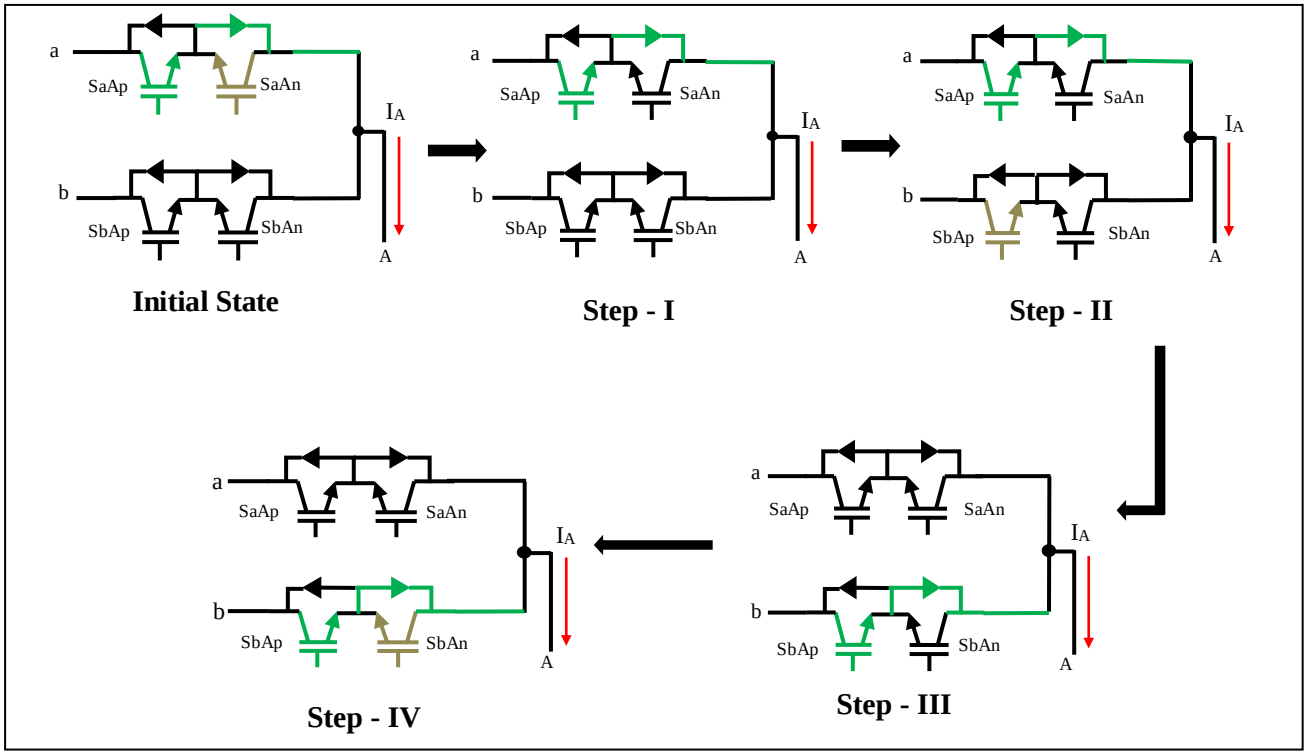


Figure 2.33 Sequence of commutation of devices when I_A is positive

Note that those switches that are green in colour are “ON”, and those that are in black are in “OFF” state. A brown colour indicates a switch that has a high gate pulse (ON state), but is in the non-conducting state as it is reverse-biased.

The time interval between two steps in the sequence has to be fixed so that the “dead time” is larger than the minimum time required for the IGBT turn ON/OFF, whichever is greater. This information is obtained device manufacturer.

The device used here is the APTGT150DU120G, for which the minimum time required for turn on and turn-off are 320 ns and 495 ns respectively when carrying a current of 150 A under steady state at 25˚C. We will never be using this device to its full capacity, yet the dead time is fixed to a safe value of 600 ns. This dead time could be generated using an RC network connected to the gate circuit, as is done conventionally for inverters. The problem that raised when using this method for an MC would be that even though a delay between the two incoming switching pulses is provided, no delay is introduced between the 2 switches in a module, which implies that a freewheeling path cannot be created. Hence, one has to go for a logic circuit that can generate and regulate the commutation sequence between the four switches involved with a dead time of 600 ns between each transition.

One such circuit was proposed by Piriyawong (2007), and is shown in Figure 2.34 for the safe commutation of the MC switches. The circuit works on a clock with a frequency of 1.667 MHz. The four D-FFs employed introduce the required delay while the combinational logic gates decide the state of the switches depending on the current direction in that phase, indicated as the CS signal.

The same circuit was implemented for the pulses to the other 6 switches connected to phases ‘B’ and ‘C’. The overall module looks like the one shown in Figure 2.35.

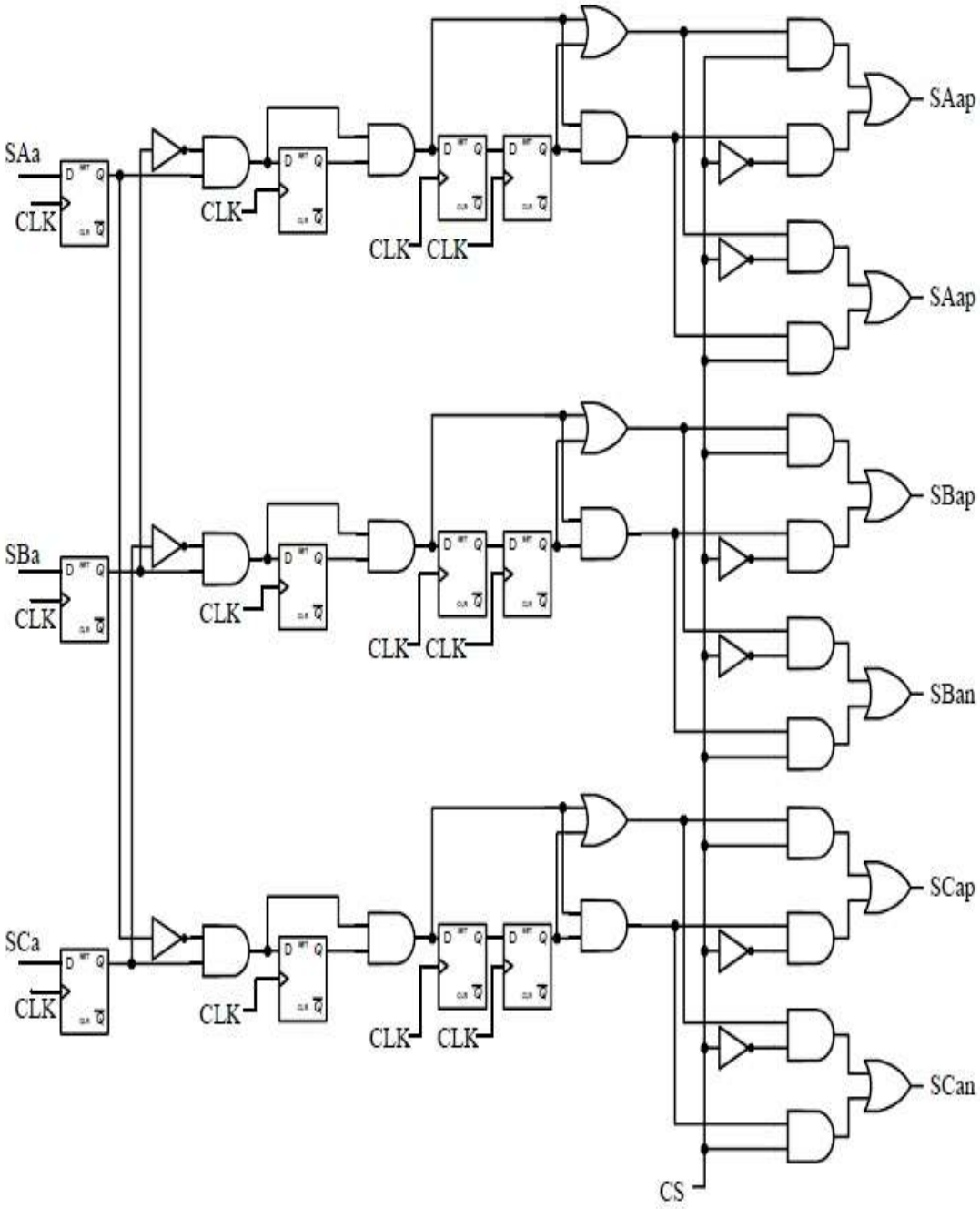


Figure 2.34 Sequential logic circuit that implements four-step commutation for one phase

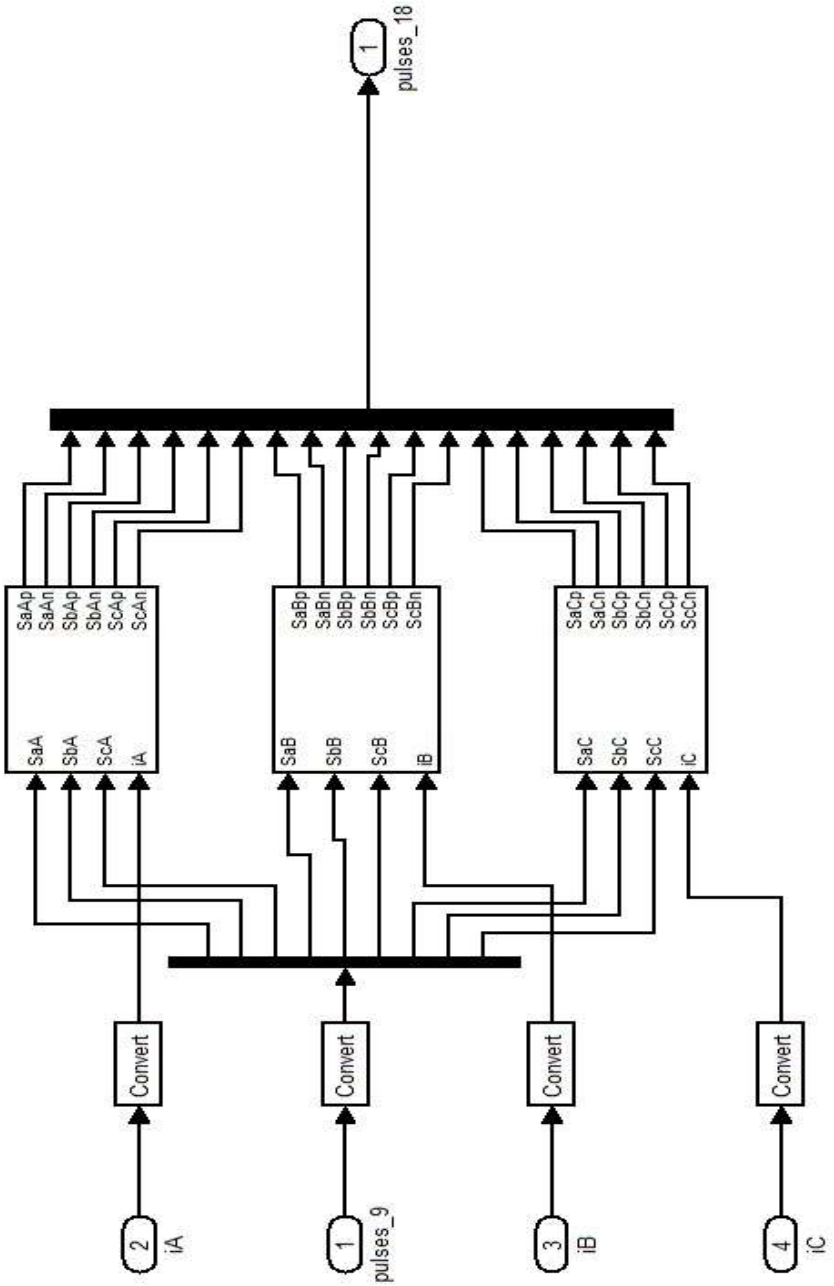


Figure 2.35 Four step sequencer for all load phases.

The pulses from the DSVM algorithm and the direction of current through each load phase are obtained are sent into, the above four step commutation circuit. Using this information the circuit generates the switching pulses for the 18 switches. The pulses of load Phase A switches are shown in Figure 2.36 for positive and negative directions of load current respectively.

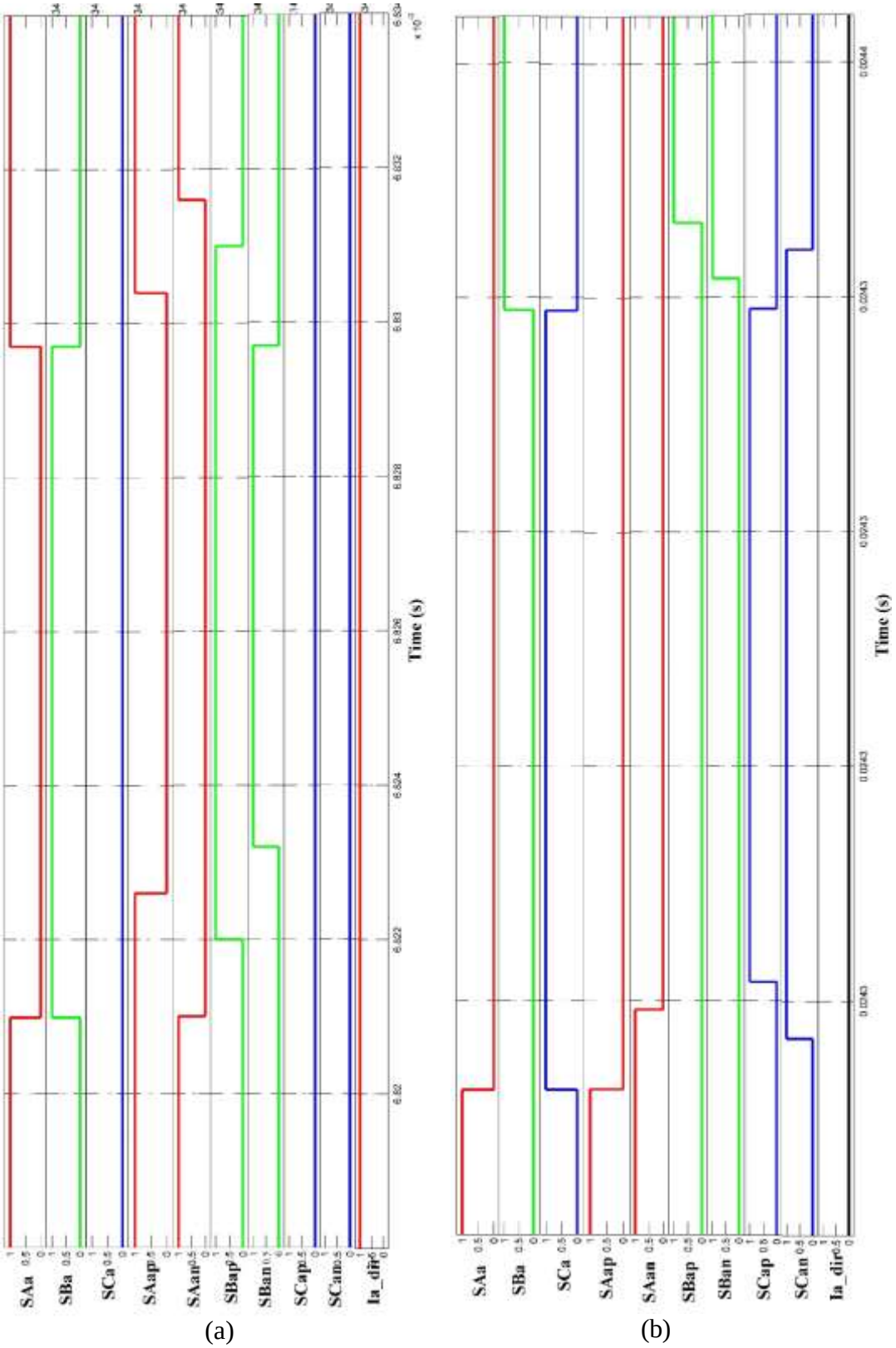


Figure 2.36 Commutation sequence when load current is (a) Positive (b) Negative

2.6 SIMULATION RESULTS:

The MC – RL load system was triggered using the DSVM algorithm. A 3-phase sine wave of 25 Hz frequency was given as the voltage reference. The input phase voltage itself is given as the reference for the input current. The parameters used for the simulation of the DSVM for matrix converter are listed in Table 2.8.

Table 2.8 – Parameters for simulation of Matrix converter

PARAMETER	VALUE
Supply Frequency	50 Hz
R_{fL}	100 Ω
L_f	3 mH
R_{fC}	50 Ω
C_F	20 μF
R_L	8 Ω
L_L	26 mH
Switching Frequency	3 kHz
Output Frequency	25 Hz
Phase Voltage	230V
Input Phase angle	0˚

The simulation results are shown for the two cases. The first, for the MC without an input filter. This will show how the input filter affects the output voltage and input current waveforms. The second case would be for the original system, with an input filter.

Case 1: No input filter connected

The output voltage waveform was obtained at the set frequency of 25 Hz, and is shown in Figure 2.37.

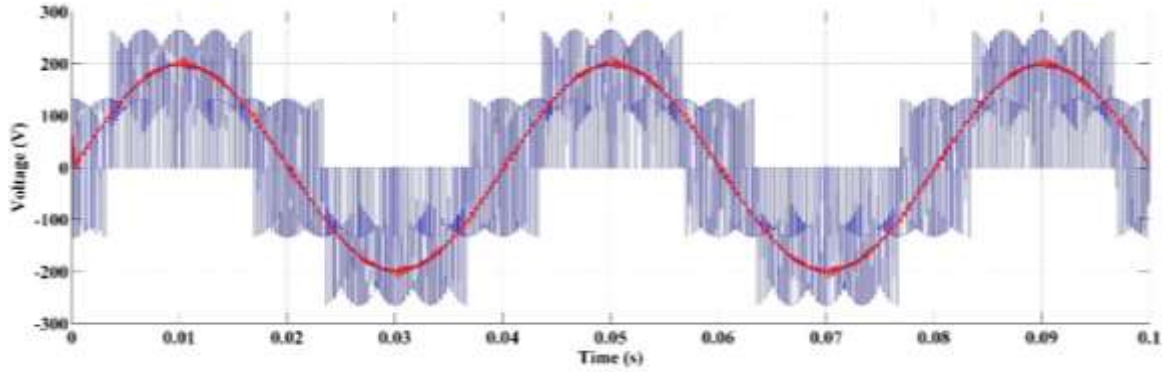


Figure 2.37 Instantaneous and Average Output phase voltage waveform

The waveform obtained is the ideal MC output phase voltage waveform, found in most textbooks. Due to absence of the filter capacitance, high $\frac{dv}{dt}$ is seen, from 0 V to 254 V, subjecting the switches to high stress. The input current waveform in the absence of an input RLC filter can be seen in Fig. 2.38.

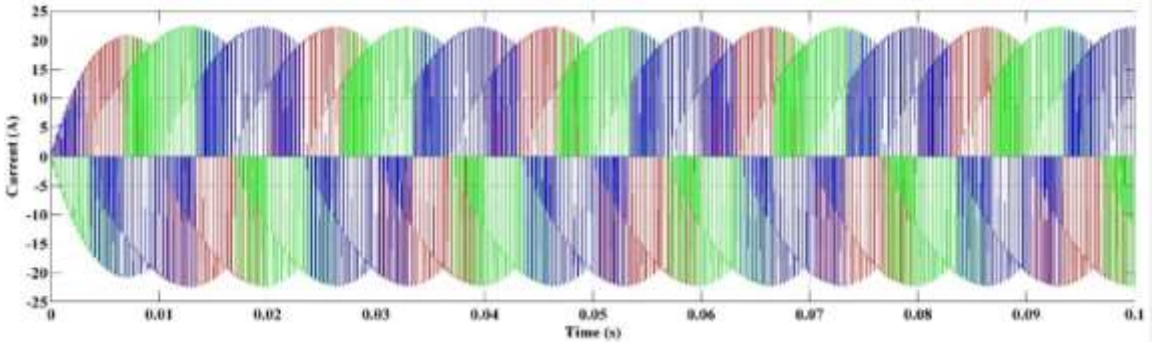


Figure 2.38 3-phase Input current of MC without input filter

In the absence of the input filter inductance, the input current is not sinusoidal, due the $\frac{di}{dt}$ not being suppressed. The instantaneous output line-line voltage waveform and its average waveform are shown in Figure 2.39.

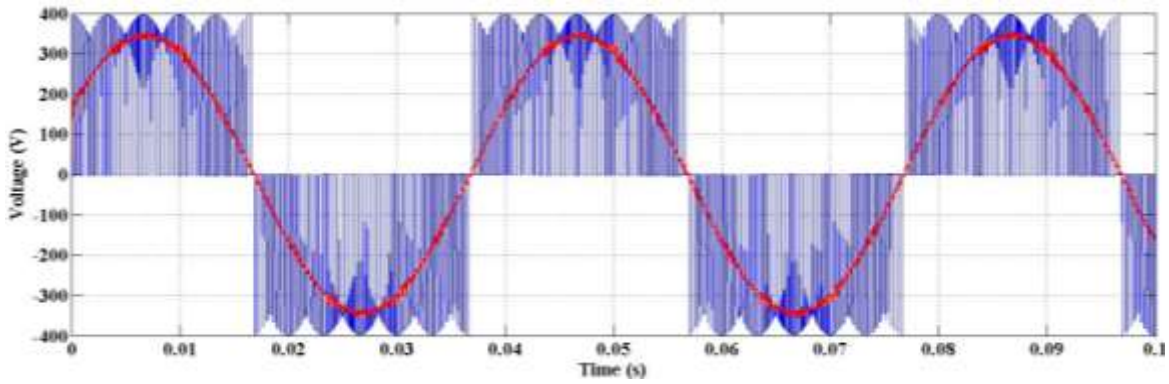
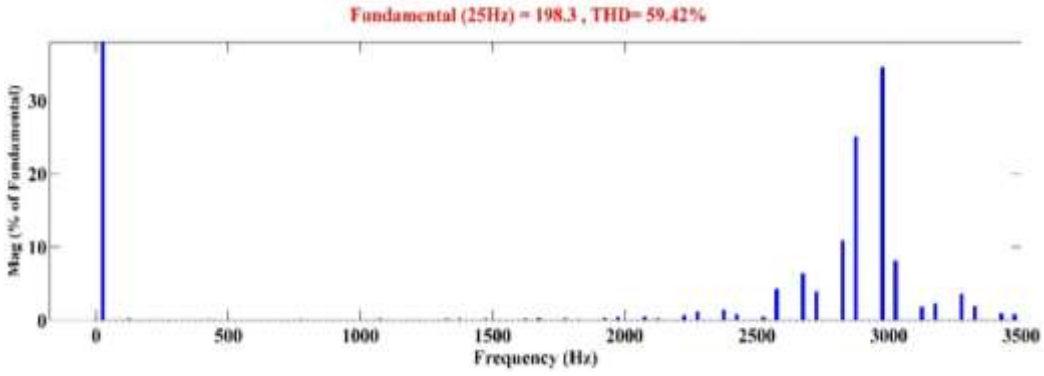
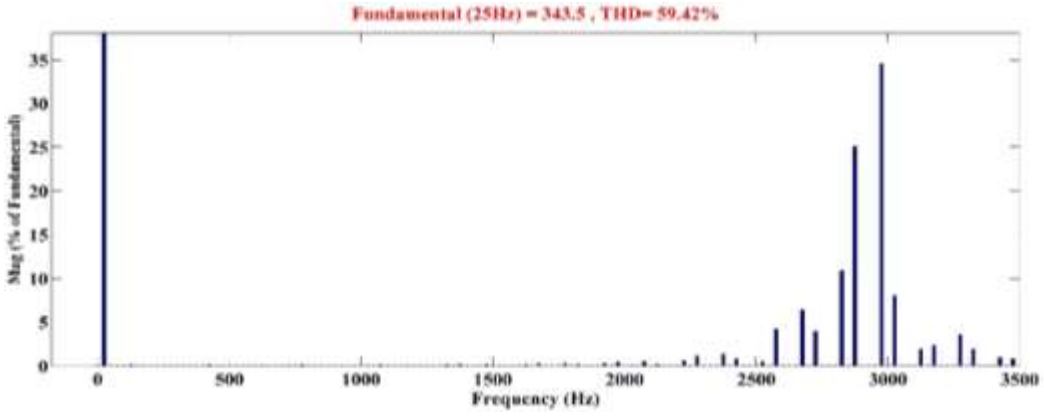


Figure 2.39 Instantaneous and average waveforms of the output line-to-line voltage

The THD and harmonic spectrum of the mean output phase voltage and line voltage waveforms are shown in Figure 2.40. It can be seen that with the MC, the THD of the output voltage waveforms is very small, and within the IEEE Standards' allowable ceiling of 5 %. It is obvious that the THD of the input current would be very high, and hence, the input RLC filter is inevitable.



(a)



(b)

Figure 2.40 Harmonic Spectrum of (a) Output Phase voltage (b) Output line voltage

Case 2: With Input RLC Filter

With the inclusion of the input RLC filter, the output voltage and input current waveforms are observed. The output phase voltage and its THD are shown in Figure 2.41. The output line-to-line voltage is shown in Figure 2.42 along with its harmonic spectrum and THD. As compared with the previous case, one can observe that the waveforms are not the same as in Figures 2.37 and 2.39.

There is a significant reduction in magnitude near the peak values of the voltage waveforms. This can be said to be caused due to the filter capacitor, which does not allow a high rate of rise in voltage. The THD of the waveforms has increased by a very small percentage, around 0.01%. This is in the case of an RL load. When one goes for an adjustable speed drive, the THD will increase further.

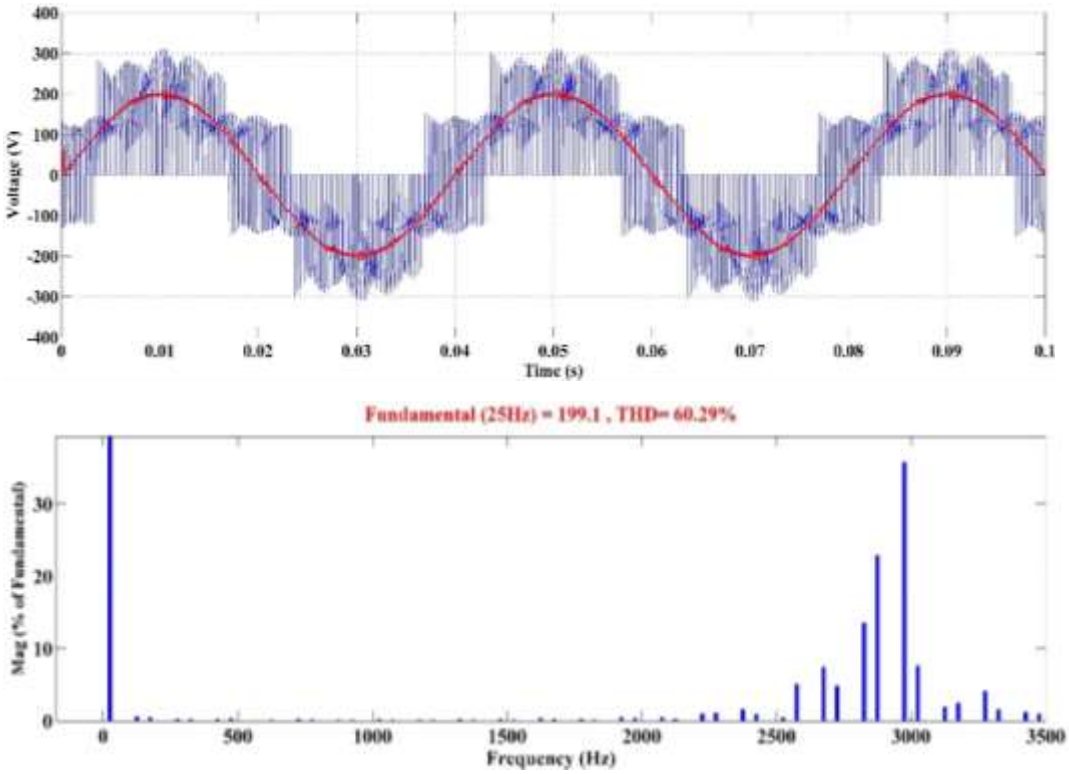


Figure 2.41 Output Phase Voltage and its Harmonic Spectrum with Input filter

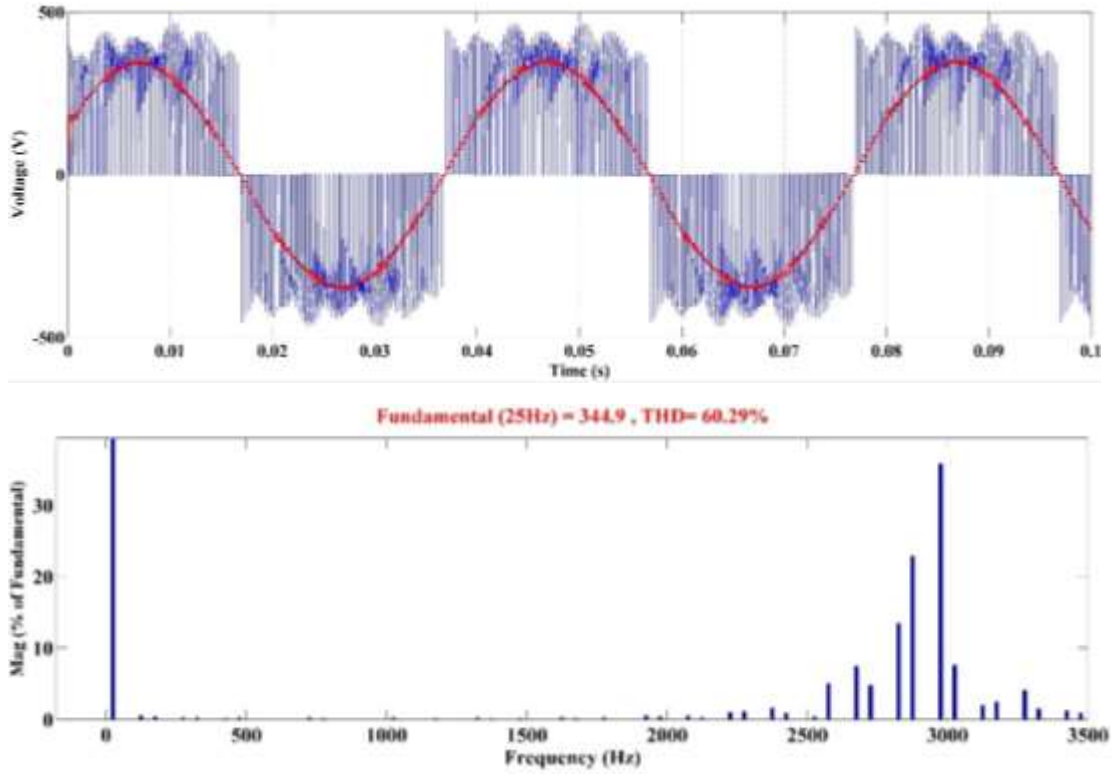


Figure 2.42 Output line-to-line voltage and its harmonic spectrum with input filter

The input current waveform with filter connected at the terminal is shown in Figure 2.43 along with its THD and harmonic spectrum. The waveform is sinusoidal, and the THD is only 0.87 %, which is well within the allowable range of 5 %. The phase relationship with the input voltage is shown in Figure 2.44.

The input current is approximately in-phase with the respective phase voltage. The phase angle difference is very small, 1.8º resulting in a power factor of 0.9995. Hence, the inclusion of input filter is essential to improve the overall power quality of the current drawn by the converter from the grid, even though there is a slight deviation of the output voltage waveform from the ideal one, resulting in a small increase in the THD.

The load current is dependant only the nature of the load, and is shown in Figure 2.45. The frequency of the load current is 25 Hz, the same as that of the output voltage.

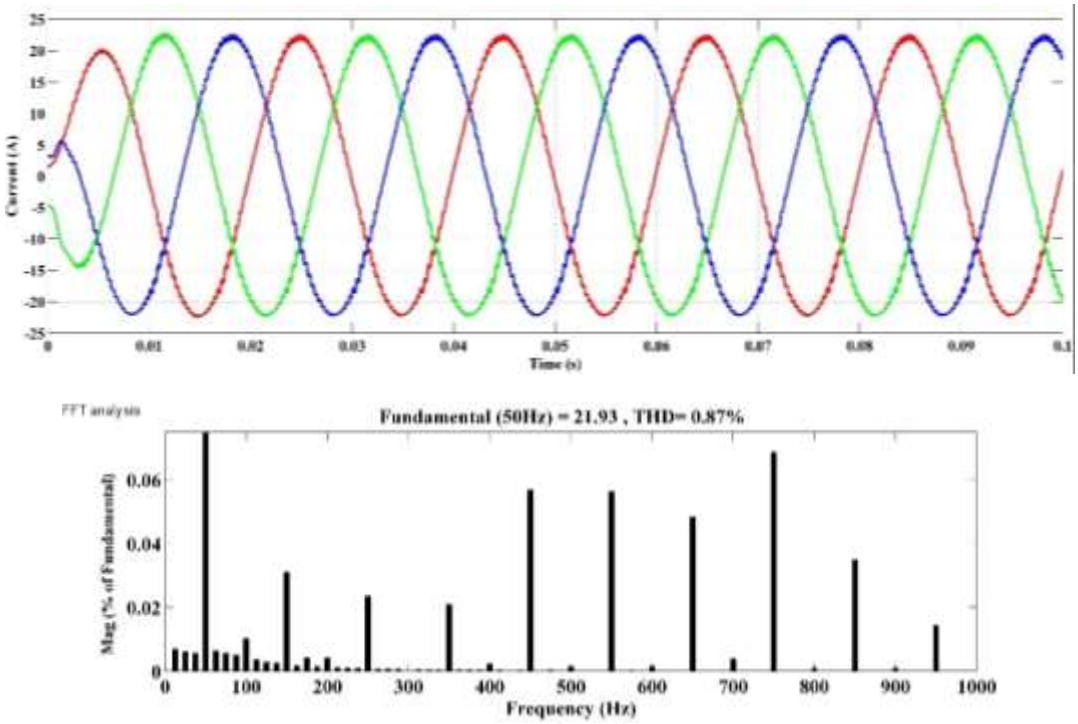


Figure 2.43 Input current when the filter is included, and its harmonic spectrum

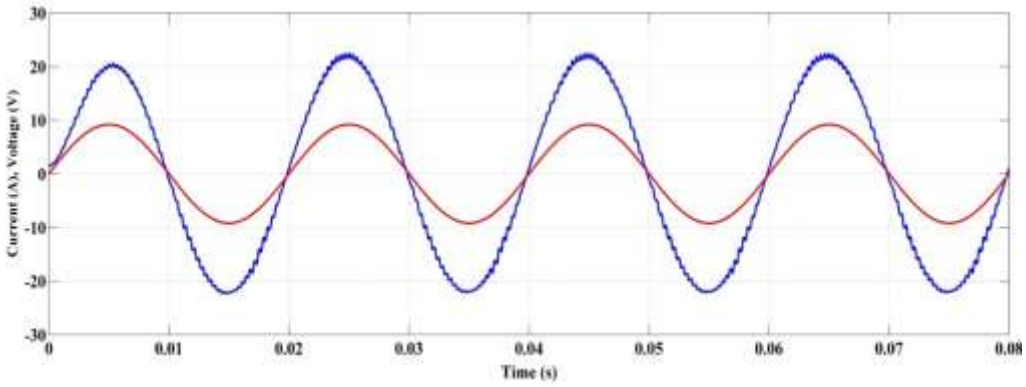


Figure 2.44 Phase relationship between the input current and phase voltage

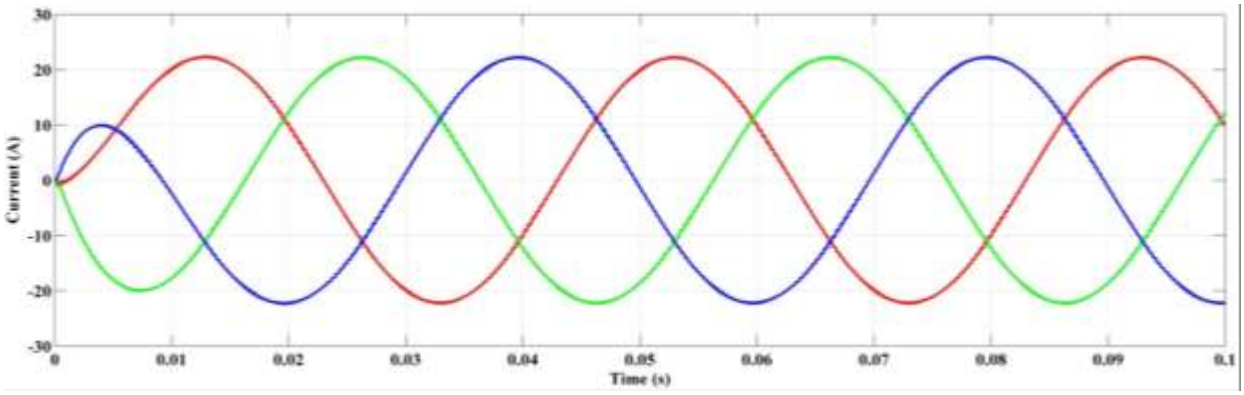


Figure 2.45 Load current

This algorithm is required to be converted to a vhdl code for programming the FPGA controller. The MATLAB/Xilinx Toolbox is a platform that generates a vhdl code using System Generator for the Xilinx model created by the user. This is explained in detail in chapter 10

CHAPTER 3

TESTING OF DFIG FOR ESTIMATION OF MACHINE PARAMETERS

3.1 INTRODUCTION

To efficiently model and analyze the DFIG machine in Matlab/Simulink, the physical parameters of the machine are used for the simulation. The DFIG model 4894 used for this work is a part of Ramsons and the name plate details of the machine is given in Table 3.1 and the DFIG machine along with its test setup is shown in Figure 3.1.

Table 3.1 Nameplate details

Type	Slip Ring Induction Motor
hp	3
Phase	3
Stator Volts (L-L)	415 V
Current	4 A
Exc. Volts	~ AC
Frequency	50 Hz
RPM	1440
Duty	S1
Class	B

Figure 3.1 3 hp DFIG and test Setup

The stator consists of-three phase star connected windings with N_s turns and resistance R_s. The rotor consists of three-phase star connected windings with N_r turns and resistance R_r. The machine parameters were calculated by performing the following tests.

a) DC test

b) Turns-ratio test

c) No load test

d) Blocked rotor test

3.2 DC TEST

This test was performed to find the stator winding resistance of each phase. It is done by applying the known DC voltage, V_{dc}, to the stator terminal and the current, I_{dc}, flowing through is measured with an ammeter. The only circuit parameter limiting the current flow is R_s, which calculated from the test by using Equation (3.1). This test does not induce voltages in stator and rotor windings and eliminates the need to measure the reactance caused by the induced voltages. In addition, it is independent of rotor resistance, R_r, stator reactance, X_s, and rotor reactance, X_r. As the current is DC, there is no induced voltage in the rotor circuit and hence no current flows in the rotor circuit. In addition, the reactance of the motor is zero at DC. Hence, the only quantity limiting the current flow is the stator resistance and this is determined from this test. The test is performed on the each phase of the stator winding and the three values are averaged together. Averaged stator resistance R_{savg}, is calculated from Table 3.2. Figure 3.2 shows the basic circuit for the DC test.

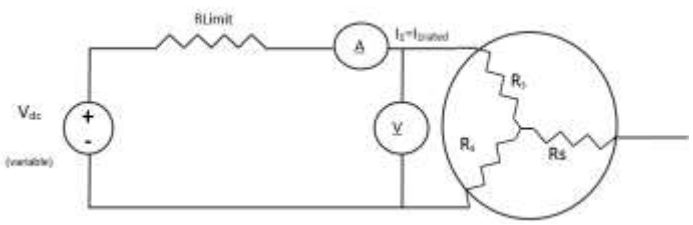


Figure 3.2 Test circuit for the DC resistance test

$$R_s = \frac{V_{dc}}{2I_{dc}} \quad (3.1)$$

Table 3.2 Calculation of the stator resistance

S.No.	V_{dc} (V)	I_{dc} (A)	$R_s = \frac{V_{dc}}{2I_{dc}}$ (Ω)
1	7.35	0.75	4.9
2	10.18	1.1	4.625
3	14	1.55	4.516
4	18	2	4.5
5	22.5	2.5	4.5

R_{savg}= 4.608 **Ω**

Figure 3.2 shows a DC power supply connected to two of the three terminals of the Y-connected DFIG. To perform the test, the current in the stator windings is adjusted to the rated value, and the voltage between the terminals is measured. The current in the stator windings is adjusted to the rated value in an attempt to heat the windings to the temperature, as they would have during normal operation (as winding resistance is a function of temperature). With this value of R_s, the stator copper losses at no load can be determined and the rotational losses can be found as the difference between the input power at no load and the stator copper losses.

The value of R_s, calculated in this fashion, is not completely accurate as the skin effect that occurs when an AC voltage is applied to the windings is neglected. A similar test is carried out to find the rotor resistance Rr. Table 3.3 gives the averaged value R_{ravg} for rotor resistance.

3.3 CALCULATION OF THE TURNS RATIO (K)

The turns-ratio of the DFIG machine is calculated by applying a known AC voltage to the stator terminals and measuring the open circuit AC voltage across the rotor terminals. Equation (3.2) gives the formula for the turns-ratio, K and Table 3.4 gives the calculation of for the turns-ratio.

$$K = \frac{\text{Applied Stator Voltage (V)}}{\text{Measured Rotor Voltage (V)}} \quad (3.2)$$

Table 3.3: Calculation of the rotor resistance

S.No.	V_{dc} (V)	I_{dc} (A)	$R_r = \frac{V_{dc}}{2I_{dc}}(\Omega)$
1	3.39	1	1.69
2	6.6	2	1.65
3	9.8	3	1.63
4	12.9	4	1.62
5	16.2	5	1.62

R_{ravg}= 1.642 **Ω**

Table 3.4 Calculation of the turns-ratio

S.No.	Applied stator voltage (V)	Measured rotor voltage (V)
1	20	10.5
2	26	13
3	30	15

Turns Ratio, K= 0.5

3.4 NO-LOAD TEST

The no-load test calculates the rotational losses and other equivalent circuit parameters required for the blocked rotor test. In this test, the rated voltage and frequency are applied to the stator when the machine is running at no-load condition. The input power, the phase voltage and the phase current are measured for each phase and averaged. Figure 3.3 shows the circuit diagram for the no-load test.

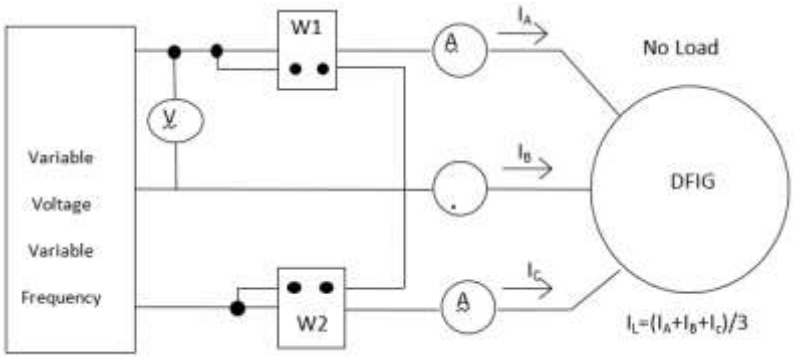


Figure 3.3 Circuit diagram for the no-load test

The no load test of a DFIG measures the rotational losses and provides information about its magnetization current.

The circuit consists of two wattmeters, a voltmeter and three ammeters connected to the stator of the DFIG machine that is allowed to freely rotate. The only load on the motor is the friction and windage losses, so all the power in the motor is consumed by mechanical losses as the slip of the motor is very low. With this very small slip, the resistance corresponding to its power converted, R_2 (1-s)/s, is very much larger than the resistance corresponding to the rotor copper losses R_2 and much larger than the rotor reactance X_2. In this case, the equivalent circuit reduces to the circuit in Figure 3.4.

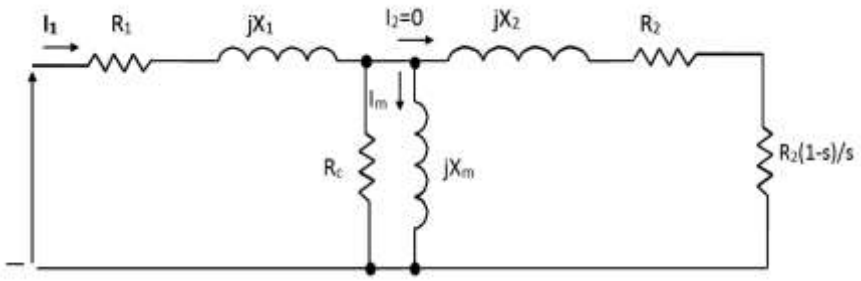


Figure 3.4 (a) Initial equivalent circuit

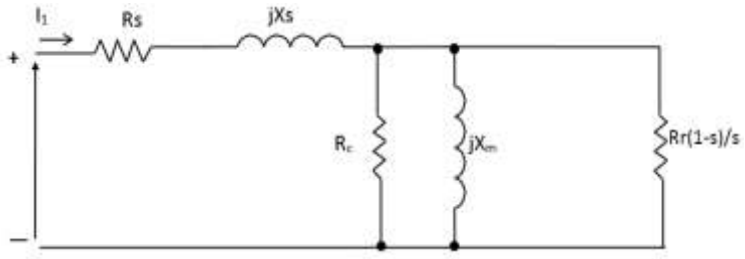


Figure 3.4 (b) Equivalent circuit after neglecting R_r and X_r

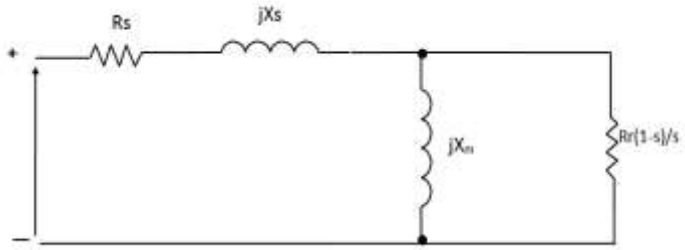


Figure 3.4 (c) Equivalent circuit after combining R_c and R_r/s

Table 3.4 gives the readings obtained from the no load test.

Table 3.4 Experimental readings for the no-load Test

V_{noload} (V)	I_{noload} (A)	Wattmeter (W_1) W	Wattmeter (W_2) W
420	1.7	64	-27

Multiplying Factor = 8

3.5 BLOCKED ROTOR TEST

The third test performed on the DFIG machine is the blocked rotor test, also called as the short circuit test. In this test, the rotor is blocked or locked so that it cannot move. A voltage is now applied to the motor and the resulting voltage, current, and power is measured. Figure 3.5 shows the connections for the blocked rotor test.

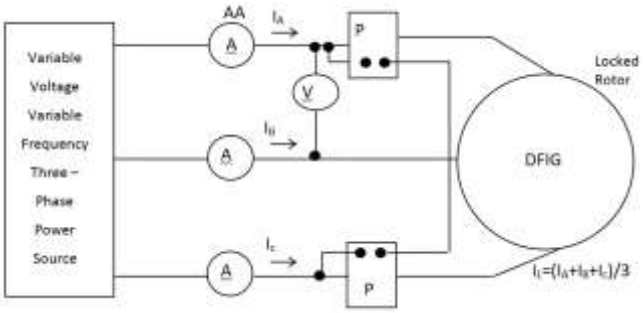


Figure 3.5 Circuit diagram for the blocked rotor test

To perform the blocked rotor test, an AC voltage is applied to the stator and the current flow through it adjusted to approximately the full load value. The voltage, current, and power flowing through the stator are obtained. Figure 3.6 gives the equivalent circuit for the blocked rotor test. Since the rotor does not move, the slip is 1. The rotor resistance $R_2/s= R_2$. Since R_2 and X_2 are small, almost all the input current will flow through them, instead of through the much larger magnetizing reactance X_m. Table 5.3 gives the readings obtained in the short circuit test.

Table 3.5 Experimental readings for the blocked rotor test

Short Circuit Voltage V_{sc} (V)	Short Circuit Current I_{sc} (A)	Wattmeter Reading (W)
112	4	490
110	4	487
116	4	493

Multiplying Factor = 1

3.6 CALCULATION OF DFIG PARAMETERS

From DC resistance test, the stator and rotor resistance was found to be R_s=4.608 Ω and R_r =1.644 Ω.

3.6.1 Calculations for the No Load and Block Rotor Test

No load impedance, $Z_o = \frac{415/\sqrt{3}}{1.55} = 154.5\Omega$

No load resistance, $R_o = \frac{(32*8)/3}{1.55^2} = 35.5\ \Omega$

No load reactance, $X_0 = \sqrt{(z_o^2 - R_0^2)} = 150.36\ \Omega$

Block Rotor Impedance, $Z_{BR} = \frac{116/\sqrt{3}}{4} = 16.74\ \Omega$

Block Rotor Resistance, $R_{BR} = \frac{490/3}{4^2} = 10.208\ \Omega$

Block Rotor Reactance, $X_{BR} = \sqrt{Z_{BR}^2 - R_{BR}^2} = 13.26\ \Omega$

Approximating $X_s = X_r' = 6.633\ \Omega$

Magnetizing Reactance, $X_m = X_o - X_s = 143.849\ \Omega$

Rotor resistance referred to primary, $R_r' = (R_{BR} - R_1)\left[\frac{X_m + X_2'}{X_m}\right]^2 = 6.128\ \Omega$

Rotor resistance, $R_r = 1.532\ \Omega$ (this value of rotor resistance matches the DC resistance test).

3.6.2 To Calculate the Maximum Torque of the DFIG 3 HP Machine

Equations (3.3) to (3.6) give the maximum torque.

$$T_{max} = \frac{3Vth^2}{2w_{syn}\left[R_{th} + \sqrt{R_{th}^2 + (X_{th}^2 + X_2)^2}\right]} \quad (3.3)$$

where, $v_{th} = \frac{jX_m v_\varphi}{R_1 + jX_1 + jX_m}$ (3.4)

$$R_{th} = R_1\left(\frac{X_m}{X_1 + X_m}\right) \quad (3.5)$$

$$X_{th} = X_1 \quad (3.6)$$

Using the above equation, we get $v_{th} = 230$

$$R_{th} = 4.210\ \Omega$$

$$\therefore \textbf{Maximum Torque}, T_{max} = 27.393\ \textbf{NM}$$

Frome the results obtained from the above tests, the machine is simulated in the Matlab/Simulink environment for further analysis. The calculated parameters of the machine are set as the simulation parameters and the maximum torque value is verified.

3.7 MATLAB SIMULATION OF THE 3 HP DFIG MACHINE WITH ESTIMATED PARAMETERS

Figures 3.7 and 3.8 show the Matlab/Simulink model of the DFIG machine used in this work along with its calculated parameters.

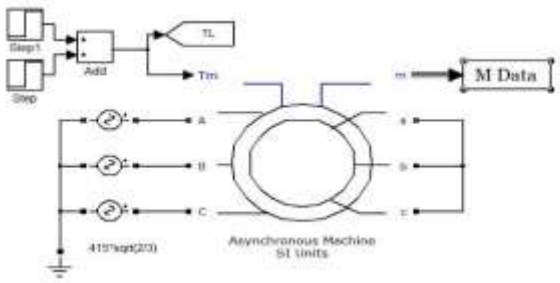


Figure 3.7 Matlab/Simulink model of the DFIG Machine

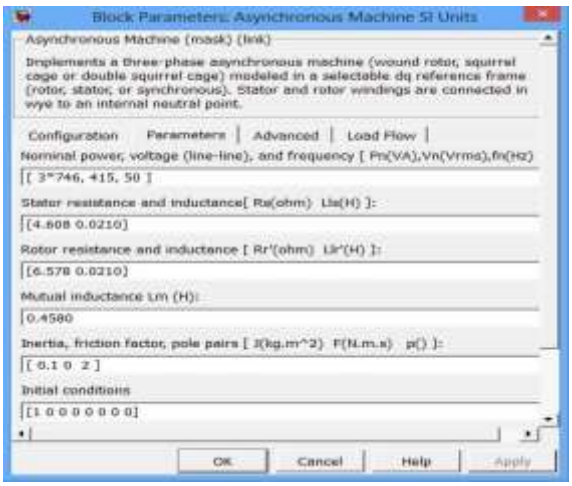


Figure 3.8 Parameters entered in Matlab/Simulink model

Figure 3.9 shows the load torque, speed and the electromagnetic torque of the machine. It is seen that the machine speed is 1500 rpm when load torque is at 0 Nm and is 1000 rpm when the load torque is 26 Nm (T_{max}). When the load torque increases beyond T_{max} (26 Nm) the machine was not able to develop the required electromagnetic torque. This results the speed

tending to infinity in Matlab simulation. It can also be seen that the electromagnetic torque follows the load torque when it is within the permissible value and is at 0 when the load torque is increased beyond the $T_{max.}$

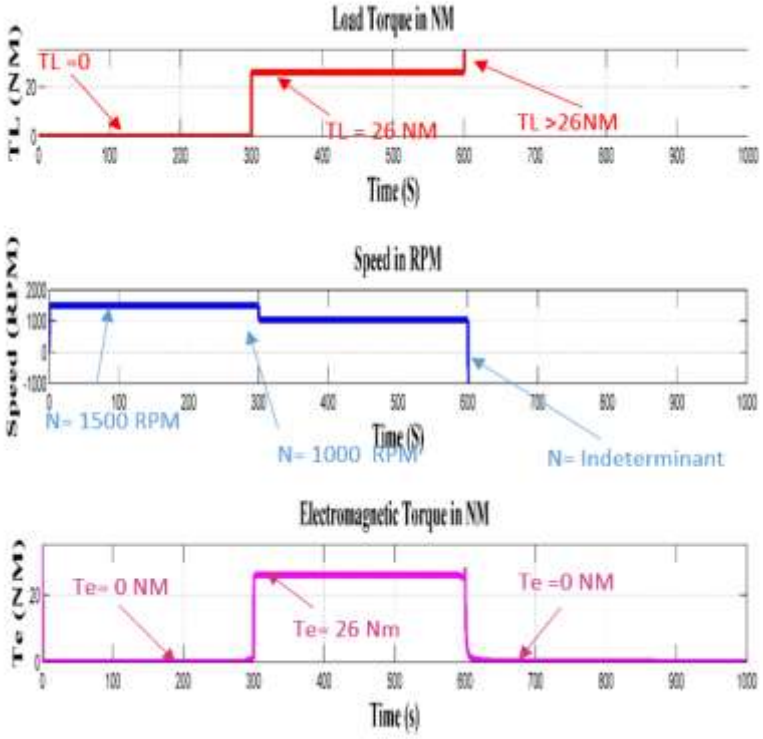


Figure 3.9 Results for load, torque, speed and electromagnetic torque obtained from the scope

A bus selector is used from the Simulink toolbox to obtain the parameters measured, inherently in the machine model. The stator and rotor currents, flux and voltages in the d-q reference frame are extracted, as shown in Figure 3.10. Figure 3.11 gives the Matlab/Simulink model to analyze the stator, rotor and total flux respectively.

Figures 3.12 and 3.13 show the plots of the stator and rotor d-q components, from which the magnitude of the total flux in the machine is plotted in Figure 3.14.

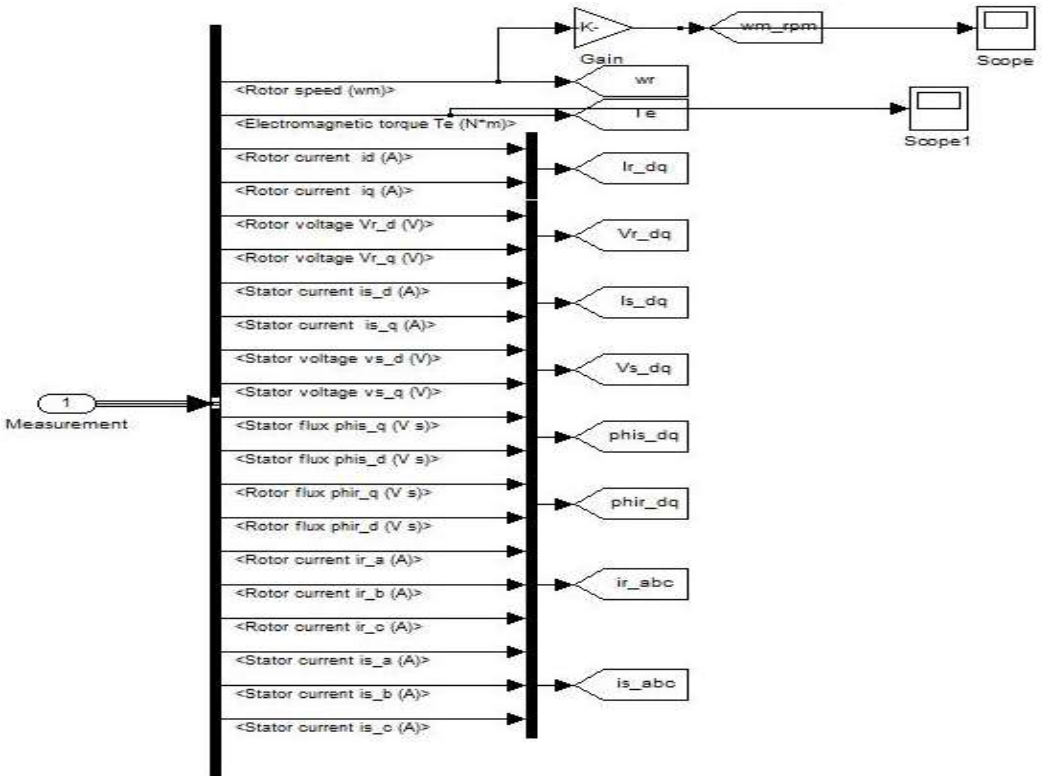


Figure 3.10 Other parameters analyzed in the Matlab/Simulink model of the machine

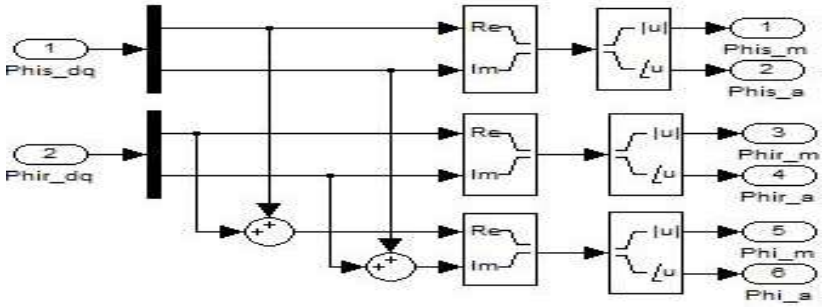


Figure 3.11 Matlab/Simulink model to calculate the magnitude of the flux in the DFIG

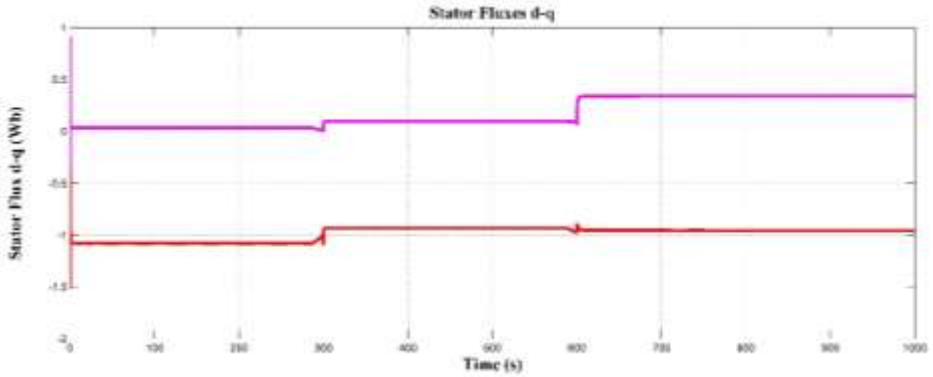


Figure 3.12 Stator flux in d-q coordinates

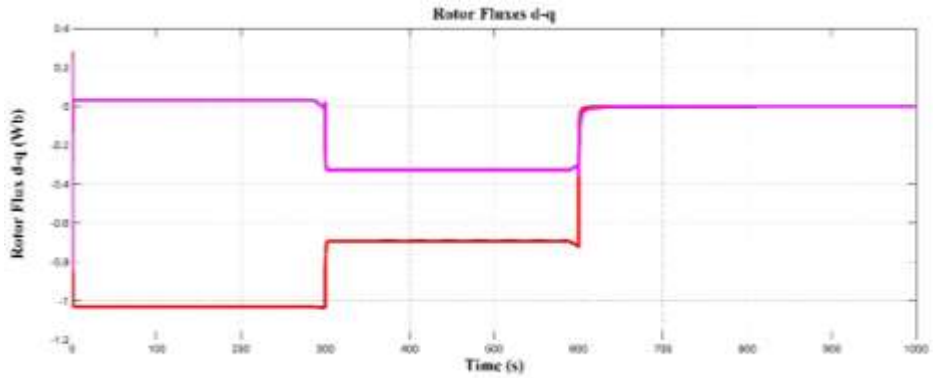


Figure 3.13 Rotor flux in d-q coordinates

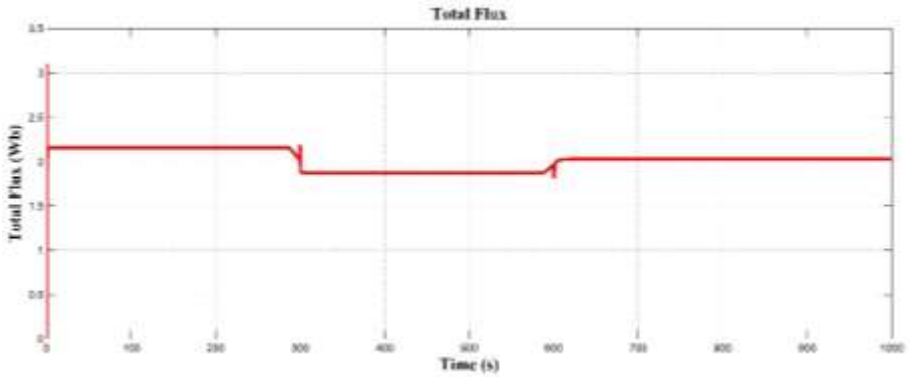


Figure 3.14 Total flux in d-q coordinates

Figures 3.15 and 3.17 show the Matlab/Simulink model to measure the stator and rotor power. Similarly, Figures 3.16 and 3.18 show the scope results of the stator and rotor powers of the DFIG machine, which is simulated as an SCIG with the rotor short-circuited.

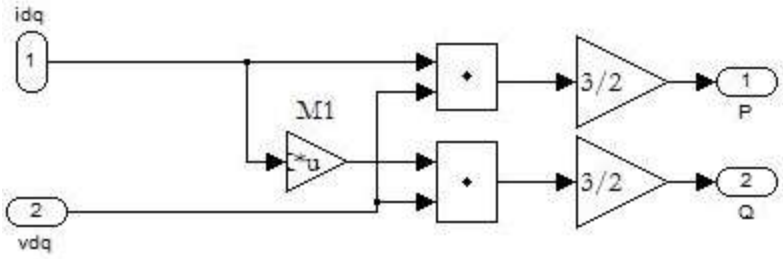


Figure 3.15 Matlab/Simulink model for calculating the stator power

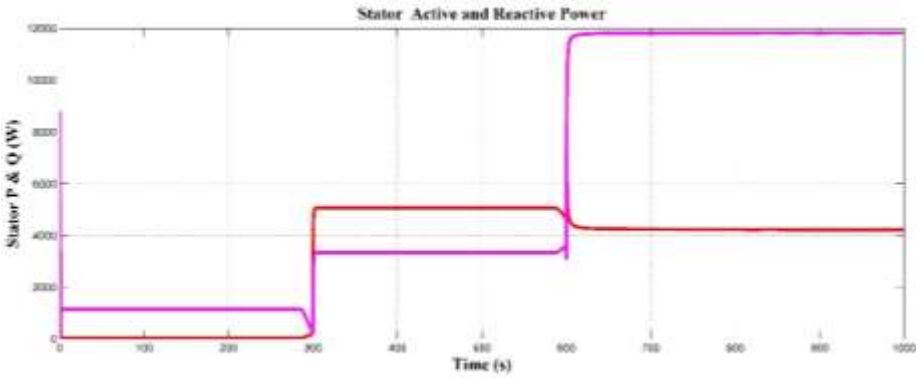


Figure 3.16 Stator active and reactive power

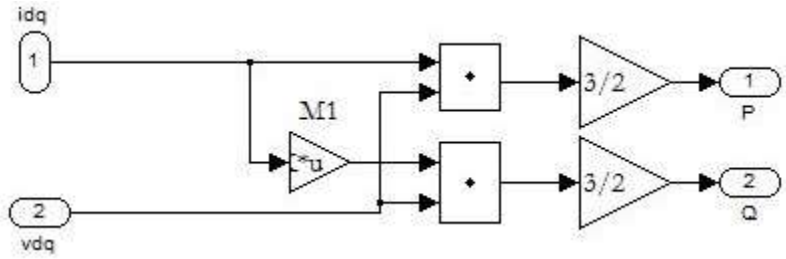


Figure 3.17 Matlab/Simulink Model for calculating the rotor power

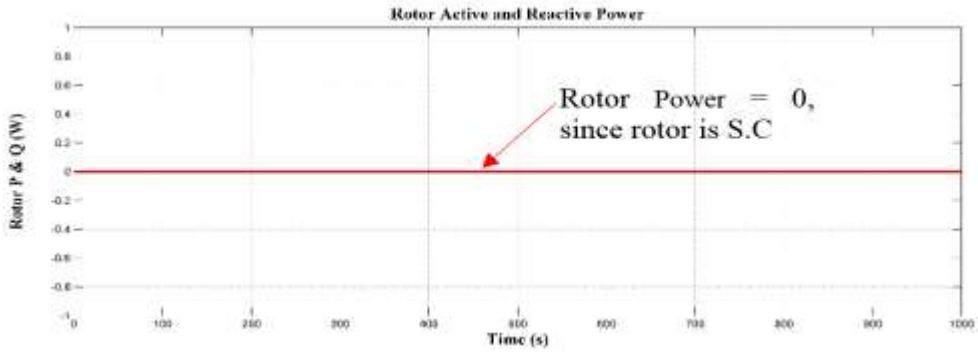


Figure 3.18 Rotor active and reactive powers

Similarly, Figures 3.19 to 3.22 show the stator and rotor voltages and currents, respectively.

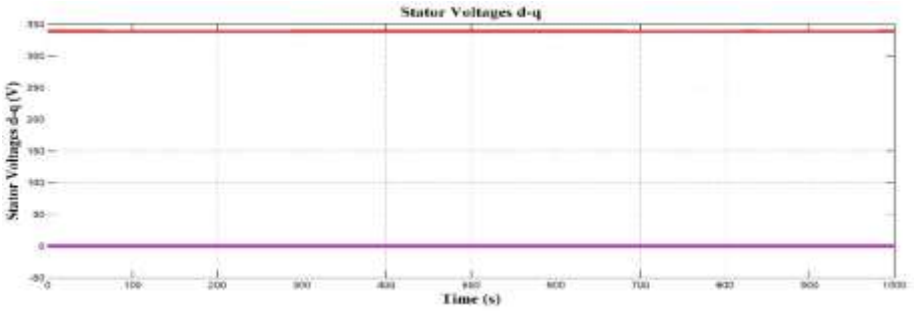


Figure 3.19 Stator voltages in d-q coordinates

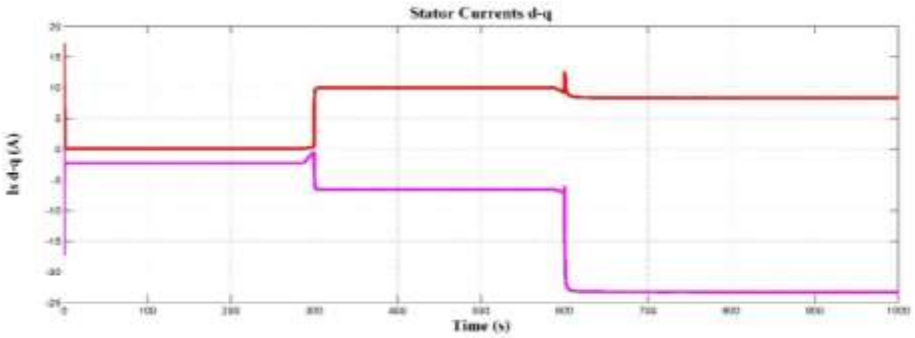


Figure 3.20 Stator currents in d-q coordinates

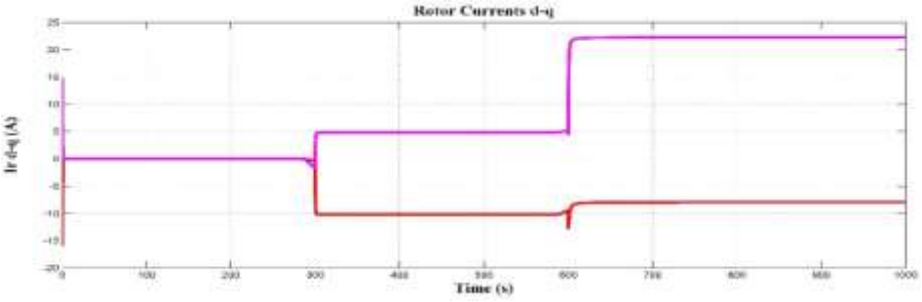


Figure 3.21 Rotor currents in d-q coordinates

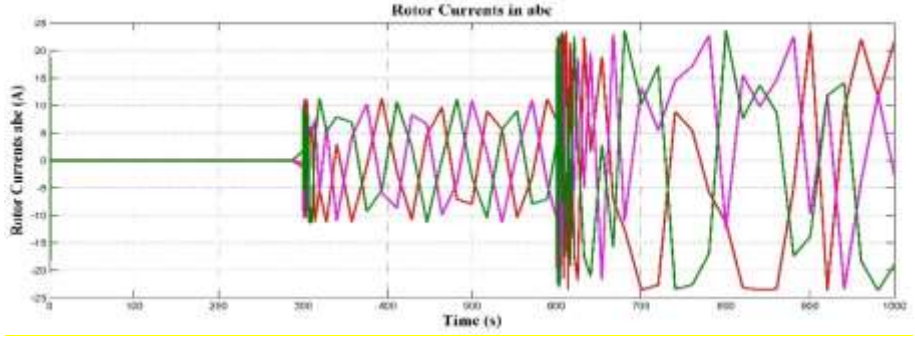


Figure 3.22 Rotor currents in abc coordinates

3.8 DFIM AS A GENERATOR

The asynchronous induction machine is run as a doubly-fed induction generator using a controlled variable voltage source. Figure 3.23 shows the Matlab/Simulink model of the DFIG acting as a generator.

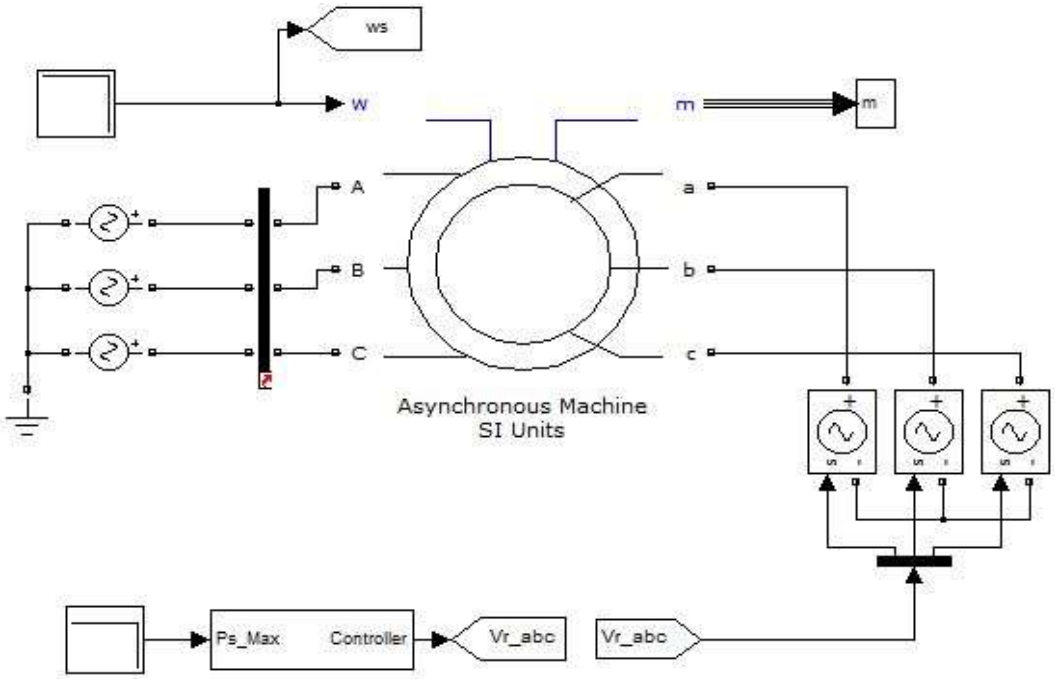


Figure 3.23 Matlab/Simulink model of the DFIM as a generator

Figure 3.24 shows the machine input speed that is set at 167 rad/s from 0 to 4s, and 137 rad/s thereafter.

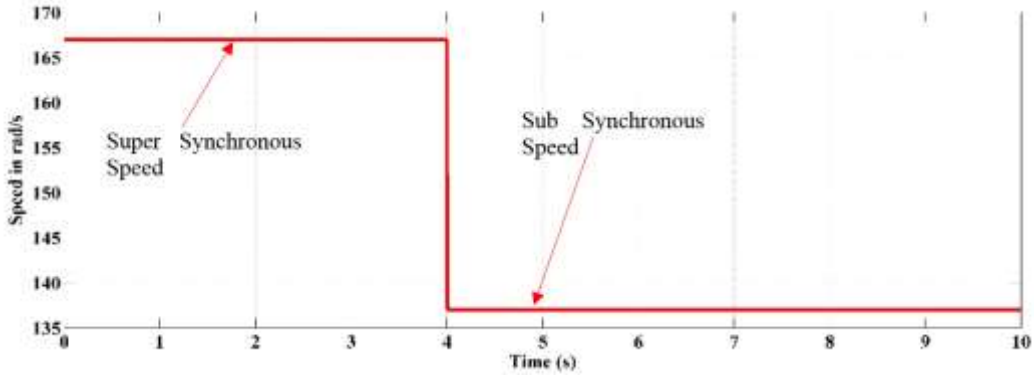


Figure 3.24 Input speed of the DFIG machine

Figures 3.25 to 3.27 show the stator and rotor flux, power and electromagnetic torque developed for sub-synchronous and super-synchronous modes of operation.

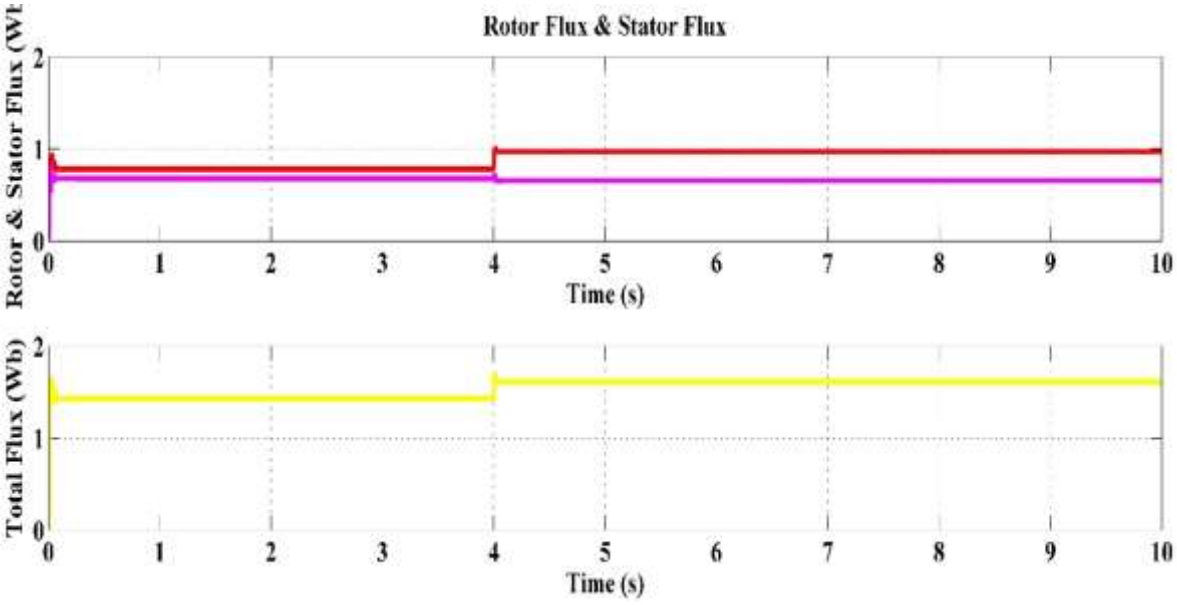


Figure 3.25 Rotor, Stator & Total Flux

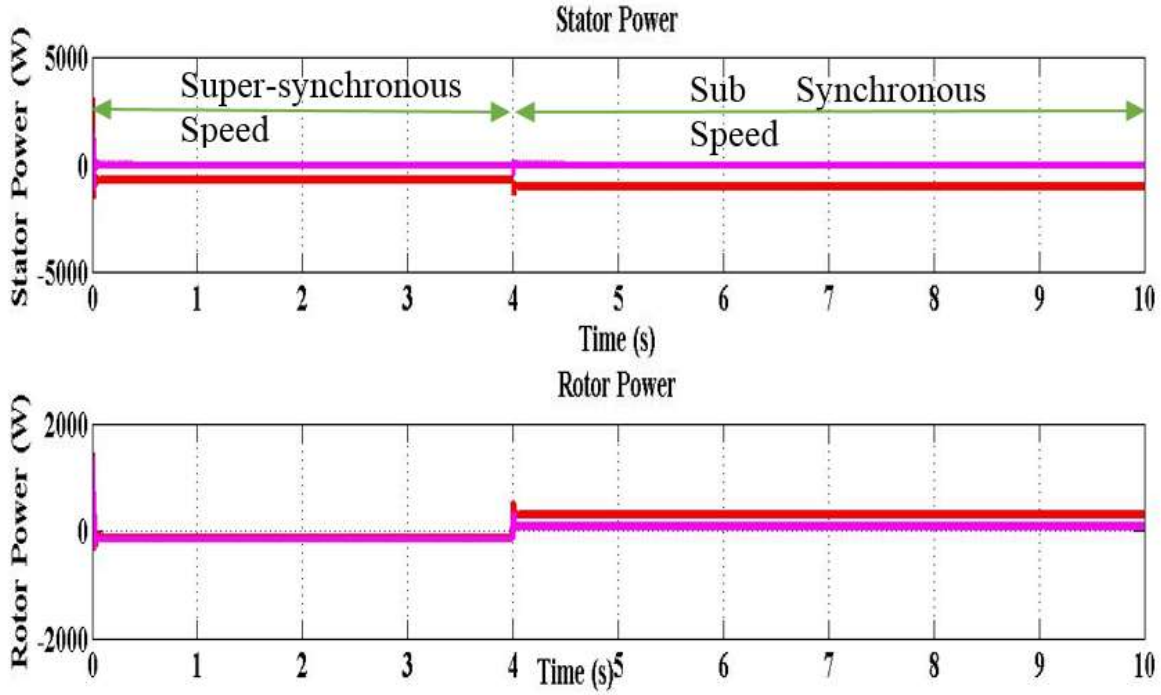


Figure 3.26 Active and reactive powers of the stator and rotor powers

From Figure 3.25, it can be observed that both the stator and rotor deliver active powers at the super-synchronous speed (power is negative) while in the sub-synchronous speed, the stator delivers power while the rotor absorbs both active and reactive power. The reactive

power reference is set at zero for both the cases. This is to ensure that the reactive power drawn by the machine is restricted to a bare minimum.

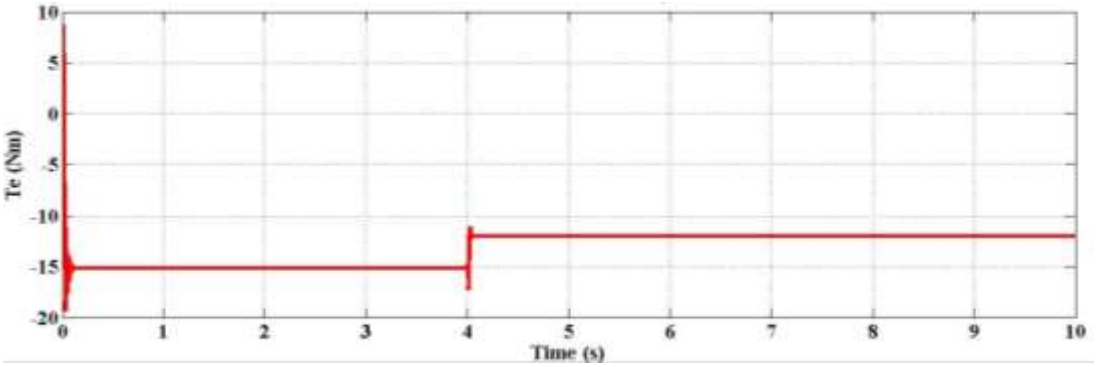


Figure 3.27 Electromagnetic torque for machine operation as Generator

The electromagnetic torque developed is negative, indicating that the machine operates as a generator under sub-synchronous and super-synchronous speeds. This was possible due to the control action that ensures that the machine delivers the required stator power irrespective of the shaft speed.

Hence, the parameters of the machine have been estimated and the behaviour of the machine has been outlined in the Matlab/Simulink environment.

CHAPTER 4

IMPLEMENTATION OF ROTOR SIDE CONTROLLER FOR DFIG USING MATLAB/SIMULINK

4.1 INTRODUCTION

It is necessary to control the stator power of the DFIG connected to the grid. This is accomplished by connecting a power electronic converter to the rotor of the DFIG. The converter is commonly called as the rotor side converter (RSC). The advantages of RSC are: partial rating and reduced size, low losses, and ability to deliver power in sub-synchronous (up to +30% N_s) as well as super-synchronous speeds (up to 30% N_s). The main objectives of the RSC are to maintain the desired stator active power and unity power factor (Q_{ref} =0). Hence, two PI controllers are connected to the RSC in order to satisfy the above objectives. The two PI controllers are called as the active power controller and the reactive power controller. This documentation explains the implementation of the PI controller on the rotor side (rotor side controller) of DFIG based wind energy conversion system.

4.2 IMPLEMENTING THE ACTIVE POWER AND REACTIVE POWER CONTROLLERS IN MATLAB

Figure 4.1 shows the Matlab/Simulink model of the active power and reactive power controllers.

4.3 ROTOR SIDE CONTROL THEORY

Direct Power Control - Space Vector Modulation (DPC-SVM) technique is used to control the stator power. The active power and reactive power command to the controller are externally set. For optimal control action, all the quantities are represented in per unit (p.u.) system. The base power of the system is s_base. Hence, the power is converted to p.u. on the base power.

The terms Ps_p and Qs_p denotes the actual real and reactive powers in p.u. The calculation of actual powers, both real and reactive, requires the values of voltages v_{ds} and v_{qs} and currents i_{ds} and i_{qs} in d-q axis respectively.

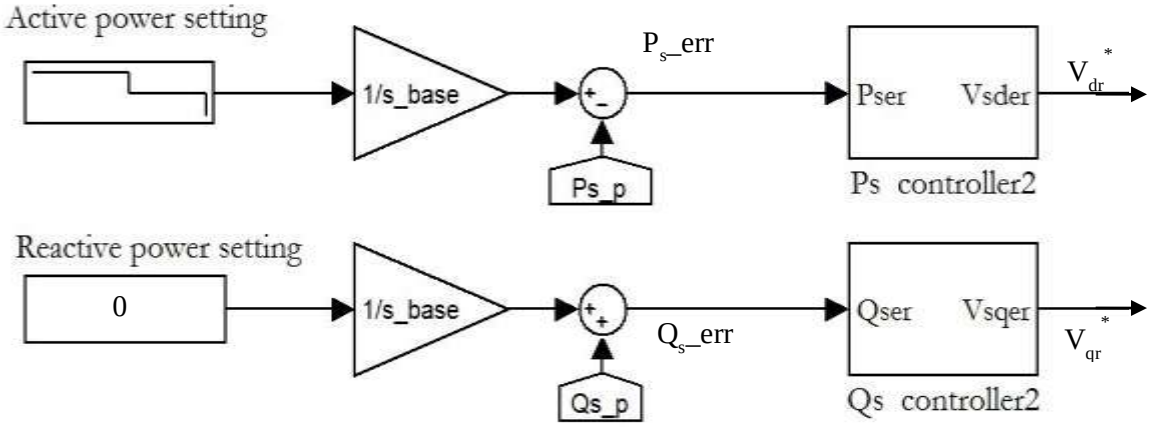


Figure 4.1 Matlab/Simulink Model for the rotor side controller

4.3.1 Calculation of v_{ds}, v_{qs}, i_{ds}, and i_{qs}

The grid voltage V_{abcs} is converted into V_{ds} and V_{qs} and this involves two steps. The first step is to convert the three-phase grid voltage in the rotating reference frame, V_{abcs}, into two-phase voltages in the stationary reference frame, $V_{\alpha\beta}$, using Equation (4.1) in order to find the grid angle, θ.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (4.1)$$

Equation (4.2) gives the grid angle θ.

$$\theta = \tan^{-1}\frac{V_\beta}{V_\alpha} \quad (4.2)$$

The second step is to convert the two-phase voltages, V_α and V_β, in the stationary reference frame into two-phase voltages V_{ds} & V_{qs}, in the synchronous reference frame using Equation (4.3). The grid angle, θ, is used in the calculation of Equation (4.3).

$$\begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} \quad (4.3)$$

Similar steps are carried out to convert the currents i_{abcs} to i_{qs} and i_{ds}.

Figure 4.2 shows the Matlab/Simulink model to calculate the voltages and currents in the d-q rotating frame.

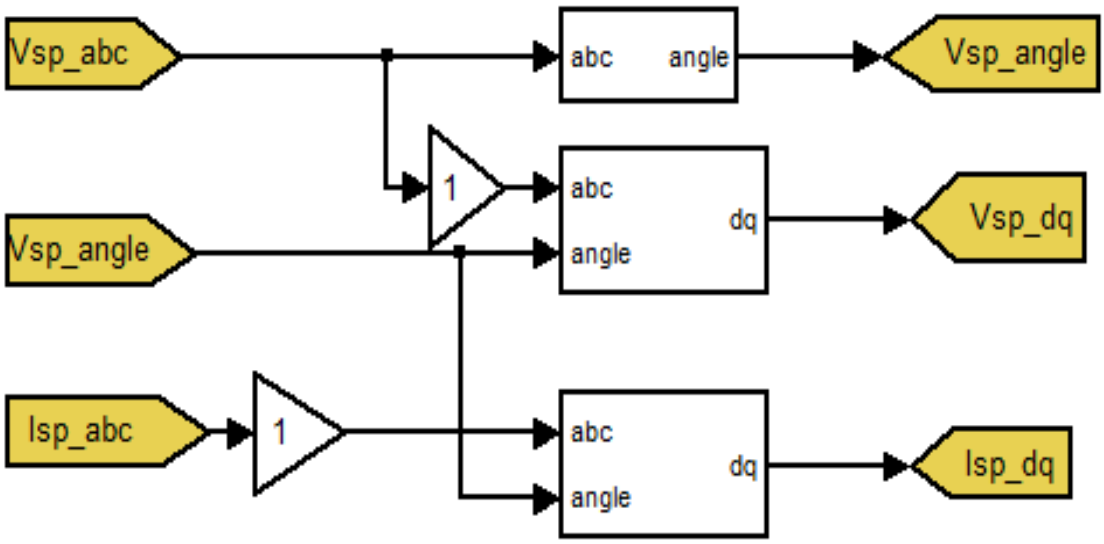


Figure 4.2 Matlab/Simulink model for calculating voltages, currents and voltage angle in the dq rotating frame

Equations (4.4) and (4.5) compute the real and reactive powers, as shown in Figure 4.3, from the voltages and currents v_{ds}, v_{qs}, $i_{ds,}$ and i_{qs}.

$$Ps_{-p} = v_{ds}i_{ds} + v_{qs}i_{qs} \quad (4.4)$$

$$Qs_{-p} = v_{ds}i_{qs} - v_{qs}i_{ds} \quad (4.5)$$

where, v_{ds}, v_{qs}, $i_{ds,}$ i_{qs} are the d-axis and q-axis voltages and current respectively.

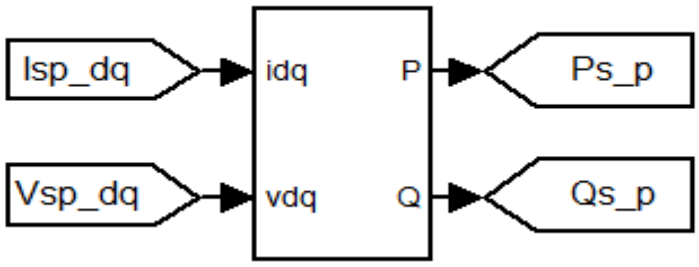


Figure 4.3 Calculation of actual real and reactive powers

The error between the demanded power and the actual power is calculated and given to the active and the reactive PI controllers, with the saturation blocks, as shown in Figure 4.4. The outputs of the two PI controller are the reference voltages v_{dr}^{*}, and v_{qr}^{*} respectively. These two reference voltages are converted to three-phase reference voltages, v_{abcr}, as discussed in the next section. This three-phase voltages act as the reference voltage for the Direct Space Vector Modulation (DSVM) technique, which is used to trigger the matrix converter connected to the rotor of the DFIG.

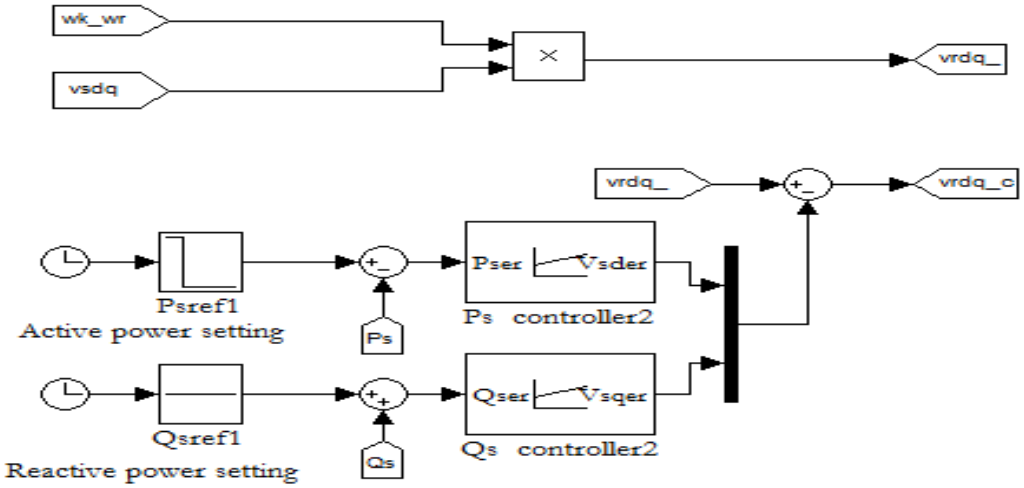


Figure 4.4 Active power and reactive power controllers for the RSC connected to the matrix converter fed DFIG based wind energy conversion system

For calculating the reference voltage, $V_{ref\_RC,}$ to the Direct Space Vector Modulation (DSVM) technique, the sequence given below is followed.

1) Calculating the present rotor voltages, V_{rp_dq}, by multiplying the stator voltages V_{sp_dq} by the slip, as shown in the Figure 4.4.
2) The reference rotor voltages, $V_{rp\_dq\_c}$, to be injected into the rotor in order to meet the demanded power is calculated by adding the rotor voltages with the correction voltages of P and Q controllers, as shown in the Figure 4.4.

The conversion of $V_{rp\_dq\_c}$ to three-phase reference voltage, V_{ref_RC}, involves two steps. The first step is to convert the voltages in the rotating reference frame, dq, to voltages in the stationary reference frame, αβ. The second step is to convert the voltages in the stationary reference frame, αβ, to the three-phase rotating frame, abc. Equation (4.6) describes the conversion of voltages in the dq frame to the αβ frame.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta_r & -\sin\theta_r \\ \sin\theta_r & \cos\theta_r \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{4.6}$$

The angle 'θ_r', in Equation (4.6), is obtained by integrating the slip speed.

Equation (4.7) describes the conversion of the voltages in the αβ frame to the three-phase rotating frame, abc.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -0.5 & -0.5 \\ \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{4.7}$$

Figure 4.5 shows the implementation of these transformations in Matlab / Simulink.

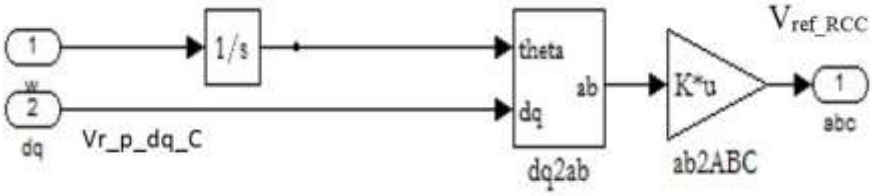


Figure 4.5 Matlab/Simulink model for converting dq to abc values

For different set point variations (super synchronous and sub-synchronous speeds) and load variations (reference power), Figures 4.6 and 4.7 show the speed variations and the generated V_{ref_RC} by the controller.

The set point was varied at 3 s from the super-synchronous speed to the sub-synchronous speed. The load was varied at 2.5 s and 4.5 s. The active power at the stator was 1000 W and 2000 W, respectively, with the demanded reactive power being zero.

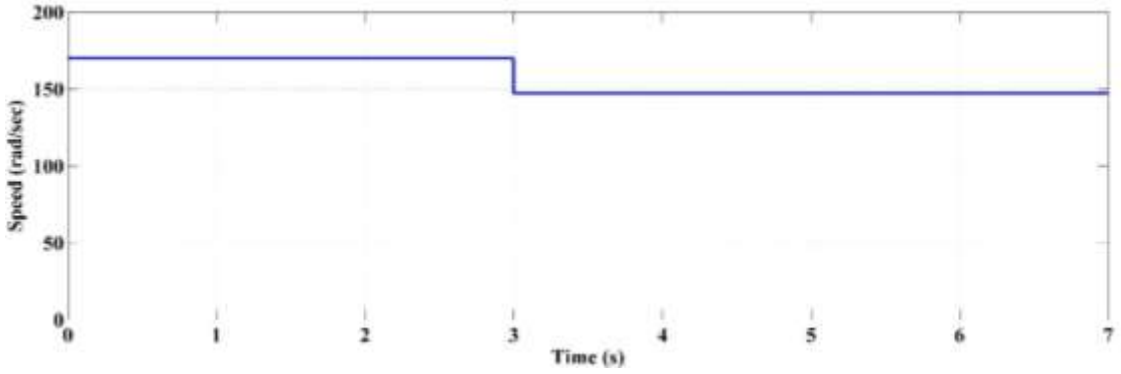


Figure 4.6 Speed versus time

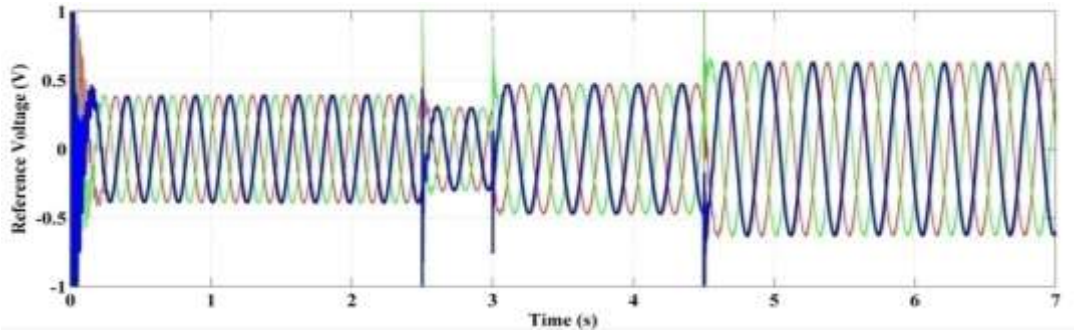


Figure 4.7 Three-phase reference voltages versus time

Figure 4.8 shows the corresponding rotor voltage generated by the matrix converter, while Figures 4.9(a) and 4.9(b) show the matrix converter output current (rotor current) and the matrix converter input current, respectively.

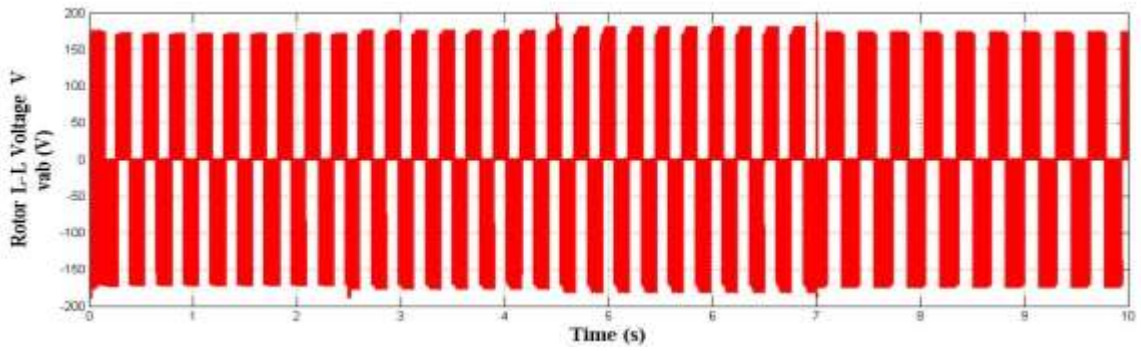


Figure 4.8 Rotor line-to-line voltage, V_{ab}, versus time

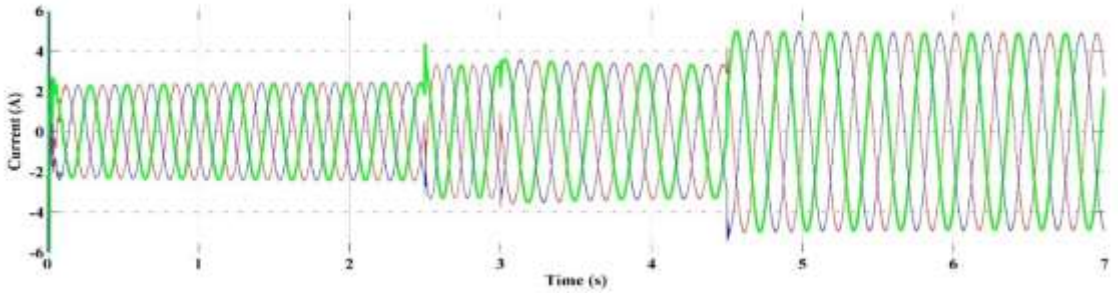


Figure 4.9 (a) Rotor currents I_{rabc} (matrix converter output currents) versus time

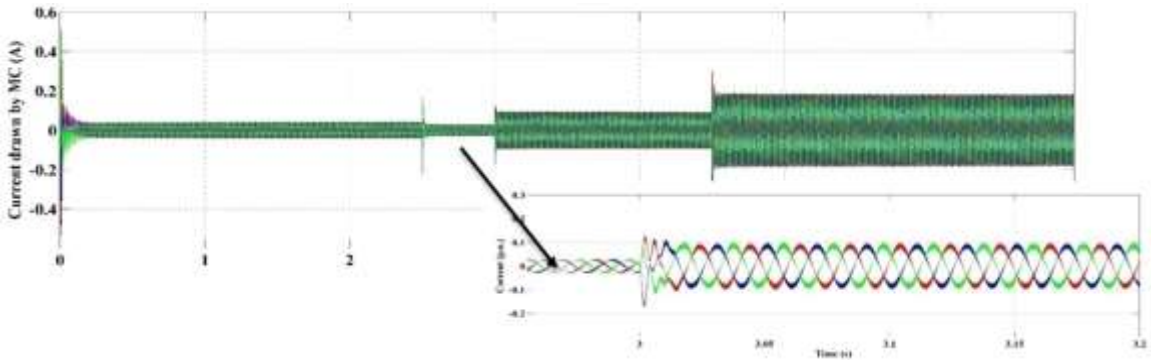


Figure 4.9 (b) Matrix converter input current versus time

Figure 4.10 shows the stator current during the power control operation and Figures 4.11 and 4.12 show the controlled stator power and the corresponding rotor power.

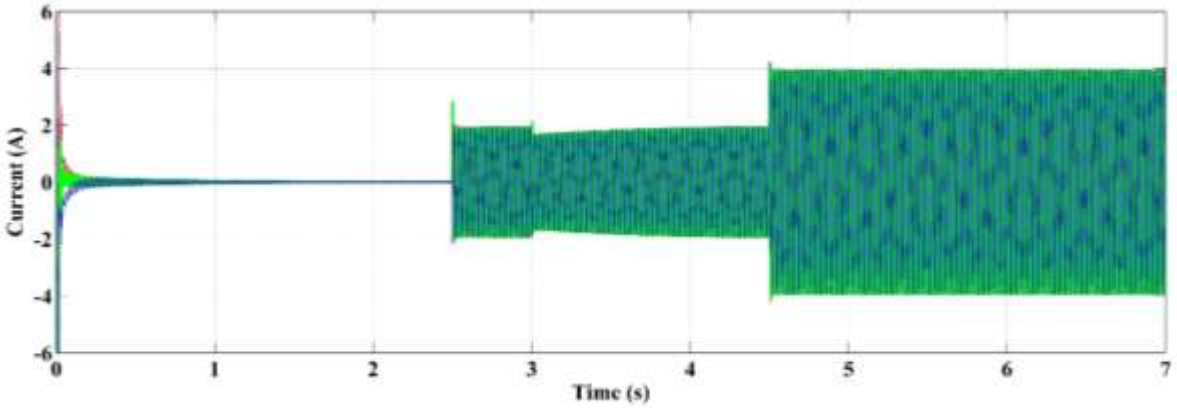


Figure 4.10 Stator currents I_{sabc} versus time

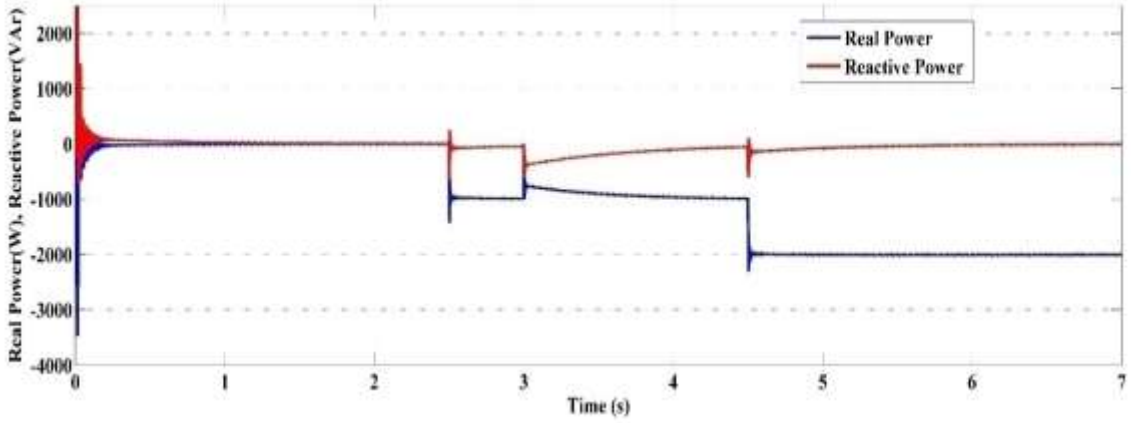


Figure 4.11 Real and reactive powers in stator versus time

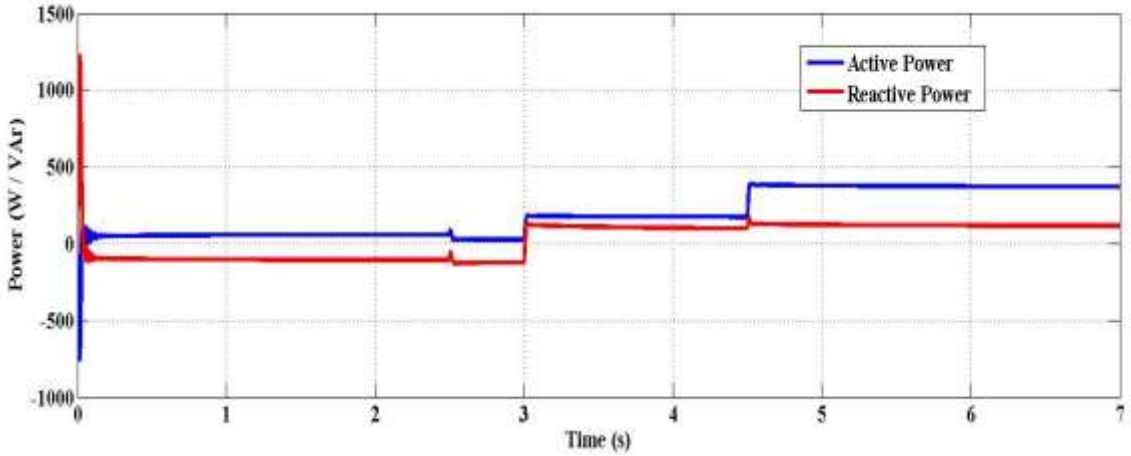


Figure 4.12 Real and reactive powers of the rotor versus time

Figure 4.13 presents the Matlab layout of the final integrated structure of the matrix converter, the DFIG DSVM algorithm, the four-step commutation algorithm, the rotor side controller and other transformation routines.

Figure 4.13 The complete Matlab simulation setup with the matrix converter, the DFIG, the DSVM, the four-step commutation, transformation routines and the rotor side controller

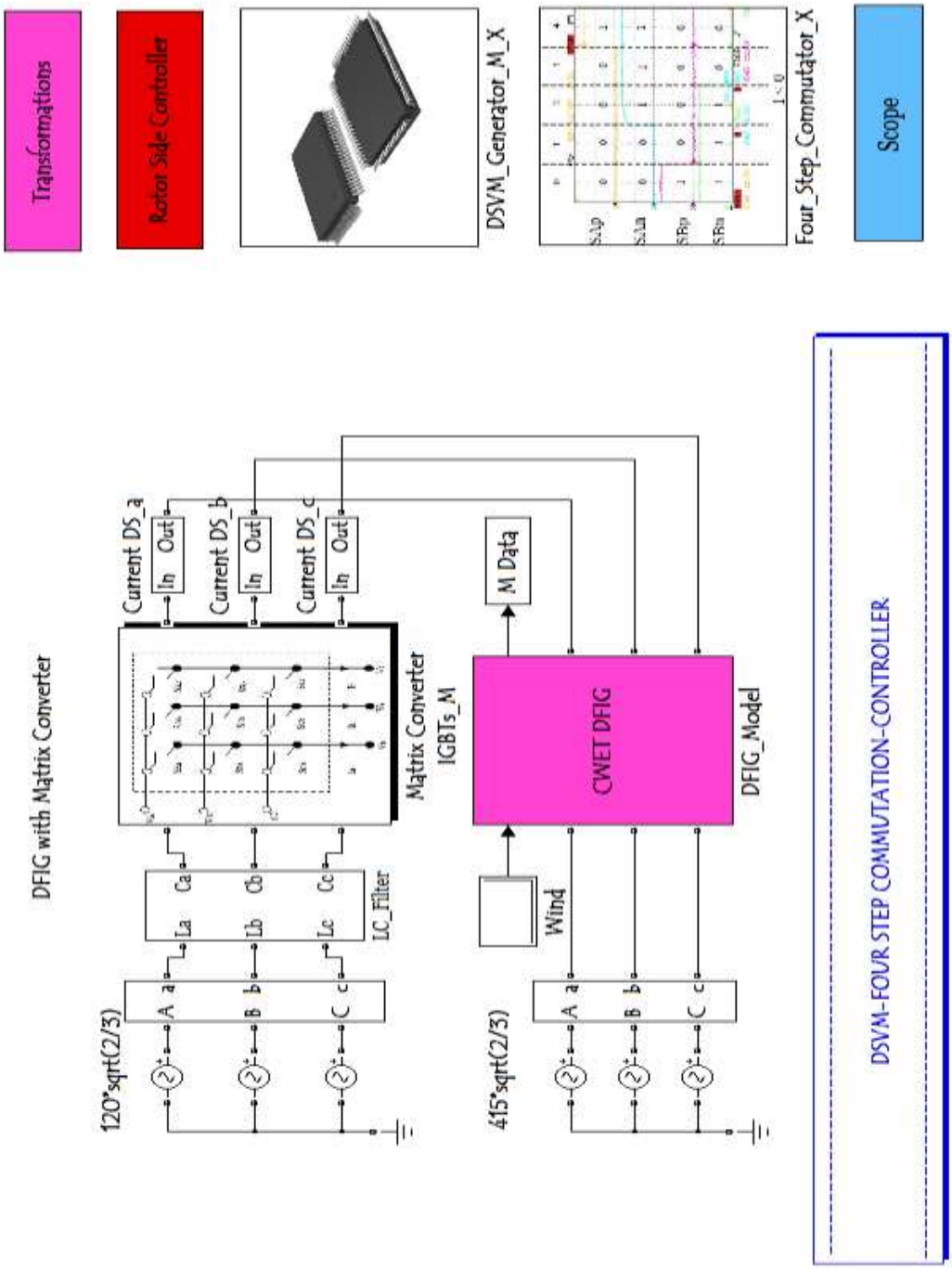


Figure 4.13 Complete Matlab Simulation Setup with Matrix converter , DFIG, DSVM , Fourstep, Transformation routines and Rotor side controller

CHAPTER 5

MODEL BASED VHDL CODING OF DIRECT SPACE MODULATION TECHNIQUE

5.1 INTRODUCTION TO MATLAB/XILINX INTERFACE

The Direct Space Vector Modulation (DSVM) algorithm is very bulky in terms of the resources required by the code to be accommodated in the SPARTAN 3E Nexys2 controller board. This is one of the biggest disadvantages of this technique, which has motivated researchers to develop more simple modulation algorithms for the Matrix Converter (MC). Many researchers do not take the effort to make the DSVM work by optimizing the code for superior performance. We have tried in our own way to shrink the code, without altering it, using the concept of 'Time Division Multiplexing (TDM)'. The VHDL code generated by Sysgen was used to generate the .bit file that is programmed in the FPGA. Figure 5.1 shows the resource estimate for implementing DSVM using a Spartan 3E controller.

In general, the main component that leads to insufficient resources is the use of too many "Multipliers". The Spartan 3E FPGA controller has only twenty on-chip 18×18 multipliers. If one observes closely, the DSVM block alone requires 10 multipliers (refer the documentation on the DSVM in Simulink). In addition to this, quite a good number of Read Only Memory (ROM) units are required. The use of ROMs has to be kept to a minimum and use of multipliers in order to save the memory space. If one wants to achieve perfect optimization of the code, the number of bits assigned to the output of each block has to be defined by the user by meticulously analyzing the width of the data lines. All the above have been rigorously carried out and tested to match the output obtained with the DSVM Simulink model to verify its accuracy.

mc_zcd_dsvm_x_4step_x_final_of_all_cw Project Status (04/09/2014 - 14:57:37)			
Project File:	mc_zcd_dsvm_x_4step_x_final_of_all_cw.xise	**Parser Errors:**	No Errors
Module Name:	mc_zcd_dsvm_x_4step_x_final_of_all_cw	**Implementation State:**	Programming File Generated
Target Device:	xc3s500e-4fg320	**• Errors:**	
Product Version:	ISE 14.1	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	938	9,312	10%	
Number of 4 input LUTs	2,857	9,312	30%	
Number of occupied Slices	2,104	4,656	45%	
Number of Slices containing only related logic	2,104	2,104	100%	
Number of Slices containing unrelated logic	0	2,104	0%	
Total Number of 4 input LUTs	3,282	9,312	35%	
Number used as logic	2,833			
Number used as a route-thru	425			
Number used as Shift registers	24			
Number of bonded IOBs	204	232	87%	
Number of BUFGMUXs	1	24	4%	
Number of MULT18X18SIOs	4	20	20%	
Average Fanout of Non-Clock Nets	2.47			

Figure 1.1 Resource estimate for the DSVM code in the ISE design suite

5.2 OUTLINE OF THE TDM AND BIT OPTIMIZATION

In this section, sample time issues, when the TDM is used, is treated elaborately. The reduction in the use of multipliers will also be demonstrated. Bit optimization could be shown for one element of the Xilinx Blockset, which will give an idea of applying it to other blocks. It is recommended that one should go through the Simulink model first, provided in "DSVM for MC in Matlab" before reading this document further. Only after the major issues are treated, we will be going into each block in Xilinx, and compare the results with the respective Simulink model block for a better understanding.

5.2.1 Time Division Multiplexing – A Solution to the Compact VHDL Code

The Xilinx TDM block behaves like a parallel processing unit. When we have one set of mathematical equations, which apply for different variables, we could reduce the resources used by parallel processing all such variables with just one set of equations.

One possibility of such a situation in our context is the transformation of the voltage and the current references to the αβ and dq reference frames. The equations for the transformations are the same in both the cases. Hence, if we could use just one chunk of code for obtaining the magnitude and angle information of both the voltage and current, it would reduce the resources used by the two blocks by exactly 50%. If we can identify more such situations and apply the TDM concept, we can save on the number of logic gates used. Fixing the sampling rate of the data lines on the TDM is important, and depends on the number of inputs to the block. The Simulink clock period corresponds to the minimum sample rate at which the data are processed. In our case, it is 20 ns. If our block has two inputs to be multiplexed, then each input should appear at the input ports at the rate of 40 ns. If there were three, the data rate required would be to be 60 ns.

Now, if three input data arrive at 60 ns each, the block processes the data on the first input port during the first 20 ns (minimum sample period), the data at the second input port during the next 20 ns cycle and the last input port data during the last 20 ns period. Thus, to process "n" number of data lines in parallel, the rate of each data line should be set to "n×Simulink period". If we do so, the output obtained at a sampling rate is equal to the Simulink period. The Time Division Demultiplexer (TDD) block is used in conjunction with the TDM block to give all the outputs of the TDM at the same instant of time, in our case, at the sampling rate of 60 ns. Hence, it appears as if the three data at the input ports of the TDM block were processed in parallel, reducing the resources used, but actually at the cost of sampling rate.

So far, we have spoken of a local situation, of a single TDM block. In our design, we may have a number of TDM blocks, each with any number of inputs. As we back-propagate from the final output (pulses to MC) back to the input (voltage and current references), one will find that the sample rates are to be defined for each data line by taking into account the number of TDM blocks present, and the number of inputs to each TDM block. One has to carefully calculate and set the sample rate of each data line by back-propagation.

From an overall system perspective, if the voltage reference itself is obtained from a controller block elsewhere in the system (which is usually the case), then, the sampling rates of the input data to the controller are also affected by the presence of the TDMs elsewhere. Looking at Figure

5.2, we can have a clear understanding of fixing the sampling rate of the inputs of this block, which has a significant number of TDMs.

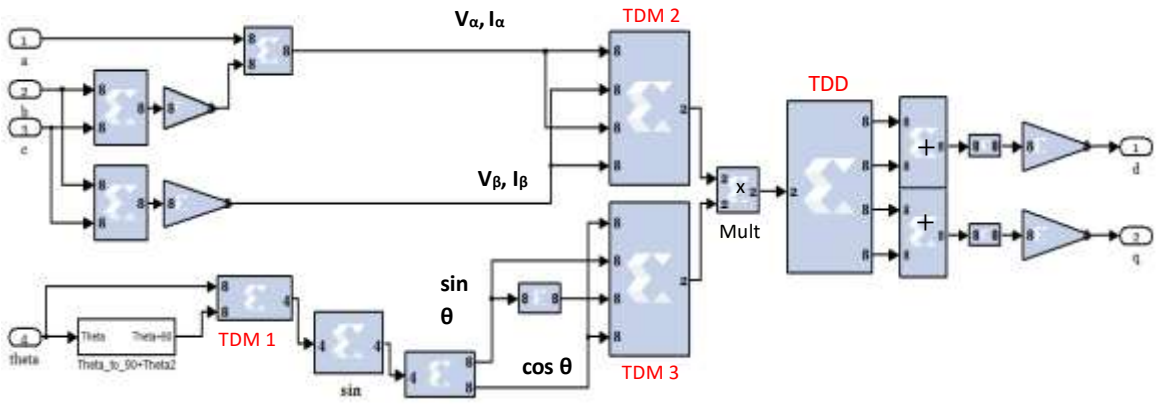


Figure 5.2 abc-dq transformation of the voltage and the current

At the outset, one has to know the sample rate before getting into TDM. The sampling period of Simulink is fixed at 20 ns in the System Generator block, which corresponds to a sampling rate of 1 to the System Generator. The numbers shown near the input terminals of each block in Figure 5.2 are sampling rates of the inputs or outputs of that block. The sample rates can be displayed as shown by using the path - System Generator → General tab → Normalized Sample Periods (in the drop-box), as shown in Figure 5.3.

Figure 5.3 Displaying the sampling rates

A sampling rate of 2 indicates that the data is sampled every 2×20 ns = 40 ns. Similarly, a sampling rate of 4 indicates that data is being sampled every 4×20 ns = 80 ns. The data can be input/ output to/ from a block.

In Figure 5.2, there are three TDMs in this module. TDM 2 and TDM 3 have four inputs, while TDM 1 has two inputs. If the TDM has four inputs, and the minimum sample rate is fixed at 40 ns from a purely precautious motive, the block would require 40×4 = 160 ns to process all the four data lines for which each of the input data lines has to appear at the input terminals at a rate of 40×4 = 160 ns respectively.

TDM 1 is employed to obtain the sinusoidal and co-sinusoidal values of the angle of the reference space vector with respect to the α-axis. By doing so, we eliminate the use of one memory block. TDM 2 and TDM3 work in parallel to convert the values in the αβ reference frame to the values in the dq reference frame. Equations (5.1) and (5.2) involve the multiplication of four factors to obtain V_{dq} and I_{dq}.

$$V_d = V_\alpha \times \cos\theta + V_\beta \times \sin\theta \quad (5.1)$$

$$V_q = -V_\alpha \times \sin\theta + V_\beta \times \cos\theta \quad (5.2)$$

In order to reduce the number of multipliers used for the transformation from one frame to another, TDM 2 and TDM 3 are employed. Hence, it is possible to implement Equations (5.1) and (5.2) using only one multiplier to do compute both the V_{dq} and the I_{dq}. During the first 40 ns period, the input on d1 lines of the TDM 2 and TDM 3, V_α and cosθ are sampled and appear at the input of the multiplier. In the next 40 ns, the input at d2 lines of the TDM 2 and TDM 3, V_β and sin θ, are processed simultaneously and appear at the multiplier's terminals. The next two inputs are processed in the same fashion. Hence, the two TDMs require 160 ns to complete the sampling of their respective four input data. This corresponds to a sampling period of 160 ns, which indicates a sample rate of 8, seen at the input data lines of TDM 2 and TDM 3 in Figure 5.2.

The four results of the multiplier are then demultiplexed using the TDD block. Note that the sample rate of each output line is also 8, corresponding to 160 ns. Further, after the addition, the d and q components are obtained from the adder blocks.

Due to the two four input TDM blocks, the output rate of the TDM 1 is also required to be 160 ns, which forces it to work at a rate of 80 ns (since there are two inputs to the TDM 1), corresponding to a sample rate of 4. In order that the TDM 1 works at a rate of 80 ns, the inputs

of the two terminal TDM should arrive at a rate of 2×80 ns = 160 ns. Similarly, one can back-propagate and observe that all the inputs to this block should arrive at the sampling rate of 8 (160 ns), so that TDM 2 and TDM 3 can work at a sampling period of 40 ns.

We should now understand the implications of the sampling rate being fixed to this block, which is somewhere at the beginning of the controller code, preceding the DSVM code. We can see that the output d and q lines are at a rate of 160 ns, which means that the subsequent blocks have to have their inputs sampled at 160 ns, else the system shows an error saying that there is a mismatch of sample rates, and cannot be processed.

Because of the one four-terminal TDM, the sampling rate of the whole system has been altered. In addition, the fast sampling rate of 20 ns offered by Nexys2 cannot be properly utilized, but alternatively, there is an effective use of the resources available on the device to implement the whole DPC-SVM controller and the DSVM algorithm. The merits clearly override the compromise in the sampling frequency.

Now, we shall see what happens if we have a sampling period of less than 160 ns for V_{abc} and I_{abc}. Let us take it to be 80 ns. Figure 5.4 shows the now altered sampling rates and the error that shows up.

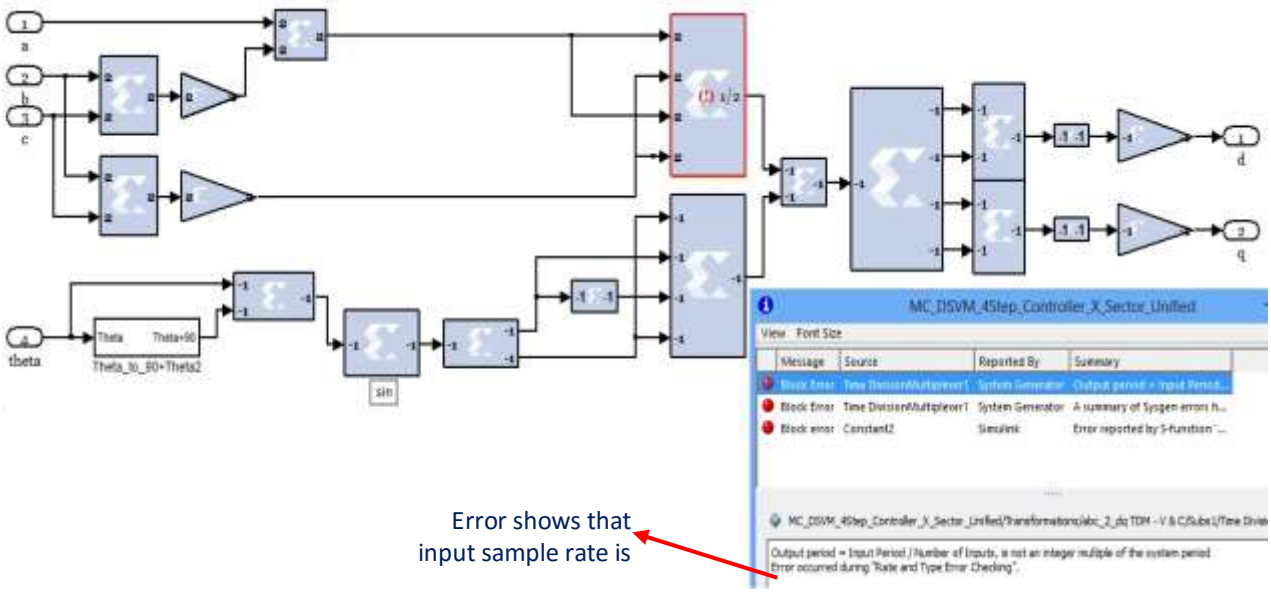


Figure 5.4 Sampling rate error

It can also be observed that the sample rates are ½ and -1, which are not realizable. A sample rate of ½ indicates that the block requires the inputs to arrive at a sample period of 10 ns, which is not possible. A sample rate of -1 indicates that there is a violation by attempting to operate at a rate lesser than the FPGA's clock period. This should give the user a good idea of why the sample period is important when using TDMs.

IMPORTANT NOTE: The voltage and current multiplexer are outside the block shown in Figure 5.2. From Fig 5.5, one can see the actual number of TDMs used only for the transformation of the current and voltage from the abc reference frame to the dq reference frame. As the current and voltage TDMs are two-input TDMs, the final sample rate of the inputs will be 16, which is equivalent to 320 ns.

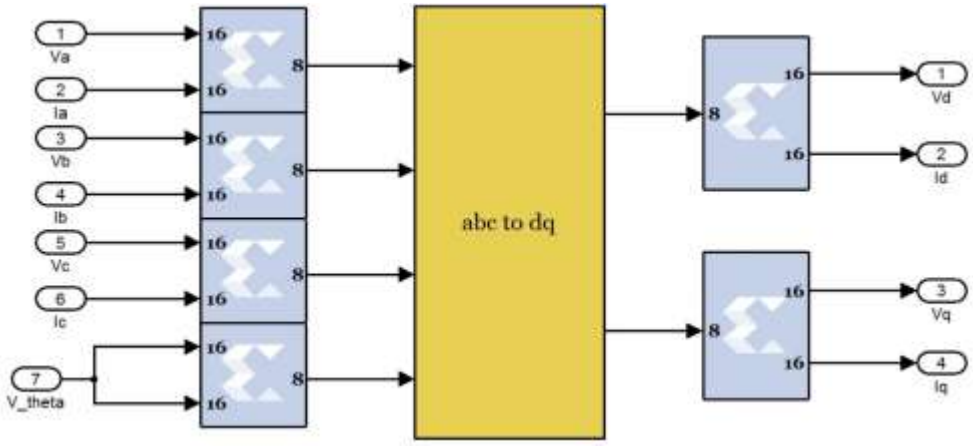


Figure 5.5 abc to dq transformation

In addition, the input sample rates for the DSVM block as well as the whole system (including the controller and modulation algorithm) are to be fixed at 16. One has to remember that the dq components are the control variables for the DPC-SVM controller, which generates the reference voltages for the DSVM module. Hence, one has to keep in mind that the input sample rates for the DSVM reference voltages and currents are fixed at 16, implying that their input sample period should be fixed as 320 ns.

Please note that this block has been included in this chapter for understanding the concept of the TDM, which is essential in order that the modulation algorithm can be implemented on an FPGA controller. However, the DSVM module alone will be discussed hereafter. For more details on

the DPC-SVM controller, which includes the transformation block kindly refer the respective technical document.

5.2.2 Reducing the Number of Multipliers

The number of multipliers can be reduced to a large extent by using TDM wherever possible. Where the TDM cannot be used, one can make use of a simple multiplexer. Figure 5.6 demonstrates how the four multipliers are eliminated in the "Vector Selector" module to generate the switching pulses.

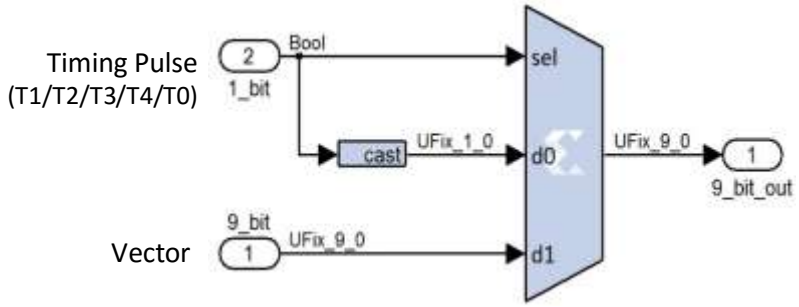


Figure 5.6 Replacing multipliers with multiplexers

The logic behind the vector selector for a particular switching period, say T1, is that when T1 is available or high, the corresponding vector V1 should be applied. This was done earlier by multiplying T1 with the vector selected, thus implying that when T1 is high, the appropriate vector is applied, and when T1 is low, the vector is not applied.

Figure 5.6 does exactly the same thing. The "select" line of the multiplexer (MUX) is the timing signal T1 itself. When T1 is low, the output of the block should be zero. So T1 itself is given to the "d0" line of the MUX. When T1 is high, the 9-bit vector should be passed. Hence, the 9-bit vector from the selection block is given to the "d1" terminal of the MUX. Thus, we have eliminated five multipliers in the system for applying five vectors by using five simple MUXs. If one works on the same lines with multiplication blocks, one can see that most of them can be replaced using simple logic in combination with multiplexers.

5.2.3 Bit Optimization

The best way to demonstrate the need for bit optimization is when the data line is required to be multiplied by a floating-point number. For example, let us consider the conversion of the angle of a space vector from radians to degrees, as shown in Figure 5.7. We would multiply the angle in radians by a factor of $\frac{360}{2\pi}$=57.29, which requires 15 bits with a binary point of 9 bits.

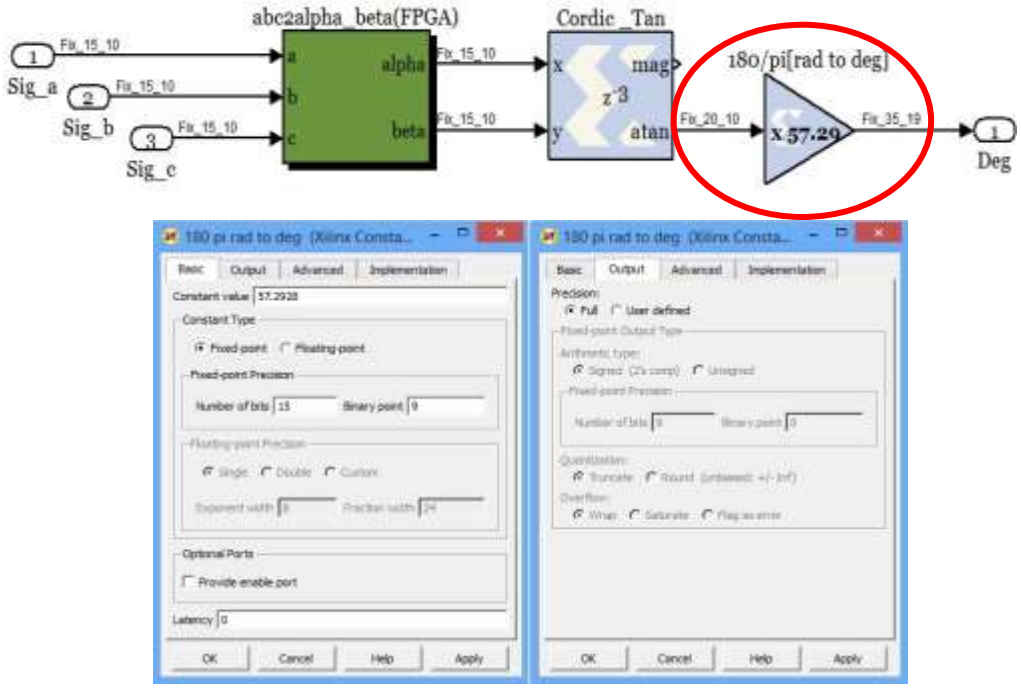


Figure 5.7 Bit requirement when the output of the block is FULLl

If we give the output of this block as “FULL”, then the resulting output number requires 35 bits with a binary point of 19 bits. If this huge number propagates into the subsequent blocks, the number of bits required by those blocks too would increase, resulting in an insufficient resource error in terms of slices available on the Nexys2 board. Hence, the programmer should analyze the bit requirement of the output data, and specify it explicitly in the “Output” of each block.

Figure 5.8 shows how the bit requirement is reduced when the number of bits of the output of the gain block was defined. It is evident that the maximum angle we would need is 360˚, which can be accommodated in 9 bits itself! Once we have specified the output to be only 9 bits, we get a

reduction of 26 bits! Hence, the number of slices that would be required is reduced in addition to the resources required by subsequent blocks.

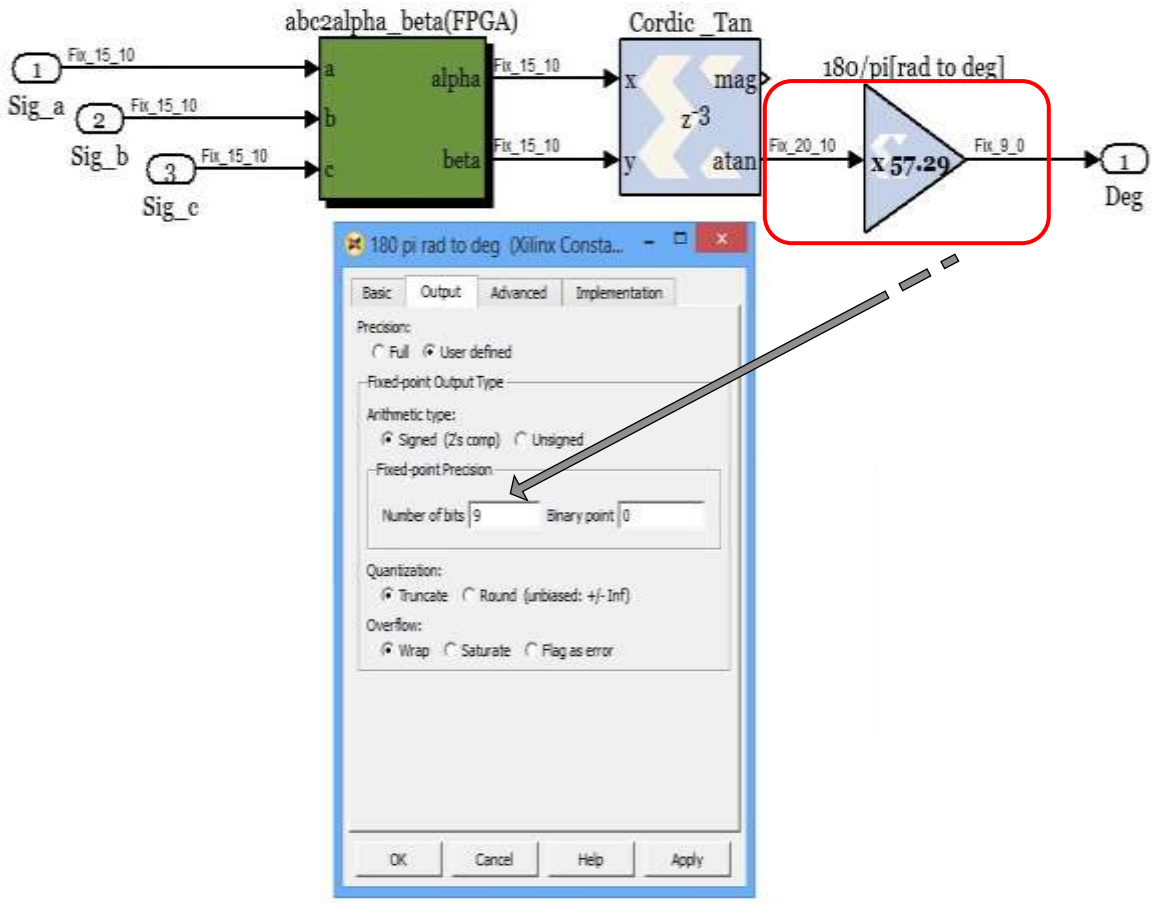


Figure 5.8-bit optimization

NOTE:

As a clear outline of using the TDM to reduce the number of multipliers and optimize the number of bits used has been provided in detail, these topics will not be dealt with further in this document. In addition, it will be directly indicated that the inputs to the DSVM block are sampled every 320 ns as explained earlier, and go ahead with the rest of the blocks in detail.

5.3 DSVM IN XILINX FOR AN MC WITH R-L LOAD

The inputs to the DSVM algorithm are the three-phase voltage and current reference waveforms. The voltage waveform reference is set by the user at a peak magnitude of unity, and a frequency of 25 Hz. The current reference waveform is the phase voltage at the supply terminals.

The following sections are written under the presumption that one has gone through "DSVM for MC in Matlab". We know that the abc to αβ frame transformation equations are the same for both the voltage and current space vectors, and these two can be time-multiplexed to effectively utilize the resources. The magnitudes of the αβ components are used to compute the angles of the space vectors. This can also be time-multiplexed.

5.3.1 TDM for Sector Identification

From the angle of the space-vectors, the locations of the two are to be estimated in the αβ frame in terms of sectors. We know that the voltage space vector hexagon and the current space vector hexagon are shifted by exactly 30˚. As a result, it might not be possible to time-multiplex the sector identification block too. Nevertheless, this can be possible if we can make the current space vector the same as that of the voltage space vector hexagon.

Rotating the current space vector hexagon by 30˚: Figure 5.9 (a) shows the voltage space vector hexagon of the MC. Figure 5.9 (b) shows the conventional current space vector hexagon with the input phase voltage reference. It is well known that the current space vector hexagon lags the voltage space vector hexagon by 30˚, and can be seen from Figure 5.9.

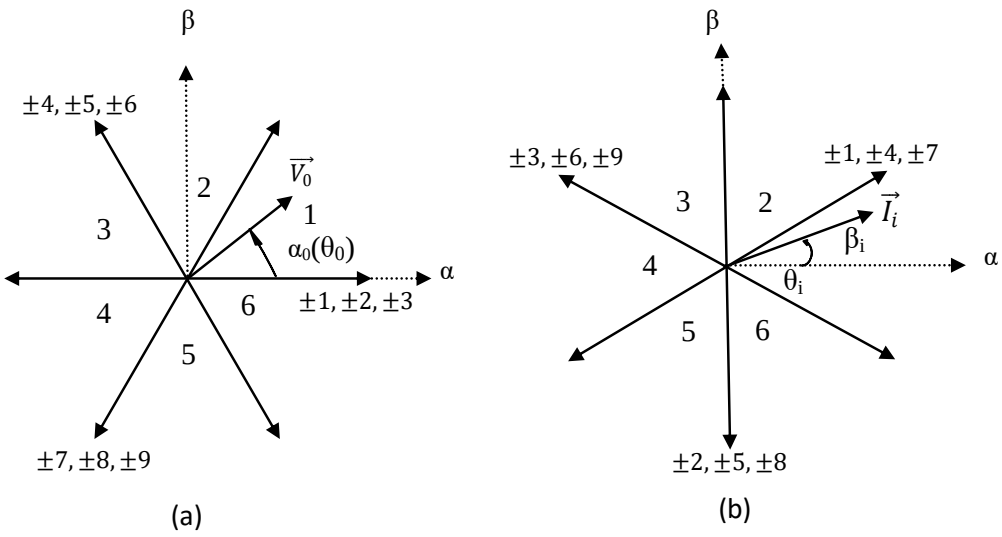


Figure 5.9 (a) Voltage space vector (b) Current space vector

Let us consider the possibility of using the sectors of the Voltage Space Vector (VSV) itself to compute the sectors of the CSV, so that we can also time-multiplex this module. If we can have a reference signal for the CSV that can introduce a +30º phase-shift, the VSV sectors itself can be used. We know that the line voltages lead the corresponding phase voltages by 30˚. We shall now explore the possibility of taking the line voltages as the current reference waveforms, and compute the sectors using those of the VSV. Figure 5.10 shows the test module where we first validate this idea by obtaining the same results when calculating the current sector using both the ways – 1) Phase voltage as the reference with the current sectors and 2) Line voltage as the reference with the voltage sectors.

The computation of the current space vector angle and sectors using the phase voltage as the reference is the conventional method, as shown first in Figure 5.10. The new method proposed to calculate the CSV angle and sector using the VSV hexagon itself is shown below the conventional method. The line voltage itself is taken as the reference current waveform as shown. Note that the 30º shift that we include while calculating the internal theta of the CSV in the conventional method is not required in this module, and is removed from the Deg_360 block. This makes the internal theta computation block to be also time-multiplexed.

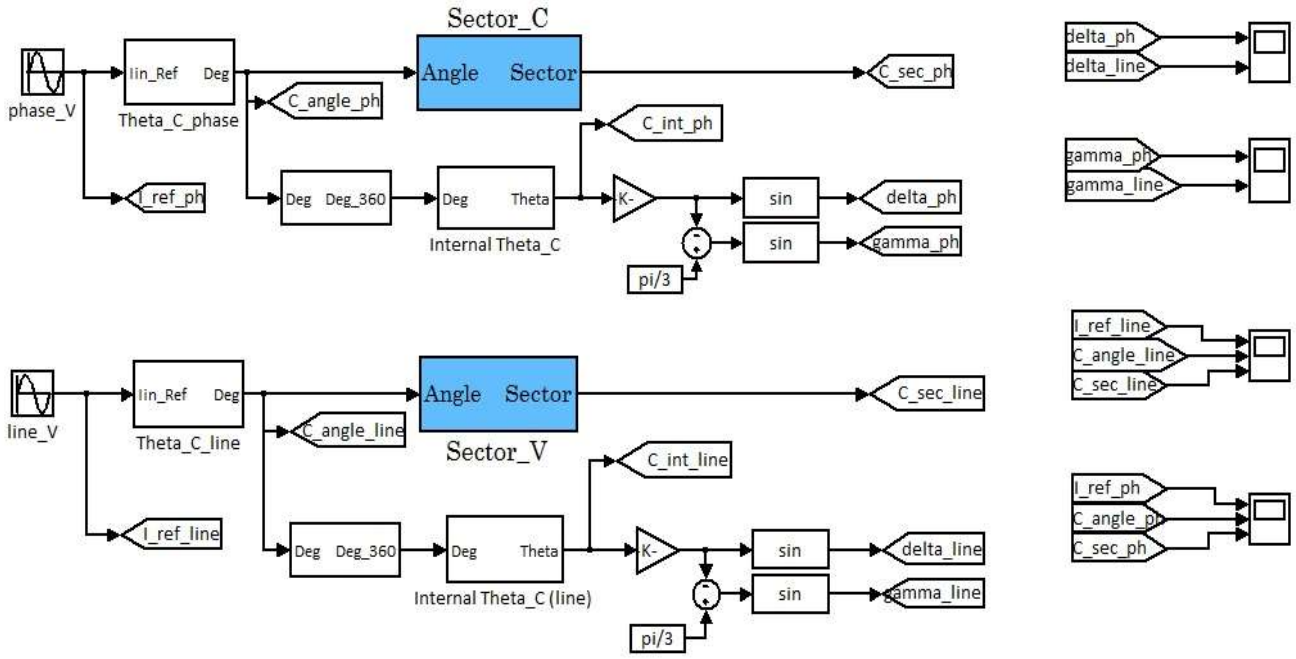


Figure 5.10 Sector computation of the CSV using the VSV

No method is validated unless substantial proof is available. From Figure 5.10, it can be concluded that the parameters that need to be matched in both the methods are the sectors obtained, and the duty cycles. Once these parameters obtained from the proposed method is the same as those obtained from the conventional method, we can prove the idea to be correct. Figures 5.11(a) and 5.11(b) show the sectors obtained from the conventional method and the proposed method respectively.

The sectors obtained are the same in both methods as can be seen. Figures 5.12 (a) and (b) show the duty cycles d_δ and d_γ respectively, using the conventional and the proposed methods.

The duty cycles computed using the proposed method matches with those obtained from the conventional method. The current sector and duty cycles are the main parameters that are carried further in the vector application and the timing pulse generation. As there is no mismatch of these two important parameters, we can safely say that the proposed method for computing current sector using the voltage sector is validated.

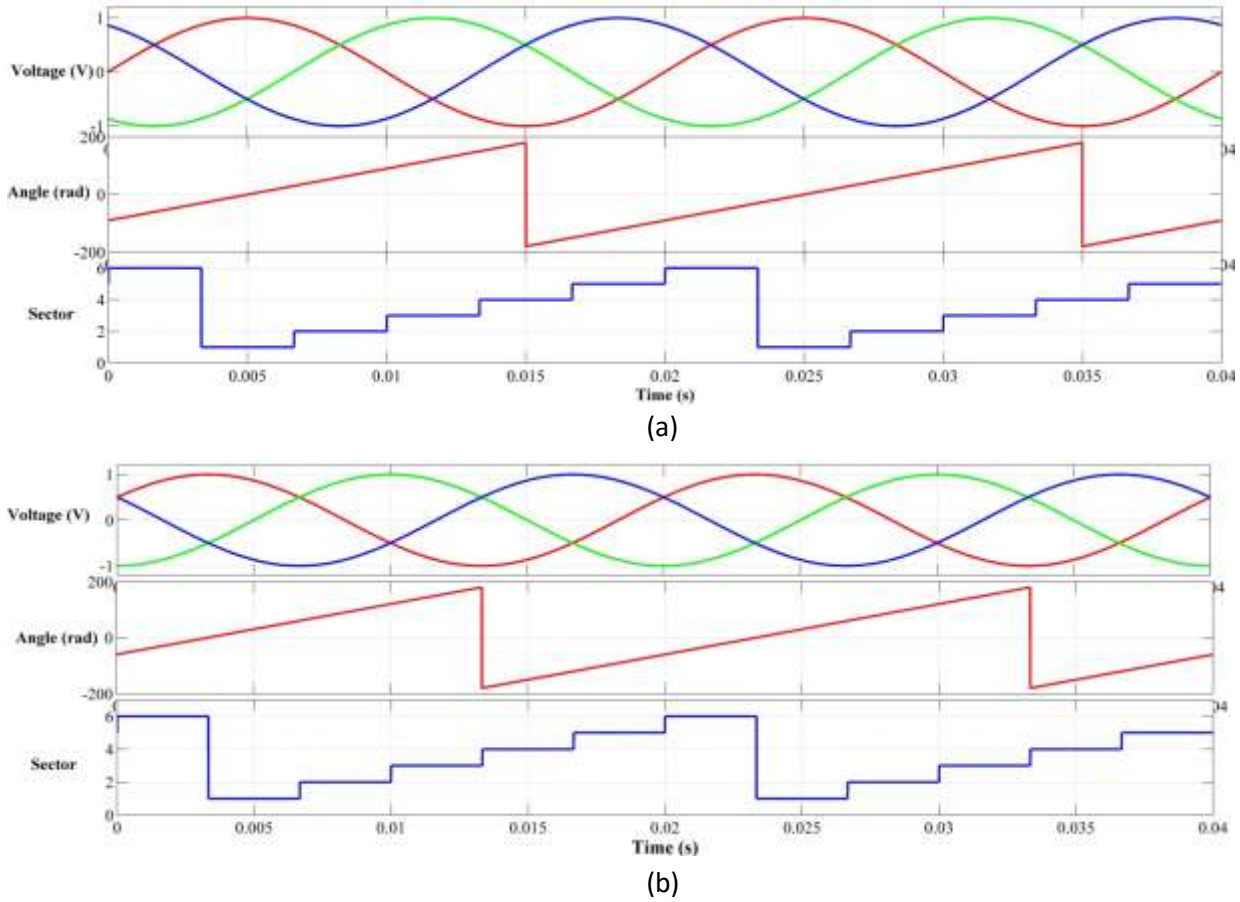
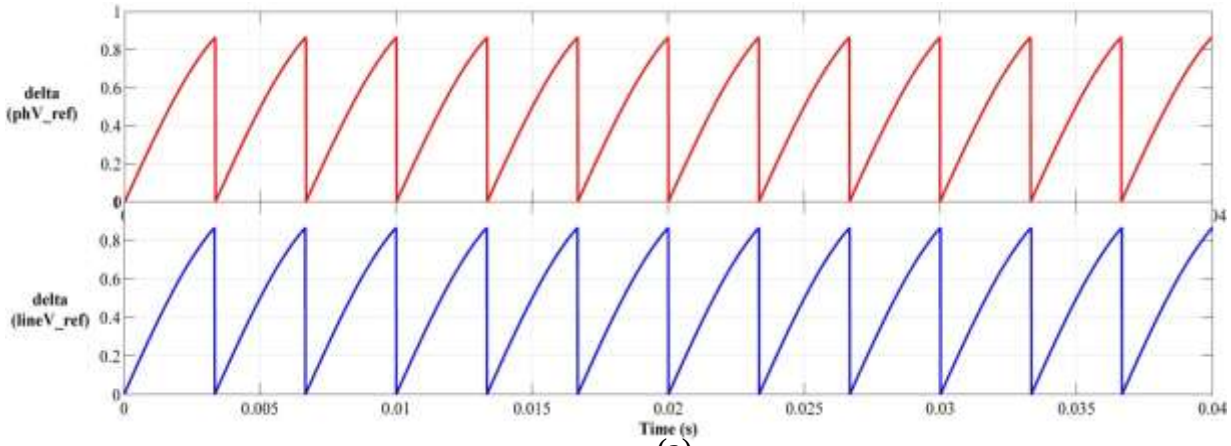


Figure 5.11 CSV sector computation using (a) conventional method (b) proposed method

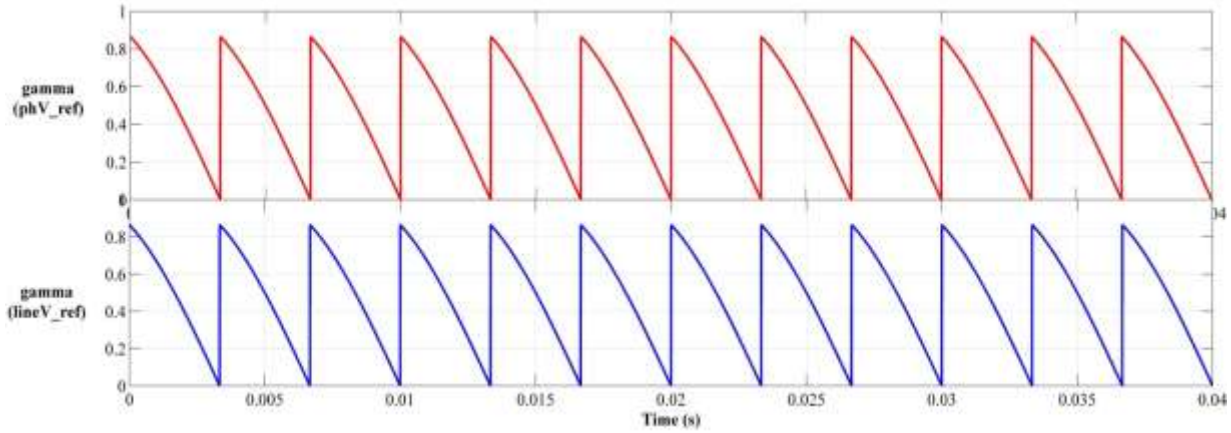
The next step would be to check for the unity power factor using the proposed method. Figure 5.13 shows the phase relationship between the input current and the phase voltage obtained using the proposed method.

In addition, it is evident that the proposed method does not affect the unity power factor operation that was achieved using the conventional method.

However, since the proposed method shown in Figure 5.10 makes possible the time-multiplexing of the current space vector module with the voltage space vector module in Xilinx, we go ahead with the proposed method. The line voltages are taken as the current reference and the sectors are computed using the voltage sector identification block.



(a)



(b)

Figure 5.12 Computation of (a) d_δ (b) d_γ using the conventional and proposed CSV methods

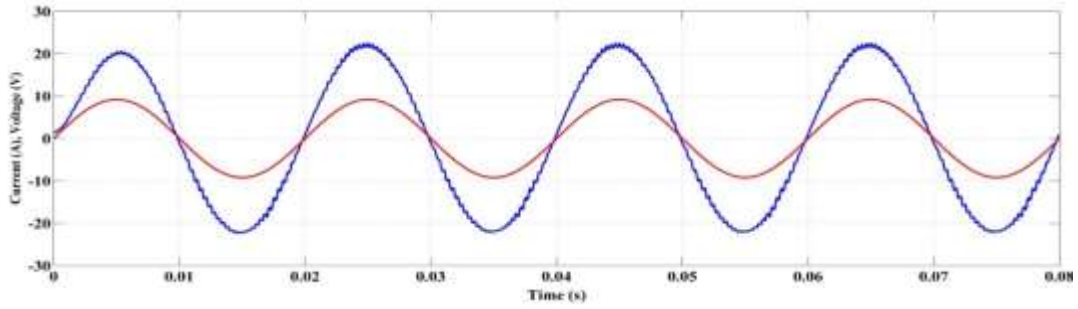


Figure 5.13 Phase relationship between input current and phase voltage

5.4 XILINX MODEL OF DSVM

The DSVM model that was simulated using the Xilinx Blockset is shown in Figure 5.14.

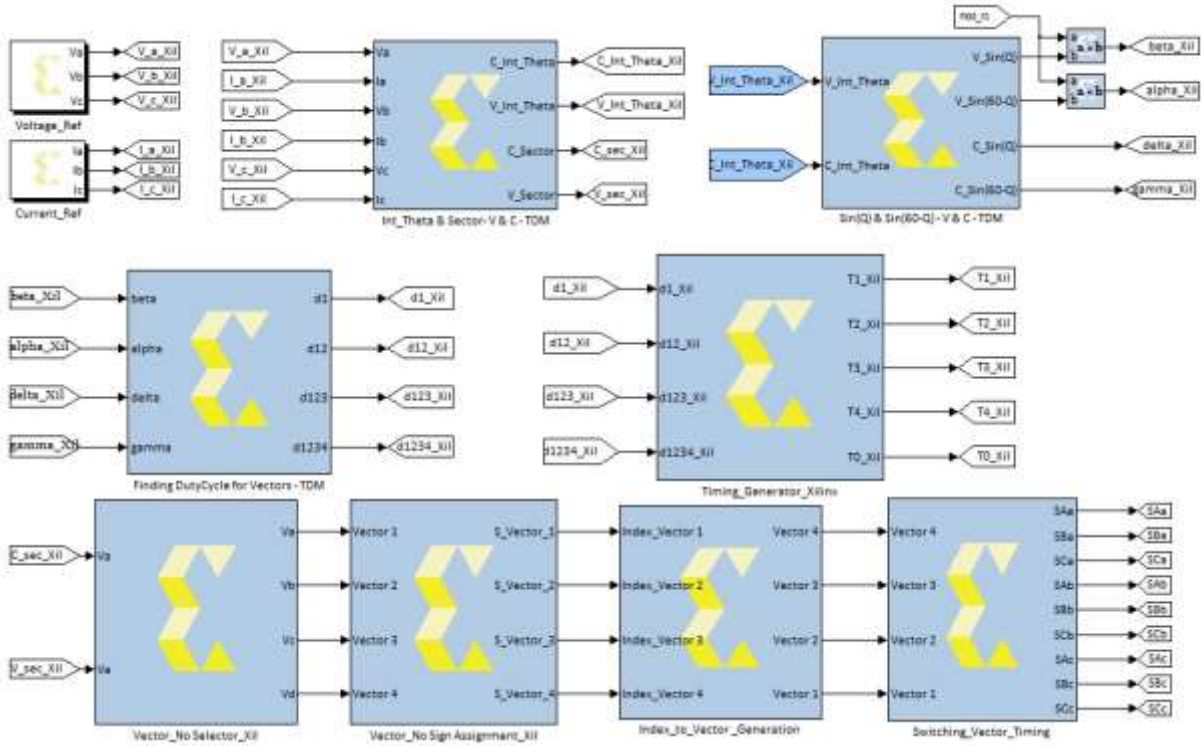


Figure 5.14 DSVM using the Xilinx Blockset

Figure 5.14 is explained through the following steps

5.4.1 Computation of internal angle and sectors: The voltage and current references are time multiplexed in the "Int_theta & Sector V&C TDM" block of Figure 5.14, as shown in Figure 5.15.

5.4.2 Finding Angle of SSVs: The Clark's transform equations are implemented directly to compute the αβ components in the abc2alpha_beta (FPGA) block, shown in Figure 5.16.

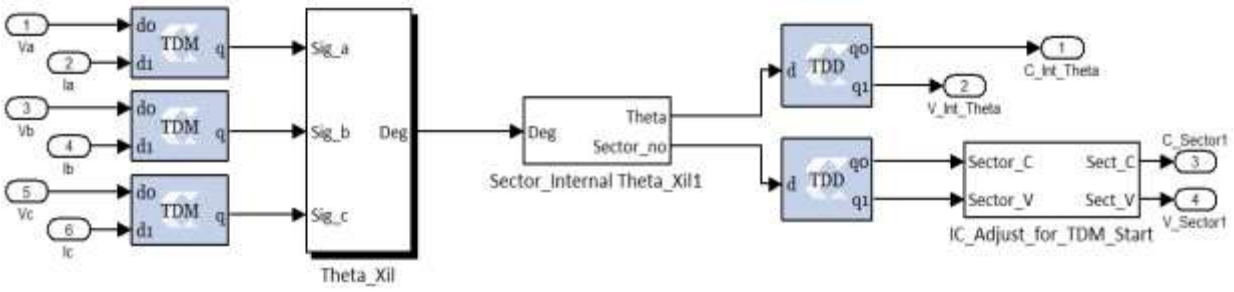


Figure 5.15 Time-multiplexing of voltage and current reference vectors for computation of sectors

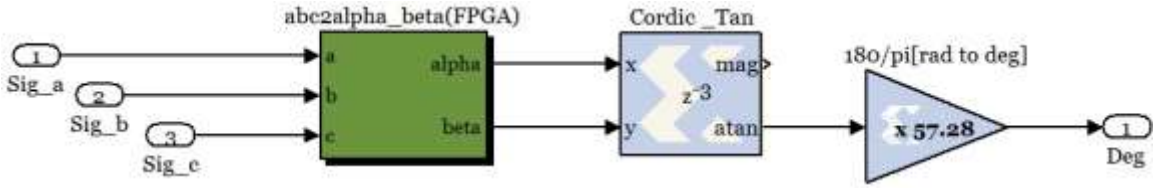


Figure 5.16 Computation of angle of space vectors

There is no simple block that can compute the angle like we do in Simulink. The Xilinx blockset provides a complex block that does the $\tan^{-1}$ function with a certain amount of delay. The "Cordic ATan" block from the Xilinx Reference Blockset → Math directory in Simulink Library Browser is used to find the angle of the space vectors in radians.

The settings of the Cordic Atan block are quite interesting, and different from normal Xilinx blockset components. Figure 5.17 shows the Cordic Atan block settings.

The number of processing elements that the Cordic aTan block requires to perform inverse tangent calculation has to be specified by the user. The more the number of units used, the more the accuracy. The trade-off is the delay introduced in the process when a large number of units are employed along with an increase in resources.

The data width also plays an important role in defining the accuracy of the angle obtained from the block. We have given the data width as 20 bits with 10 floating point bits. For any input data type, the block casts it as a Fix_20_10 data type first, and works through the algorithm with this data type. The output obtained from this block is also a Fix_20_10 data type. With 20 units and

data with of 20_10, the accuracy achieved is reasonable, and approximates the angle obtained from the Simulink model, as shown in Figure 5.18.

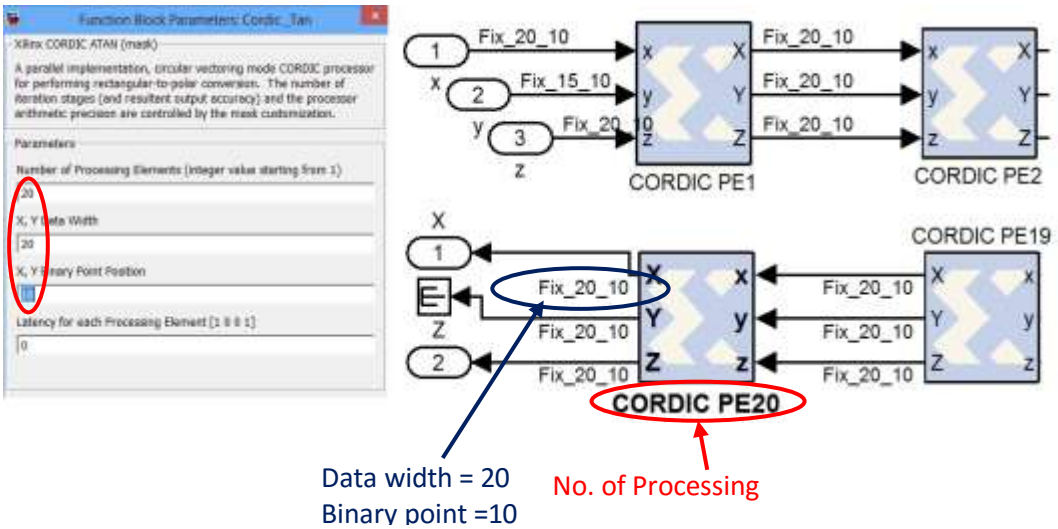


Figure 5.17 Settings of the Cordic aTan block

It has to be noted that the Cordic tan block introduces a delay of 3 cycles, which is denoted as z^{-3} on the block itself. Hence, instead of getting the voltage internal angle and sector at the q0 terminals of the TDDs, we get the internal angle and sector of the current. Hence, one has to carefully observe the sequence of the outputs obtained when the TDM is used with a Cordic atan block as a part of the time-multiplexed code.

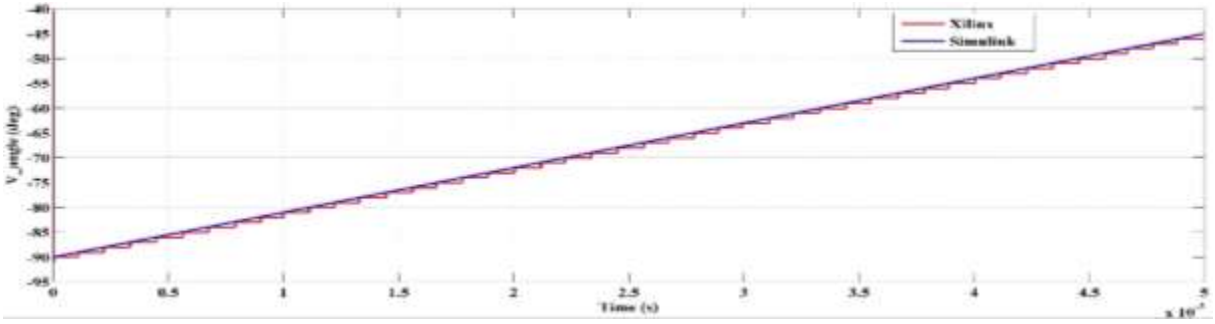


Figure 5.18 Comparison of VSV angle obtained from the Simulink and Xilinx

One way is to observe the outputs and extract the data accordingly, or we could introduce an extra delay cycle by setting the "Latency" of the Cordic aTan block to 1. Then, the total number

of delay cycles would become 4, an even number, which does not cause uncertainty in the sequence of the outputs when using a two-input TDM.

5.4.3 Sector Identification: The next step is to compute the sectors and internal theta (0˚ to 60˚) within a sector. We have to remember that for finding the internal theta, there is no "mod" block in Xilinx. The method for finding the modulus of a number involves a series of subtraction and addition, for which it is best to convert the angle to the [0, 360] range. If not, it will result in a wrong answer. The conversion is straightforward, and the same as in the Simulink model.

The Sector Computation block is somewhat different here. We could use the same equivalent Xilinx blocks, but it would require 6 adders, which would again utilize a fair amount of slices on the FPGA. We replace the adders with a simple "Concatenate" block, which allows the user to concatenate two or more Boolean inputs, and obtain an unsigned integer at the output. If the block has 3 inputs, then we could get the numbers 0 to 7 as the output from the block, depending on the status of the input bits. This will be explained when we calculate the sectors using Table 5.1. The voltage space vector sectors are tabulated in Table 5.1. The sector computation block is shown in Figure 5.19.

Table 5.1 VSV sectors

VSV Sectors	
Sector	Angle (º)
1	0-60
2	60-120
3	120-180
4	180-240
5	240-300
6	300-360

If the angle is less than 60˚, the sector is the first sector. To check if the angle is between 60˚ and 120˚, a simple logic circuit consisting of NOT and AND gates is used. This is used to check if the angle lies within any of the ranges, as given in Table I. The output of these conditions is of "Boolean" type.

We require a Boolean type input to use the concatenation block. The next part would be how to bring out the "integer" that says the sector is 1 or 2 or so on from these Boolean outputs.

For this, we have to first fix the number of bits required to represent the sector number. The highest sector number is 6, for which we need 3 bits. We first form a table with the digitized values of the sectors and check for the condition when each bit goes high. This data is tabulated in Table 5.2.

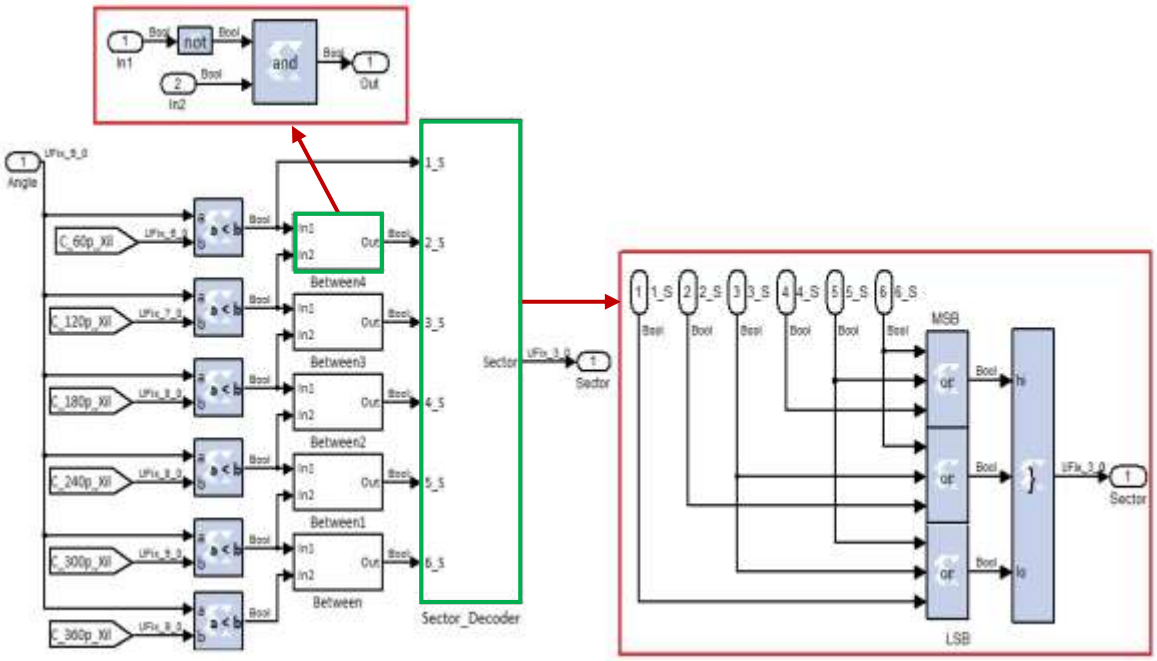


Figure 5.19 Sector identification block using VSV sectors

Table 5.2 Sector Identification Logic

MSB is high when the condition for 4th, 5th OR 6th sectors is true. **MSB=(4_S || 5_S || 6_S)** The second bit is high when the condition for 2nd, 3rd OR 6th sectors is true. **MB=(2_S || 3_S || 6_S)**	**Sector No.**				The LSB is high when the condition for the 1st, 3rd OR 5th sectors is true. **LSB=(1_S || 3_S || 5_S)**
	MSB		LSB	Eqvt. Integer	
	0	0	1	1	
	0	1	0	2	
	0	1	1	3	
	1	0	0	4	
	1	0	1	5	
	1	1	0	6	

Remember that we are going to combine six Boolean inputs to obtain a three bit Boolean output, which is going to represent the sector number as an integer using the concatenate block. The six Boolean inputs are the status of the conditions that check the range of the angle in which the SV angle is. Now, we know that at a time, only one condition can be true. Say the SV angle is 270˚, which triggers the 5th condition to be true. All the other conditions are obviously false. Hence, we get a binary input of the pattern 000010, which correspond to the terminals 1_S through 6_S.

Table 5.2 comes into the picture now. The conditions for the MSB, MB and LSB are checked. MSB becomes high and the LSB becomes high, giving a Boolean output of 101. These bits are now concatenated and the output is obtained as 5.

Though the concept might seem complicated, it is quite simple, involving a few logic gates alone. The voltage and current sectors obtained are shown in Figures 5.20 (a) and 5.20 (b) respectively, wherein the outputs are seen to match with those obtained from the Simulink module as well.

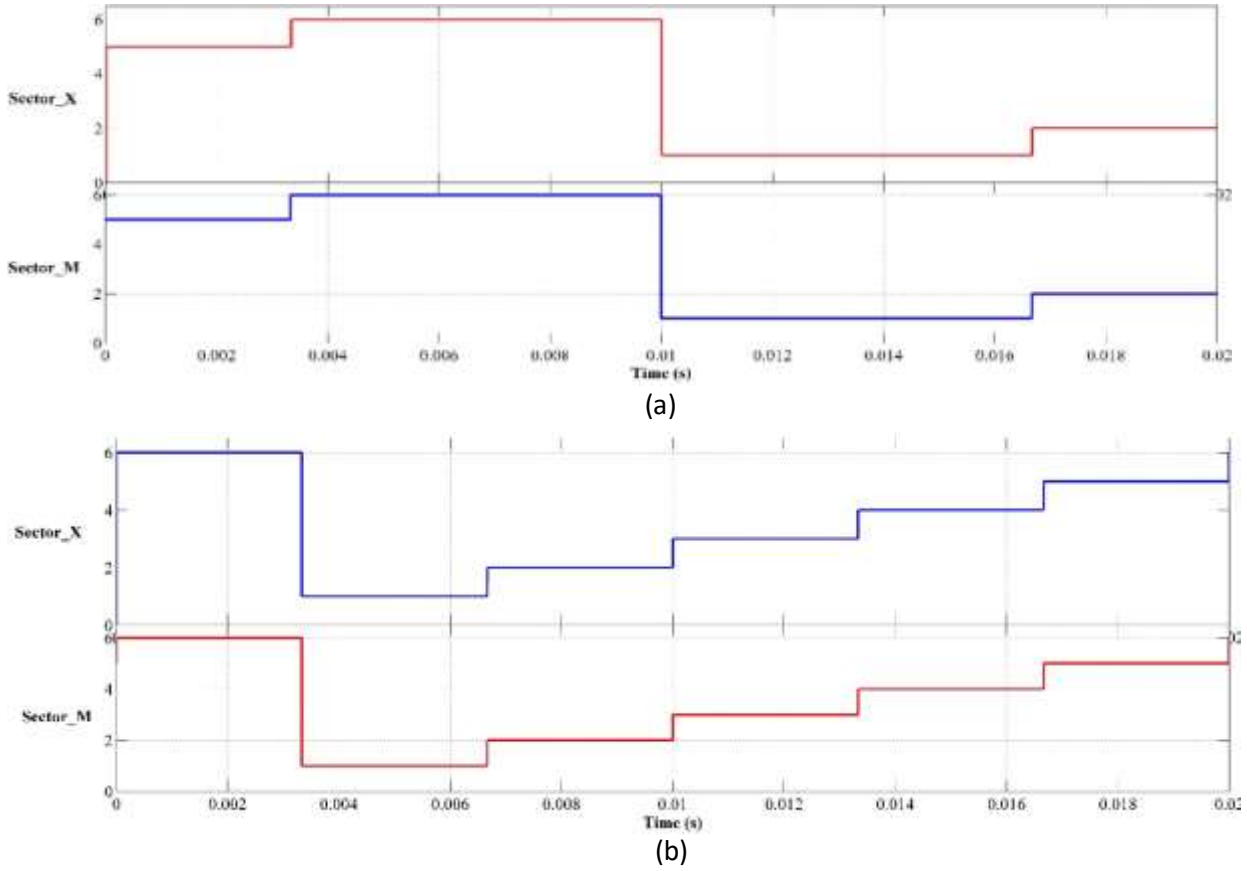


Figure 5.20 Sectors obtained from Xilinx and Simulink (a) VSV Sectors (b) CSV Sectors

5.4.4 Internal angle calculation: Usually, the location of the space vector in a sector spanning 60˚ is found using the modulus operator, which is a straightforward method. From the angle, the internal angle is calculated as in Equation (5.3).

$$\text{Internal angle} = \text{mod}(\text{angle}/60) \tag{5.3}$$

But there is no such block in the Xilinx blockset to implement Equation (5.3) directly. One has to perform this operation by using basic arithmetic blocks. When the space vector is the first sector, its angle will be in the range of 0˚ to 60˚, which will correspond to the internal angle itself. However, in the other sectors, the case is not so. One idea would be to find a reference for calculating the angle within a sector. The previous sector's maximum angle limit could be taken as one such reference. If the angle of the space vector is subtracted from the previous sector's maximum angle, the internal angle can be found.

Let us consider the angle is equal to 130˚ now, and we find that the location is the third sector. If we subtract the second sector's maximum angle, 120˚ from 130˚, we get 10˚. This corresponds to the internal angle. We have to tell the controller, which value we have to subtract. For this, we use the sector number as the reference to pass this information through a multiplexer, shown in Figure 5.21.

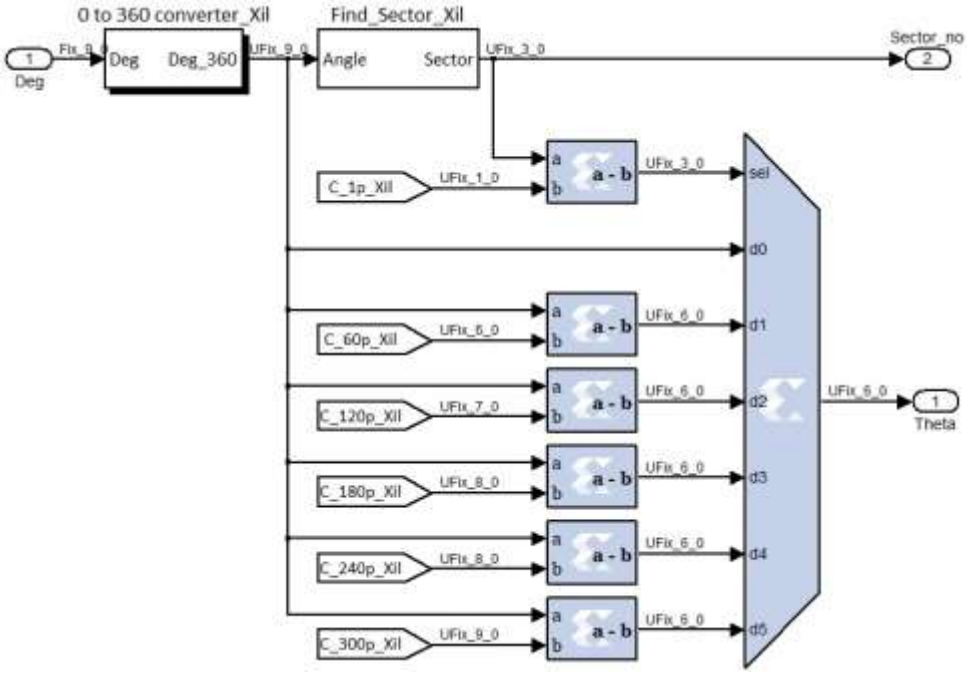


Figure 5.21 Internal angle computation

From Figure 5.21, we use the sector number to tell the controller that when the sector is 1, it has to pass the angle itself as it is. When the sector is 2, the internal angle will be obtained by subtracting 60 from the angle. Similarly, when the sector is 3, the internal angle will be the angle minus 120. The same applies for other sectors as well, which can be inferred directly from Figure 5.21.

Figure 5.22 shows the internal angle of the VSV obtained from the Xilinx and Simulink modules. It can be inferred that the Xilinx output approximates the Simulink output.

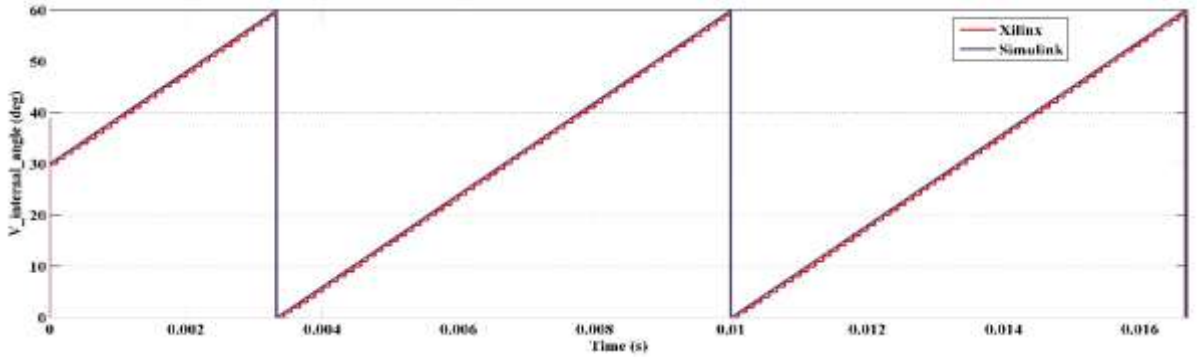


Figure 5.22 Internal angle of the VSV

5.4.5 Initial TDM adjustment: The output data from the TDD is obtained after an interval of 320 ns, until which the current and voltage sectors and the internal angles are zero, assigned by the controller. The sector cannot be zero. Hence, we check for a zero-sector condition. If it is zero, we assign an initial value of 1 to the sector. This is shown in Figure 5.23.

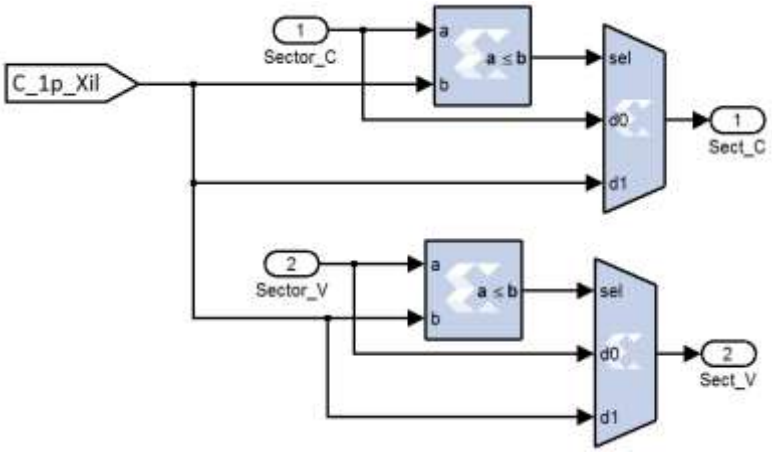


Figure 5.23 Sector Initialization

5.4.6 Duty cycles: From the internal theta of the VSV and CSV, d_α, d_β, d_γ, d_δ are computed first, from which the duty cycles of the MC, d_1, d_2, d_3, d_4 are calculated. To make use of a single ROM to obtain the duty cycles of the VSV and CSV, the terms θ_v, $(60-\theta_v)$, θ_i and $(60-\theta_i)$ are time-multiplexed. Figure 5.24 shows the block that computes the duty cycles of the CSV and VSV.

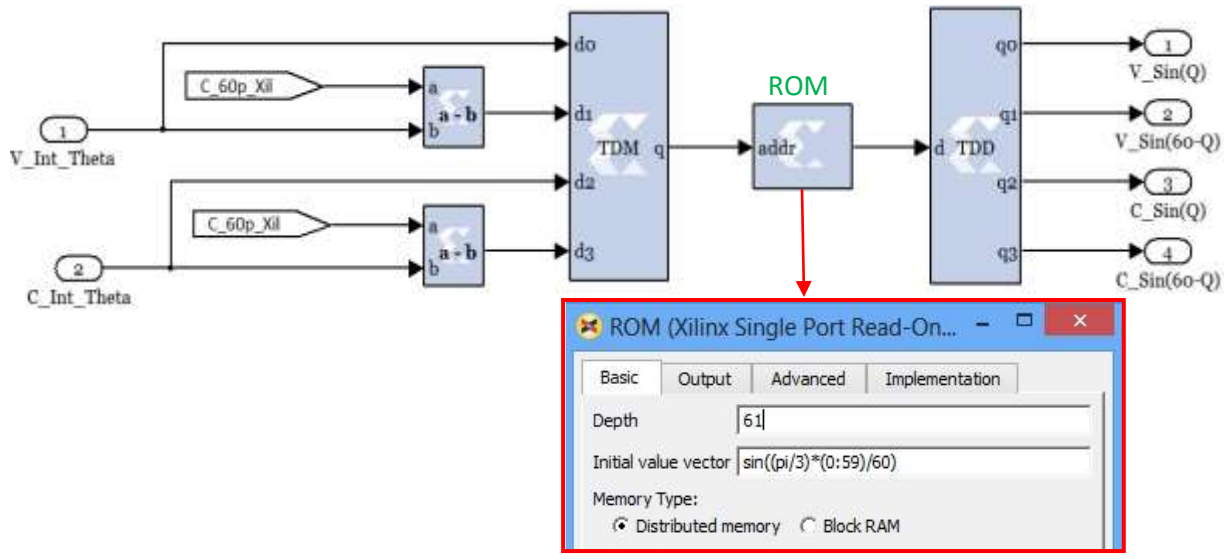


Figure 5.24 Calculation of duty cycles of the VSV and the CSV

The ROM computes the sine of the angle at its input. It considers the input as the address of a location in its memory block. The internal angle can never exceed 60˚. Including 0˚ and 60˚, we need to find the sine value of 61 angles. Hence, the depth of the ROM is set at 61, with its locations addressed from 0 to 60. The expression given in the “Initial value vector” field stores the sine of the respective address in that address itself. Hence, the location 0 will have the value sine (0), which is zero in it. The location with address 60 will have sine (60), which is nothing but 0.866 stored in it. When the angle is 60˚, the location 60 on the ROM is referenced, which gives 0.866 as the output. The four duty cycles in comparison with those obtained from Simulink are shown in Figure 5.25. The duty cycles of the MC are computed as shown in Figure 5.26.

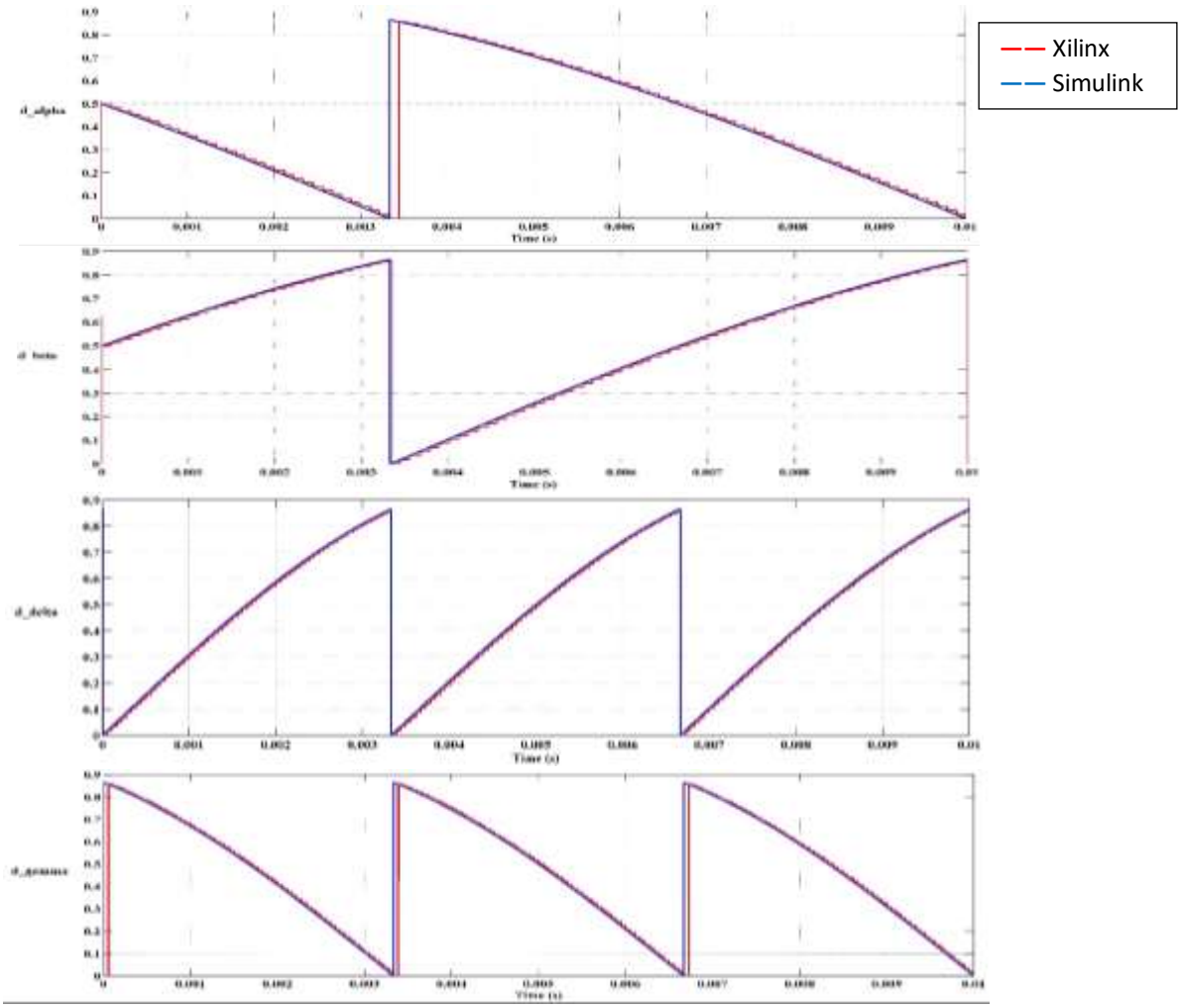


Figure 5.25 Duty cycles of the VSV and CSV from Xilinx and Simulink

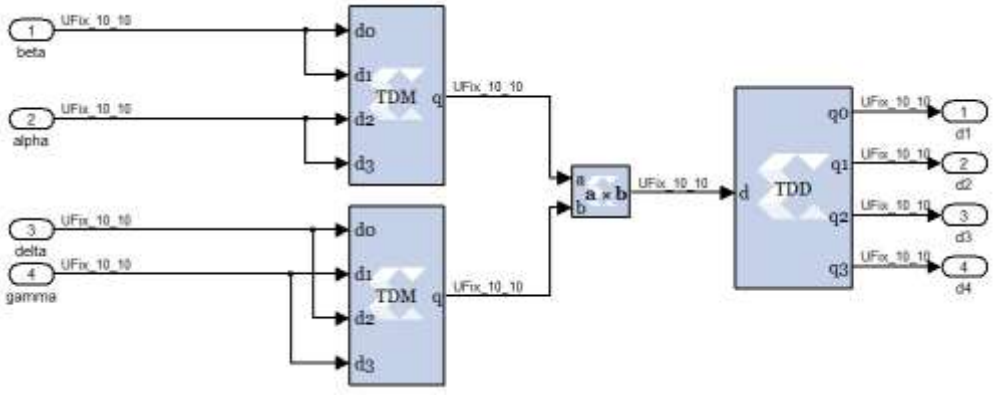


Figure 5.26 Duty cycles of the MC

Time-division multiplexing has been utilized to avoid the use of four multipliers. Since we need to multiply four values to get the duty cycles d1, d2, d3 and d4. Two four-input TDMs can be used in parallel to multiply the respective duty cycles of the VSV and CSV. The duty cycles of the MC are shown in Figure 5.27.

5.4.7 Timing Generator: The duty cycles of the MC are compared with a ramp, more specifically a saw tooth signal of frequency 3 kHz to generate the timing pulses for the MC switches. A ramp signal is generated using a counter of sample period equal to the Simulink period, 20 ns. We know that all the signals in the Xilinx model are sampled every 320 ns for reasons already explained. However, we can send the output of the model at a high sampling frequency by using one signal in the final stage that can force the output data rate to 1.

The timing pulses are used to generate the pulses for the nine bi-directional switches at the last stage of the DSVM block using a multiplexer. The select line of the multiplexer is the timing pulse itself, and the switching vectors would be one of the data lines. The sample rate of the output data of a multiplexer is always equal to that of its Select line. Hence, to effectively obtain the switching pulses at a high sample rate even though the rest of the data are sampled at a comparatively low sample rate, the timing pulses are generated using an up-counter of sample period equal to 20 ns. Figure 5.28 shows the Timing Generator block.

It is very similar to that of the Simulink model, except for the generation of the carrier wave. An up-counter is configured to obtain a sawtooth wave at a frequency of 3 kHz. The gain block is used as a normalization factor to obtain the unity peak amplitude carrier signal. Figure 5.29 shows the timing pulses thus generated.

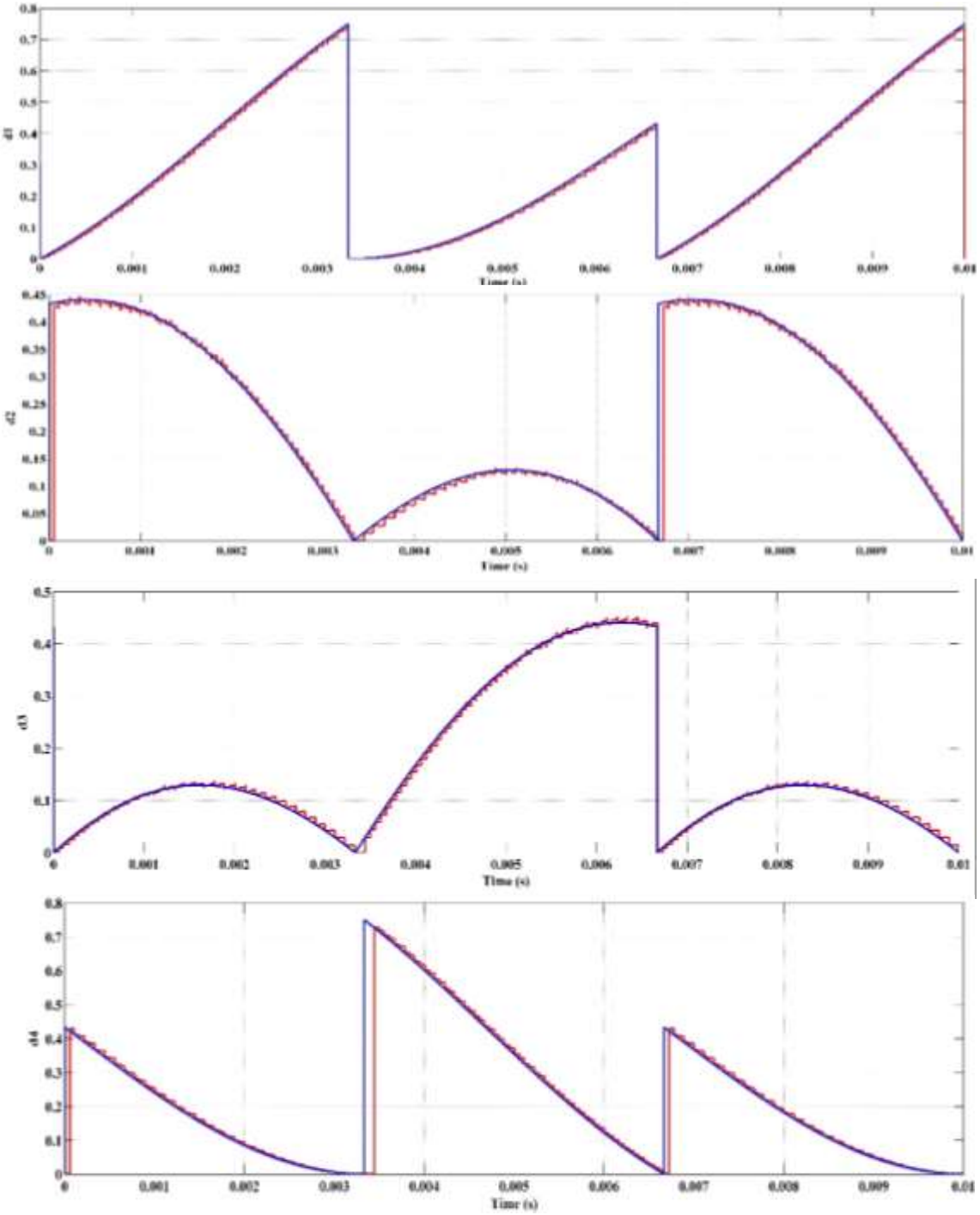


Figure 5.27 Duty cycles of MC

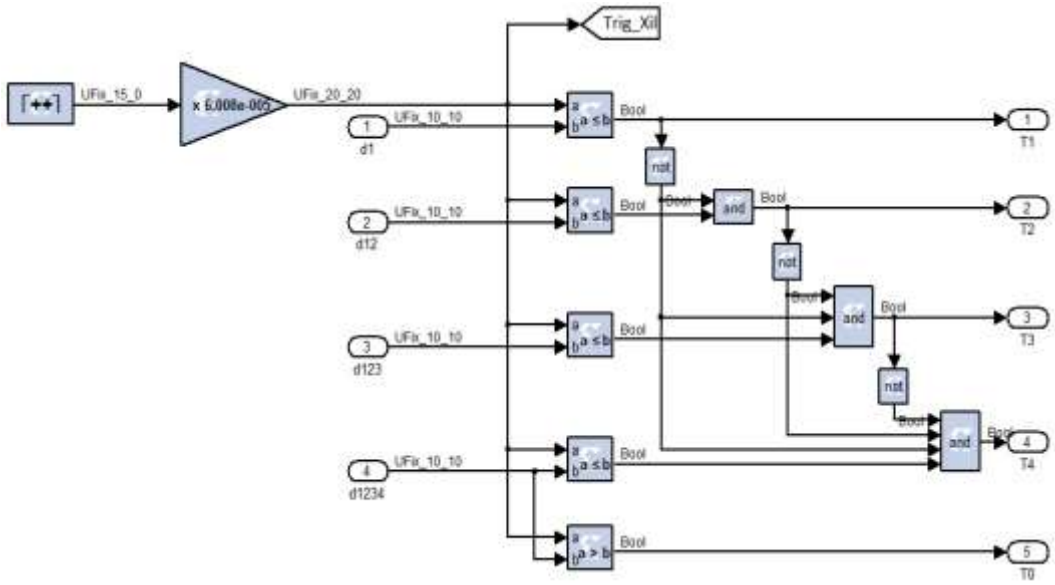


Figure 5.28 Timing Generator using the Xilinx Blockset

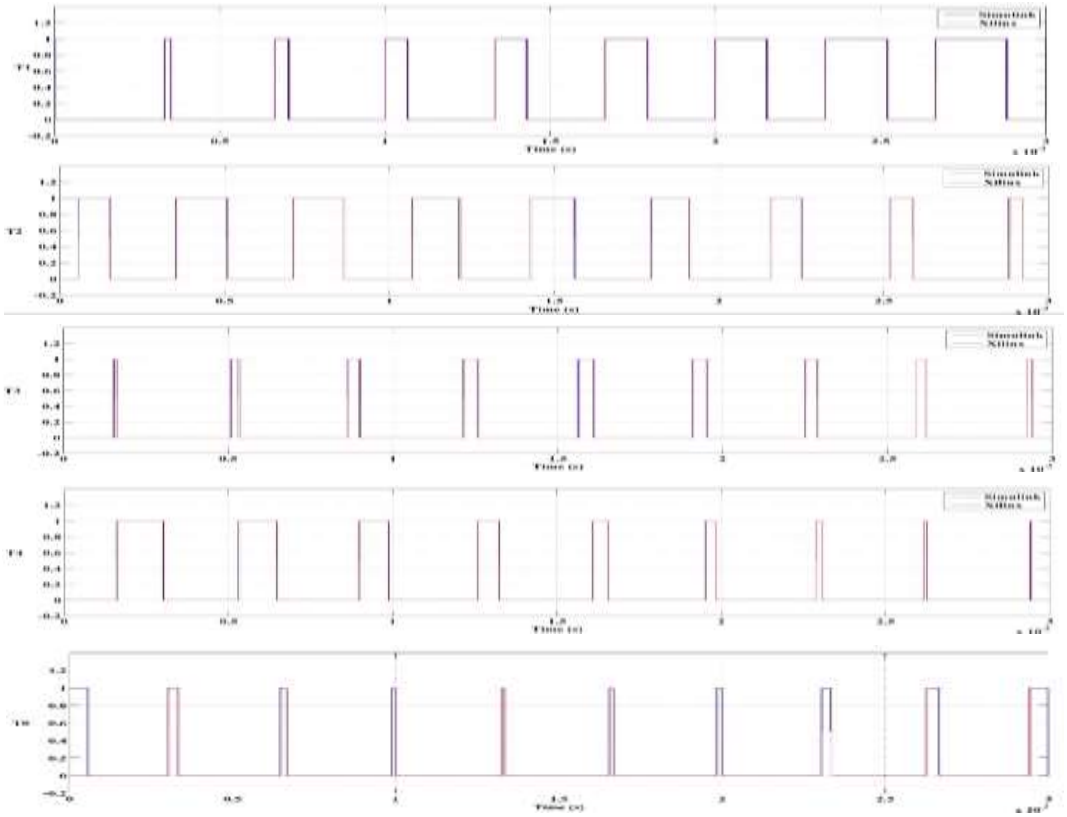


Figure 5.29 Timing pulses obtained from Xilinx and Simulink

5.4.8 Switching Vector Selection: From the location of the CSV and VSV in terms of their respective sector numbers, the switching state to be applied is selected from Table 5.3 in the "DSVM for MC in MATLAB/Simulink" chapter. Figure 5.30 shows the switching state selection block.

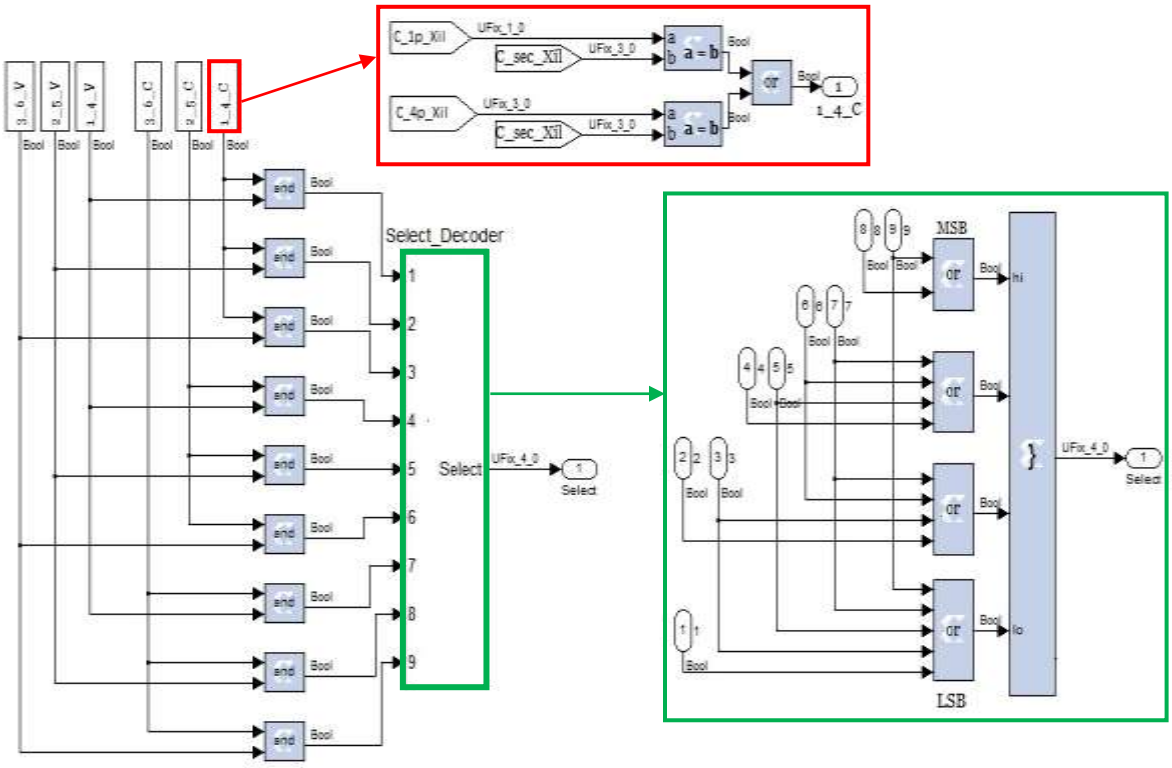


Figure 5.30 Switch state selection

There are nine possible combinations of current and voltage sectors. This arises because both the space vectors are rotating in the αβ plane at different angular velocity. Hence, the voltage and current sectors need not be the same at an instant of time. The block highlighted using red colour in Figure 5.30 checks whether the current sector is 1 or 4. The other five modules at the top left hand corner check for the respective sector equivalency of current and voltage sectors.

Similar to the Sector Identification module that uses a bit-wise logic to obtain the sector number, a reference number for the switch state number can also be extracted. Table 5.3 shows the switch state identification logic. Say for example, the sector numbers K_v and K_c are 4 and 3 respectively. From Figure 5.30, it can be seen that the condition connected to port number "7" of the Sector Decoder alone is "high", and all others are low.

In the Sector Decoder block, it is equivalent to the 3rd, 2nd and LSB bits being high. The output of the concatenate block is then the integer 7 that will act as a select line of a multiplexer to get the actual four vectors that are to be applied. This vector selection block is shown in Figure 5.31.

Table 5.3 Switch state Selection logic

2nd bit changes when SS is 2, 3, 6 or 7, i.e.,	Switch state number (SS)					LSB changes when SS is 1, 3, 5, 7 or 9, i.e.,
	MSB	3rd	2nd	LSB	Eqvt. Integer	
2nd= (1_4_C and 2_5_V) **OR** (1_4_C and 3_6_V) **OR** (2_5_C and 3_6_V) **OR** (3_6_C and (1_4_V)	0	0	0	1	1	**LSB**= (1_4_C and 1_4_V) **OR** (1_4_C and 3_6_V) **OR** (2_5_C and 2_5_V) **OR** (3_6_C and 1_4_V) **OR** (3_6_C and 3_6_V)
	0	0	1	0	2	
	0	0	1	1	3	
	0	1	0	0	4	
3rd bit changes when SS is 4, 5, 6 or 7, i.e.,	0	1	0	1	5	MSB changes when SS is 8 or 9, i.e.,
	0	1	1	0	6	
	0	1	1	1	7	
3rd = (1_4_C and 3_6_V) **OR** (2_5_C and 2_5_V) **OR** (2_5_C and 3_6_V) **OR** (3_6_C and 1_4_V)	1	0	0	0	8	**MSB=** (3_6_C & 2_5_V) **OR** (2_6_C & 3_6_V)
	1	0	0	1	9	

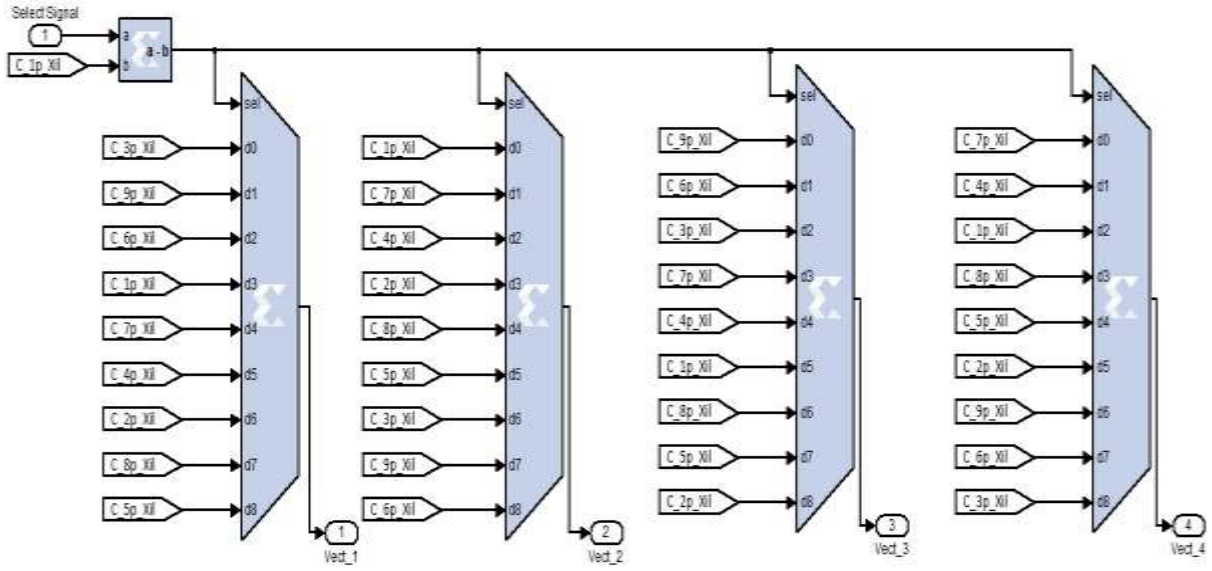


Figure 5.31 Vector Selection Block

This block is used instead of employing four ROMS to store the four vector values. With one select signal that contains the information about the sector location of the CSV and the VSV, the four switching states can be obtained using four multiplexers. The constants connected at the nine terminals of the four multiplexers correspond to the values in Table 5.3 of DSVM in Matlab document.

For the example we have considered the number seven minus one, six appears on the select line of the four multiplexers. The vectors selected are 2, 3, 8 and 9 and correspond to vector 1, vector 2, vector 3 and vector 4 respectively. These are the same vectors that are given in Table 5.3 of the Matlab document corresponding to K_c of 3 and K_v of 4.

5.4.9 Vector Sign Assignment:

A positive or negative sign of the first and the fourth switching vector depends on the polarity of Equation (5.4)

$$\text{Duty cycle polarity} = (-1)^{K_v + K_i}. \qquad (5.4)$$

If it amounts to one, the first and fourth switching states are positive, otherwise, they are to be negated. If the above expression is positive, then the second and third vectors are negated,

otherwise they are positive. This logic is implemented in the Vector Sign Assignment block, shown in Figure 5.32.

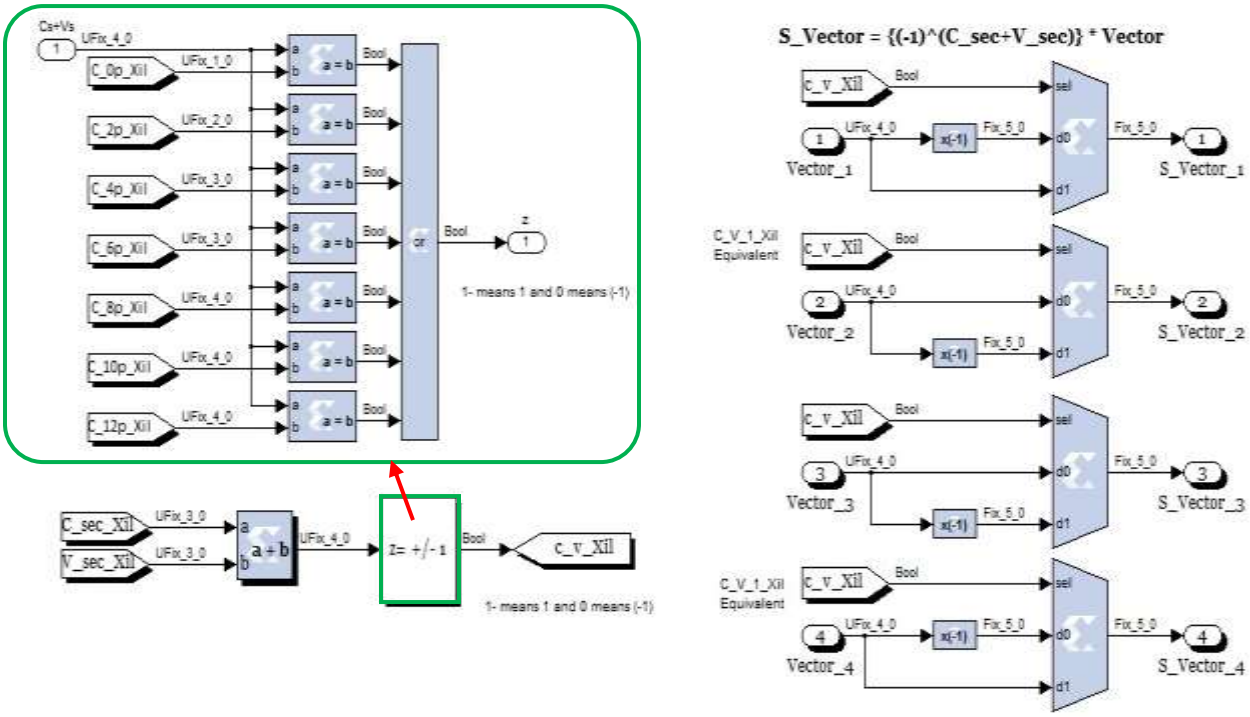


Figure 5.32 Vector Sign Assignment

The current sector and voltage sector is summed, and checked whether the result is an odd or even number. If it is an even number, then Equation (5.4) would be positive. If it is an odd number, Equation (5.4) would be negative. We now compare the sum obtained to even numbers from 0 to 12.

For our example, the sum of K_v and K_c is 4+3=7. As it is not an even number, the output of the block, c_v_Xil is zero. This signifies that the first and fourth vectors become negative, while the second and third vectors are positive. The four multiplexers are used to implement this sign change depending on the value of c_v_Xil. The same can be inferred when the sum of the sectors is an even number.

5.4.10 Vector Generation:

The inputs to this block are the four vector numbers. This block changes the vector numbers from ±1 to ±9 to 1 to 18, as tabulated in Table 5.4, for the DSVM Code. Figure 5.33 shows the vector generation block.

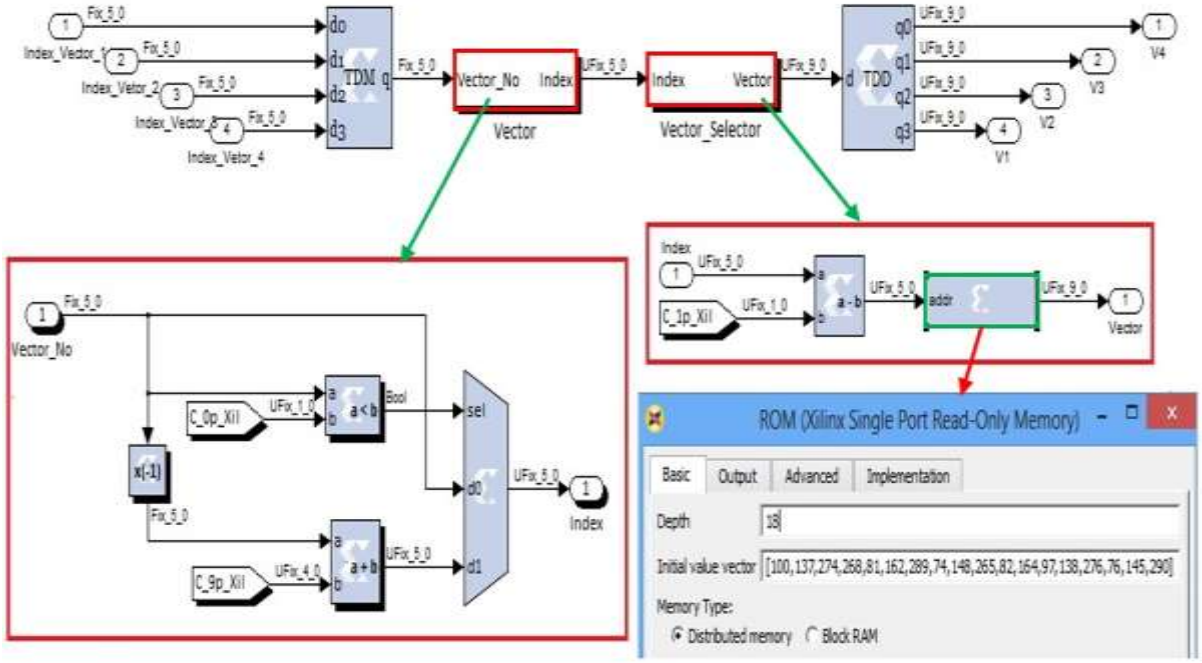


Figure 5.33 Vector generation

The vector number is passed as the select line of the multiplexer. If it is less than zero, the vector is passed as such. This is done by connecting the vector itself to the d0 terminal of the mux. If it is less than zero, the select line goes high, and the vector has to be converted to a positive number. For this purpose, the incoming vector number after being added to nine, is given at the d1 terminal of the multiplexer.

Each vector number ranging from 1 to 18 actually corresponds to a unique nine-bit switching vector. The integer equivalent of eighteen nine-bit switching vectors are stored in the ROM and retrieved by referencing the address of the location. Therefore, the user has to make sure that he enters the integer equivalent of the vectors in order of the address location numbers, from 0 to 17. Figure 5.33 shows the setting of the ROM block. Table 5.4 shows the integer equivalent of the switching vectors.

Table 5.4 Integer equivalent of switching vectors

Switch state	Switching vector	Integer eqvt. of the switching vector
1	[0 0 1 1 0 0 1 0 0]	100
2	[0 1 0 0 0 1 0 0 1]	137
3	[1 0 0 0 1 0 0 1 0]	274
4	[1 0 0 0 0 1 1 0 0]	268
5	[0 0 1 0 1 0 0 0 1]	081
6	[0 1 0 1 0 0 0 1 0]	162
7	[1 0 0 1 0 0 0 0 1]	289
8	[0 0 1 0 0 1 0 1 0]	074
9	[0 1 0 0 1 0 1 0 0]	148
10	[1 0 0 0 0 1 0 0 1]	265
11	[0 0 1 0 1 0 0 1 0]	82
12	[0 1 0 1 0 0 1 0 0]	164
13	[0 0 1 1 0 0 0 0 1]	097
14	[0 1 0 0 0 1 0 1 0]	138
15	[1 0 0 0 1 0 1 0 0]	276
16	[0 0 1 0 0 1 1 0 0]	076
17	[0 1 0 0 1 0 0 0 1]	145
18	[1 0 0 1 0 0 0 1 0]	290

As this is common for all the vector numbers, the four vectors are time-division multiplexed and pumped into this block. The four nine-bit switching vectors corresponding to the four vectors, are obtained from the TDD of this block.

5.4.11 Switching Vector Timing:

The final step is to generate the switching pulses for the MC switches by timing the switching vectors using the timing pulses generated earlier. Figure 5.34 shows the block that generates the switching pulses of the MC from the switching vectors obtained.

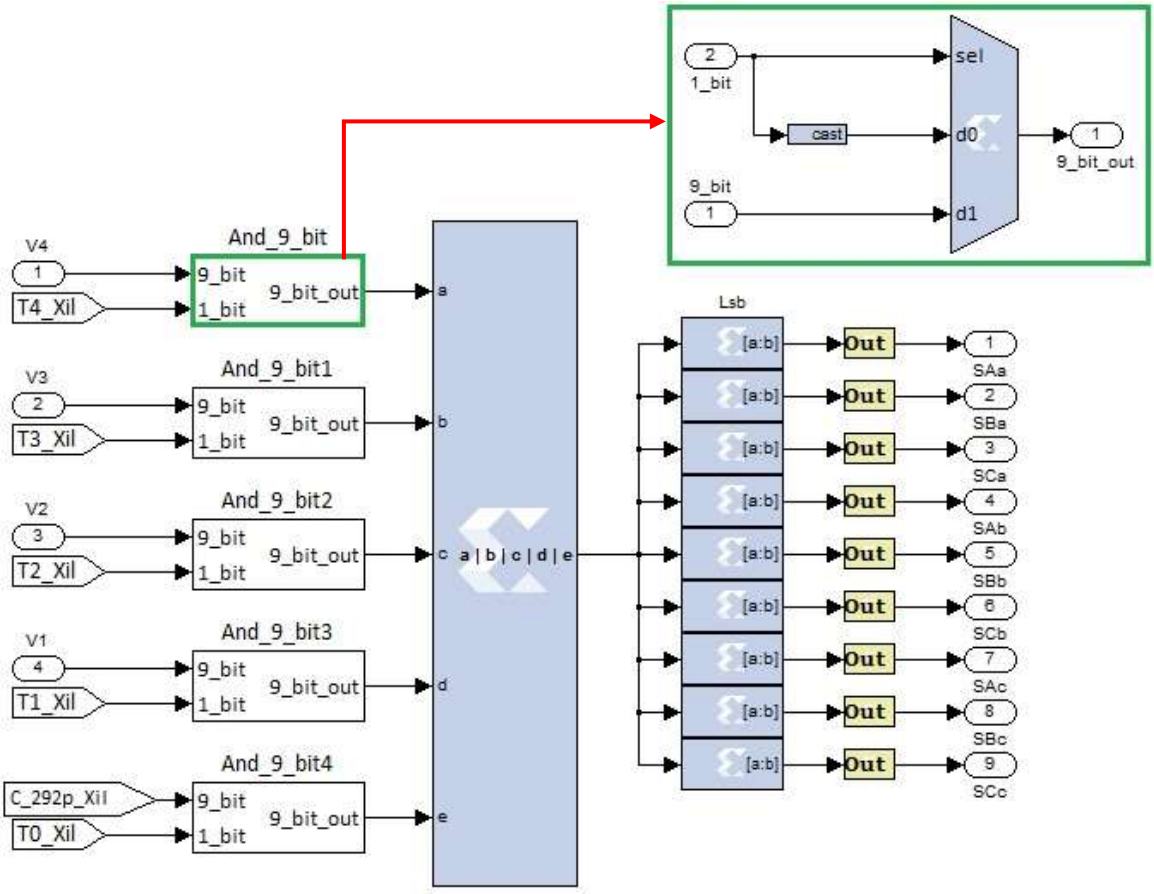


Figure 5.34 Switching Vector Timing

When the timing pulse is available or high, the corresponding switching vector is applied. Hence, the timing pulse itself is given as select line of the mux. Finally, each bit in the nine-bit binary number is “sliced” with the MSB as reference to get the switching pulses of the MC. Fig. 5.35 shows the switching pulses to the MC.

The pulses from the Xilinx model are shown in red colour, while the blue colour indicates the pulses from the Simulink model. As the pulses obtained from both models are almost identical, the output voltage waveform is expected to be identical to the Matlab simulation when these pulses generated from the FPGA controller are fed to a matrix converter. The switching pulses have to be delayed before sending them to the devices to avoid a short-circuit of input phases. A Xilinx model has been developed for the four-step commutation circuit to delay the pulses.

5.5 FOUR-STEP COMMUTATION IN MATLAB/XILINX

The same sequential commutation circuit of Figure 2.34 can be implemented in the MATLAB/Xilinx interface directly. This would require a large number of registers. We could generate the commutation sequence using a simpler circuit by checking for the occurrence of a falling or rising edge on a switch's pulse from the DSVM, and the load current direction. This is quite simple and easy to implement once the state diagram for the commutation sequence is drawn.

. The sequence of commutation from 'b' phase to 'a' phase, when current direction is positive is given in Table 5.5. Table 5.6 gives the sequence of the same when current direction is negative.

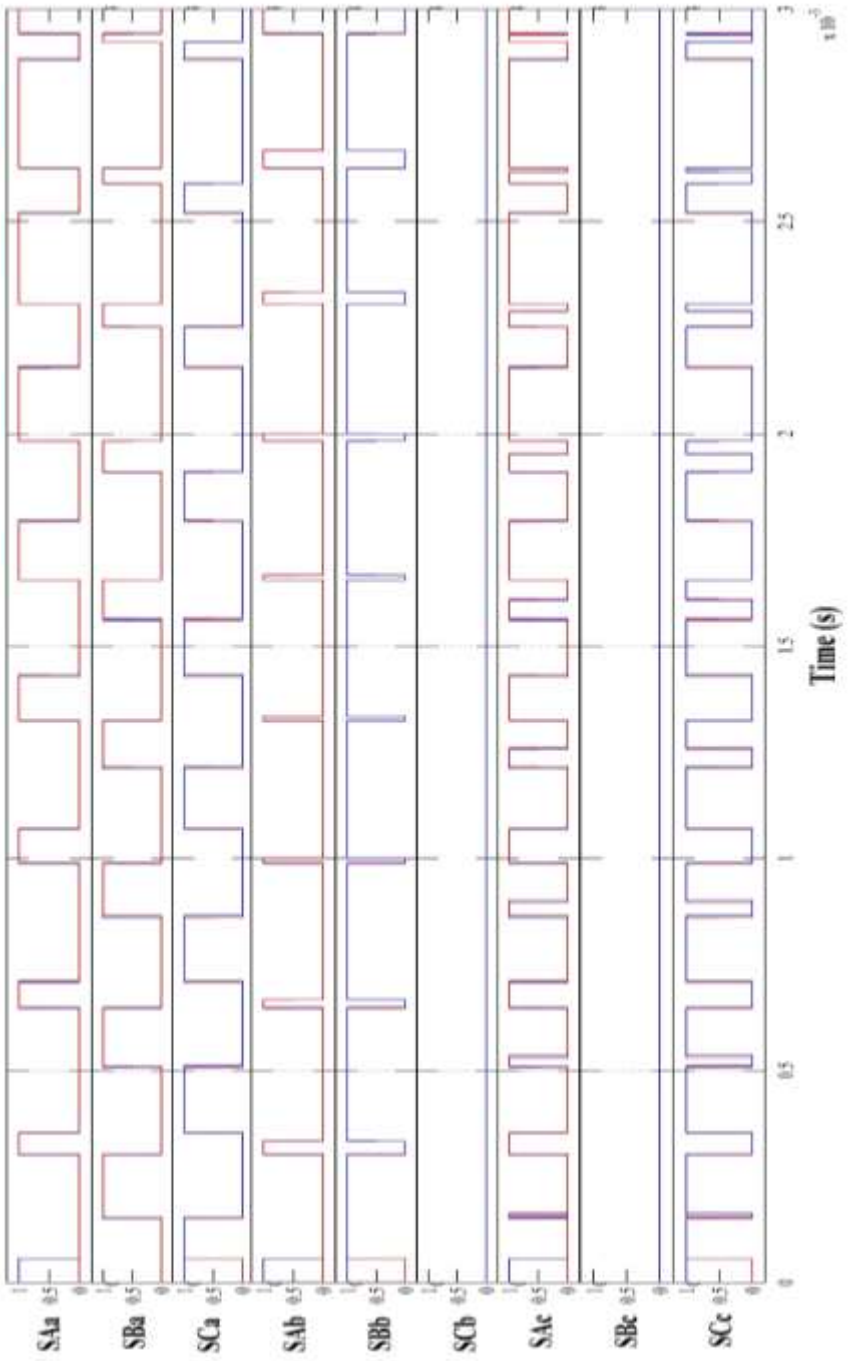


Figure 5.35 Switching pulses of the MC from Xilinx and Simulink models

Table **5.5**. Sequence of commutation when current is positive

$I_A = 1$	SaA , SbA				SaA , SbA			
	SaAp	SaAn	SbAp	SbAn	SaAp	SaAn	SbAp	SbAn
Present state	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
I	1	0	0	0	0	0	1	0
II	1	0	1	0	1	0	1	0
III	0	0	1	0	1	0	0	0
IV	0	0	1	1	1	1	0	0

Table **5.6**. Sequence of the commutation when the current is negative

$I_A = 0$	SaA , SbA				SaA , SbA			
	SaAp	SaAn	SbAp	SbAn	SaAp	SaAn	SbAp	SbAn
Present state	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
I	0	1	0	0	0	0	0	1
II	0	1	0	1	0	1	0	1
III	0	0	0	1	0	1	0	0
IV	0	0	1	1	1	1	0	0

From Table 5.5, one can infer that when the current direction is positive, the sequence for commutation is the same for a rising switching pulse (S= 0 to 1), irrespective of which switch is

going to be turned ON. The same can be observed for a falling pulse (S= 1 to 0). From Table 5.6, when the direction of current is negative, the same sequence can be observed for rising pulse irrespective of which switch is going to be turned on. This applies for the falling pulse too.

The state diagram for implementing four-step commutation based on the switching pulse transition and the current direction is derived from Tables 5.5 and 5.6. The state diagram, shown in Figure 5.36 can be divided vertically into two areas, positive current (I_A=1) and negative current (I_A=0).

NOTE: A switch state is represented by the state of S_{Xp}, the positive switch followed by the state of S_{Xn}, the negative switch.

For example, let us consider that the current is negative, and switch S_{bA} is to be turned-on and S_{aA} is going to be turned off. The following steps will help infer the sequence from Figure 5.36.

a. The sequence to be followed is shown in the left half of the state diagram as current direction is negative.
b. The initial state of switch S_{bA} would be S=0 and that of S_{aA} would be S=1. Please go to the start points for the respective values of 'S'.
c. As a rising edge is detected on S_{bA}, the steps for the transition S=0 to 1 will be followed for this switch.
d. As a falling edge is detected on S_{aA}, the steps for transition S=1 to 0 is followed for switch S_{aA}.
e. Each switch shouldbe hekd at a particular state for the fixed delay time, 600 ns before the next step in the sequence is implemented.
f. Once the final states are reached (S_{bA} =1,1 and S_{aA}=0,0), the switches are to be held in these states until another change in switching pulse is detected.

In our case, as the transition is occurring between phases 'a' and 'b', the switch state of both the switches of S_{cA} would be zero, and it remains so until a change in S_{cA} is detected. This method is quite plain and requires a logic circuit that detects a transition on the incoming switching pulse, a counter that will set the delay between state transitions and also maintain the final switch states, some memory blocks to store the switch states and a decision block to determine which states are passed based on the current direction.

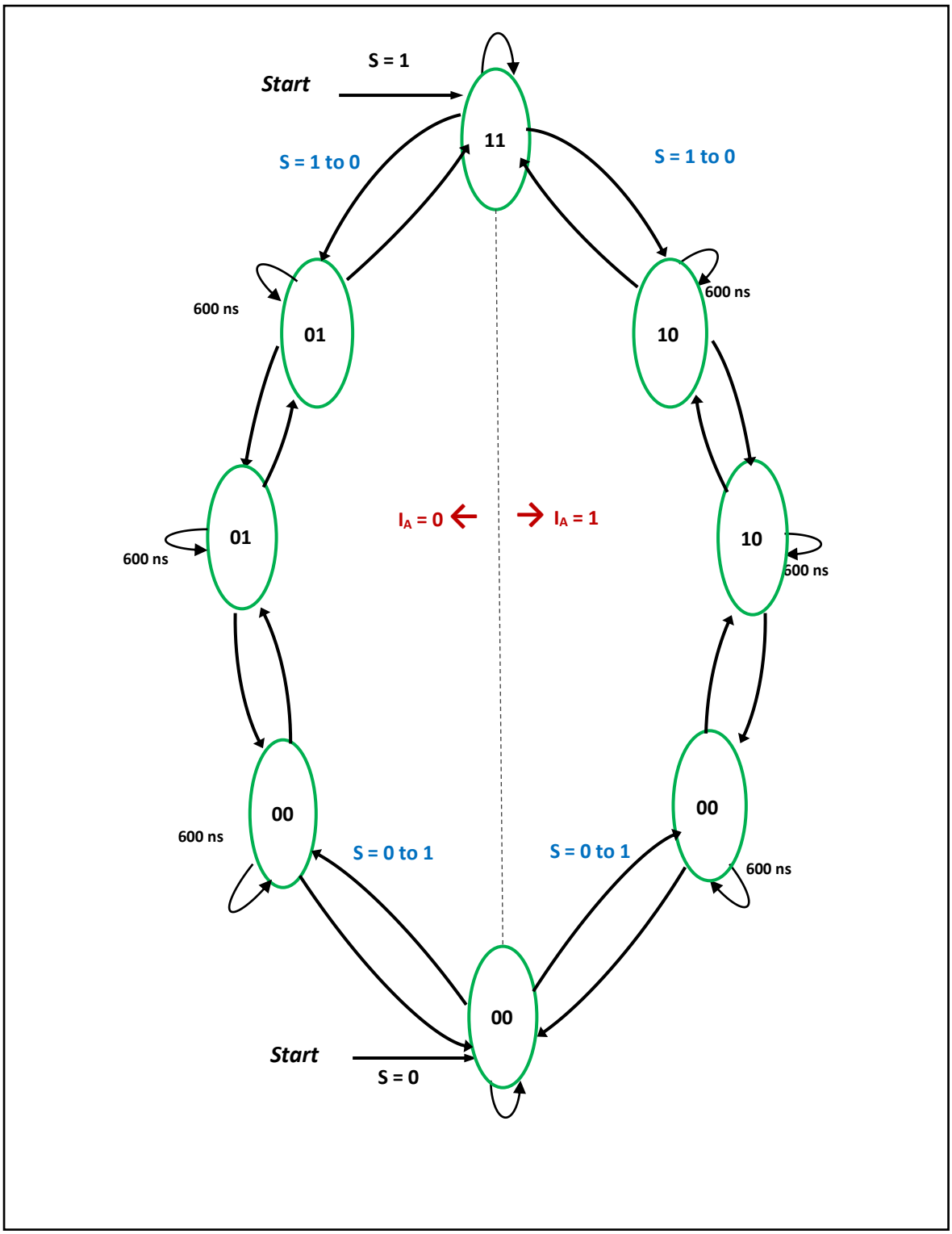


Figure 5.36 Four-step commutation state diagram

Figure 5.37 shows the block diagram of the four-step sequencer for one switch S_{aA}. The block named S_change detects the switching pulse transition. The other two blocks (S=1 to 0, falling and S=0 to 1, Rising) contain the sequence logic. Figure 5.38 shows the change in S_nlock block.

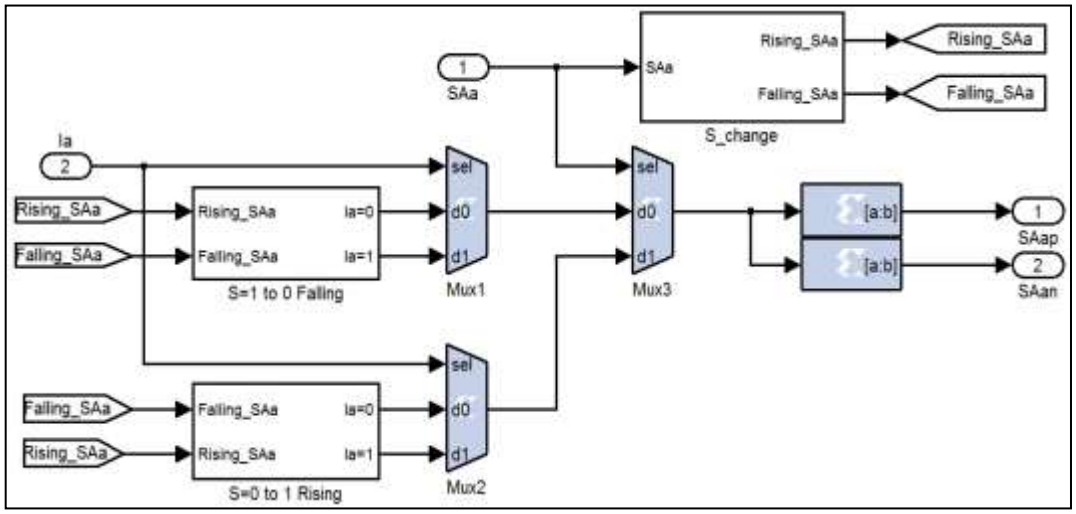


Figure 5.37 Block diagram of commutation sequencer for switch SaA

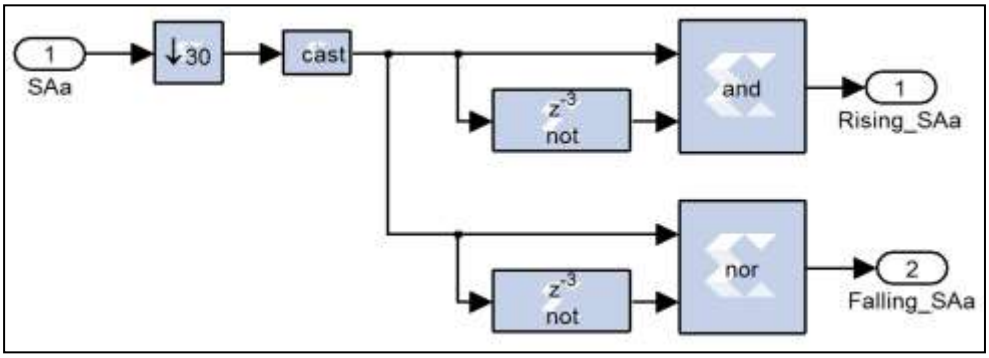


Figure 5.38 Edge detection block

The sample rate of the pulse S_{aA} from the DSVM is 1, corresponding to a sample period of 20 ns. The minimum time required for one-step in the commutation sequence is 600 ns, and a total of three such cycles is needed. Hence, the incoming signal is first down-sampled to 600 ns (sample rate 30). The logic for detecting a rising edge is shown graphically in Figure 5.39 (a), while that of the falling edge is shown in Figure 5.39 (b).

The switching pulse transition information should not change for 3 cycles of 600 ns for completing the commutation sequence. In order to do so, we require the rising and falling edge detection pulse for a duration of 1800 ns. It is for this purpose that we delay the incoming pulses by 3 cycles for generating the edge detect pulses, as shown in Figure 5.38.

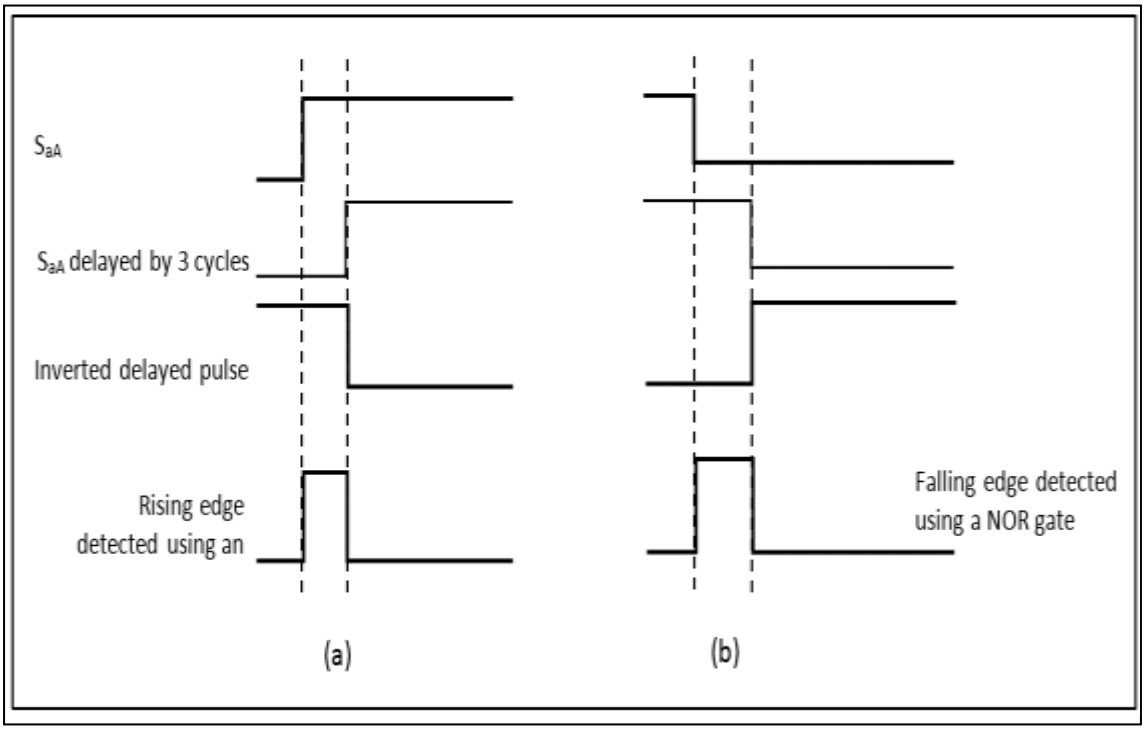


Figure 5.39 rising and falling edge detection

The logic shown in Figure 5.39 is implemented directly to detect the respective edges of S_{aA}. Based on the edge detected, one of the two blocks shown in Figure 5.37 will get triggered and generate the commutation sequence. The following section discusses the two blocks in detail.

Block S=1 to 0, falling: This block generates the commutation sequence for both positive and negative current directions when a falling edge is captured. The output of this block is given to MUX 1, which selects the required sequence depending on the value of the current direction bit. Figure 5.40 shows how the sequence is obtained using this block.

Two two-bit up-counters are used to set the step number (0 to 3). The counter has to start counting when a falling edge is detected. Hence, the 'Falling edge detect' signal is given as the 'Enable' signal of the counter. The rising edge detects signal is given as the reset signal to the

counter, for which the reasons will be evident soon. Also, the sequence of switch states when S= 1 to 0 transition occurs for positive and negative currents are stored in the respective ROMs, as shown in Figure 5.41. It has to be noted that the initial states need not be stored.

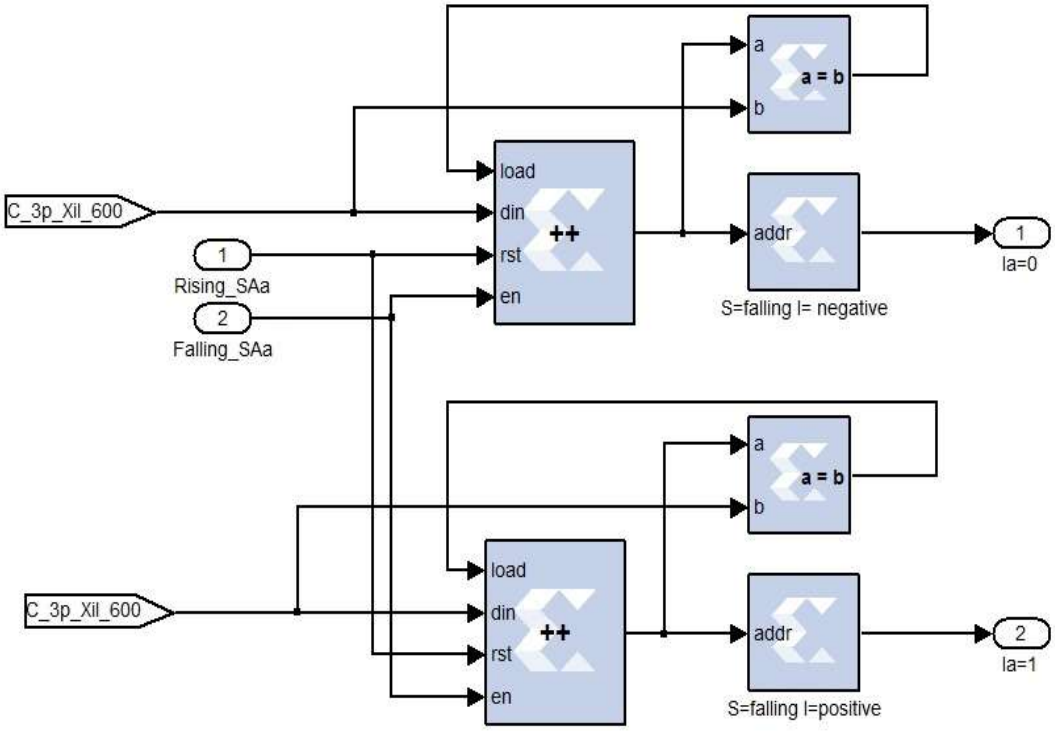


Figure 5.40 Commutation sequence generation when a falling edge is detected

Figure 5.41 Commutation sequence stored in ROM when the switch is to be turned OFF

When a falling edge is detected, the counter starts counting from 0 to 3. The output of the counter references in the memory location in the ROMs. The value stored in the corresponding location is obtained as the output from the ROMs. Once the counter value reaches 3, it means the final state has been reached, i.e., both switches are turned OFF. This state has to be held until the counter is reset, which will happen only if a transition happens from S=0 to 1, meaning that the switch has to come out of the "OFF" state to the "ON" state. To hold the switch in the OFF state until the counter is reset, we use the load and din ports of the counter. These ports can be enabled by setting the counter as shown in Figure 5.42.

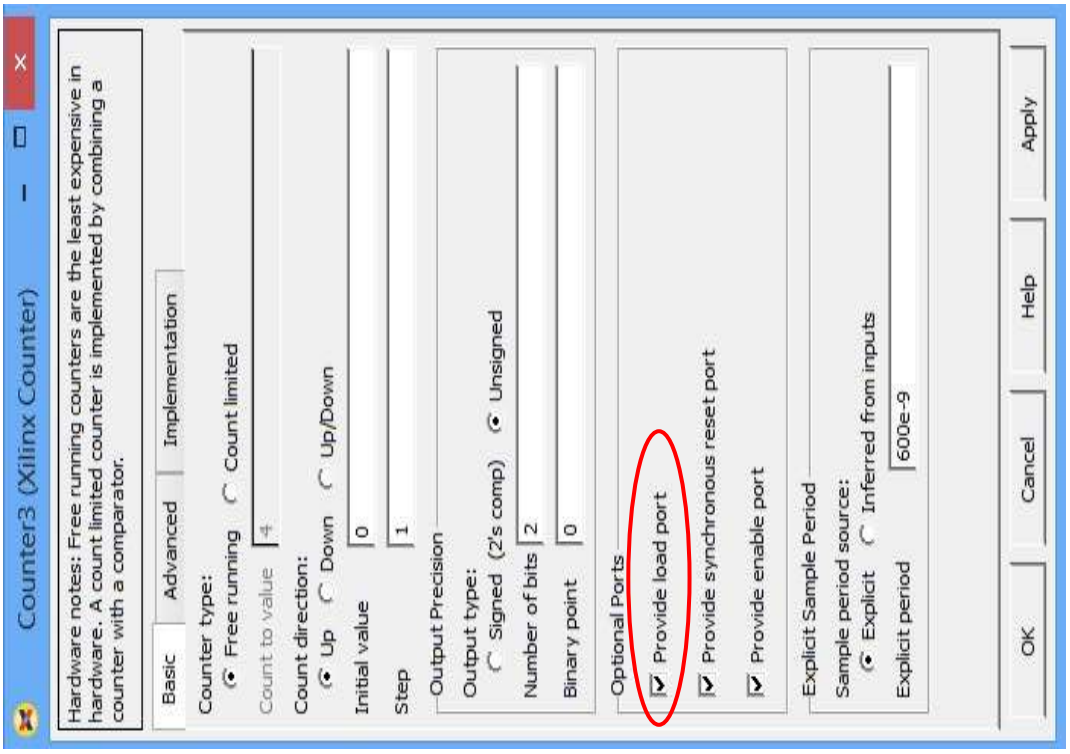


Figure 5.42 Counter settings to uphold the final switch state

The output of the counter is then checked for equivalence with three, as in Figure 5.40. If it is not equal to 3, then the load port is disabled, and the count value is obtained as the output from the counter. If the enable signal is still available, the counting resumes. When the counter output is equal to 3, the 'load' port becomes high, and whatever is given at the 'din' port is passed as the counter output. Also, when the load port is high, the counter does not count. The output of the counter will be 3 (given to 'din' port), and the 'load' line will be maintained high until the counter is reset. In this manner the final state is held until the next rising edge is detected.

Figures 5.43 and 5.44 show the counter and memory block outputs when a falling edge is detected for negative and positive currents respectively.

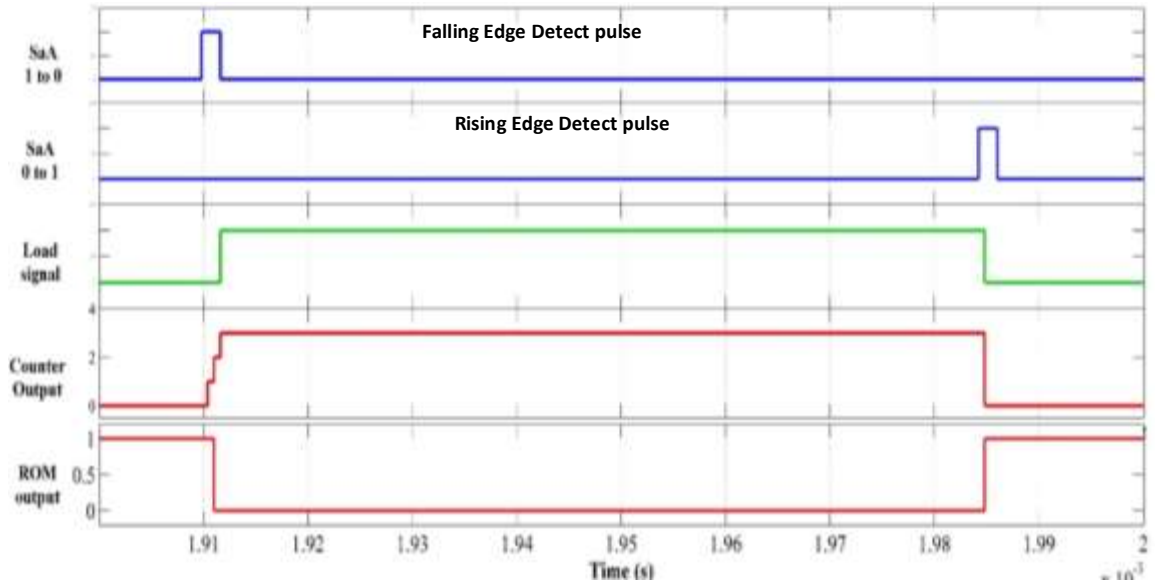


Figure 5.43 Counter output for the negative current when a falling edge is detected

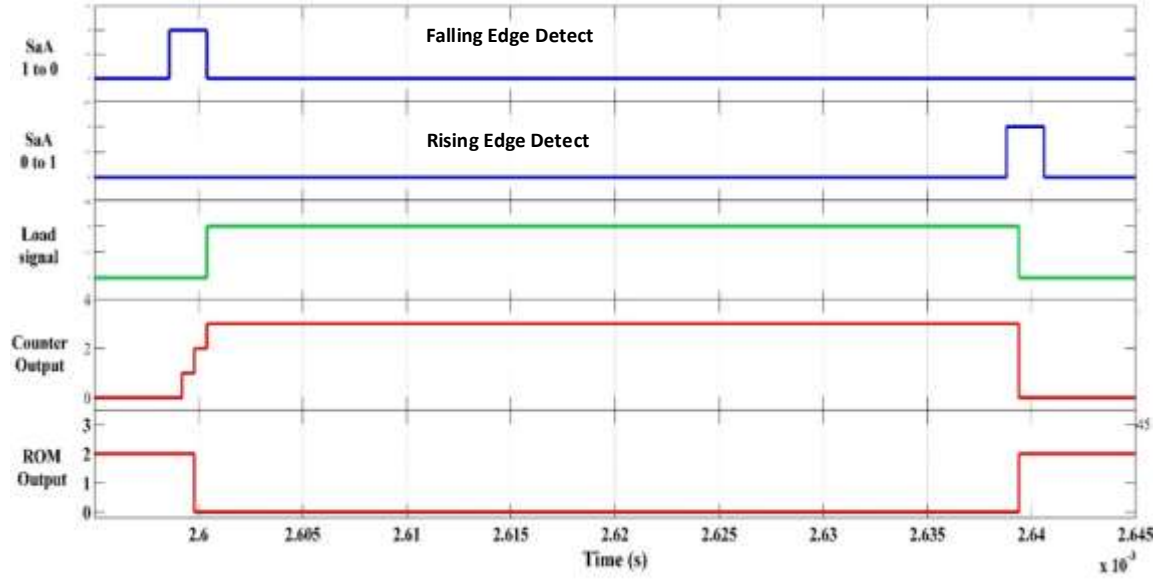


Figure 5.44 Counter output for positive current when a Falling Edge is detected

Block S= 0 to 1, Rising: In the previous block, the counter was reset when a rising edge was detected, as the rising edge pulse was the "reset" signal to the counter. In this block, the rising edge pulse is the "Enable" signal of the counter, and the falling edge pulse is the "reset" signal. The operation is similar to that of the previous block, except that the counter begins to count when a rising edge is detected, and gets reset when a falling edge is detected. The ROM values

correspond to the switch states for S = 0 to 1. The logic circuit and the ROM block settings for rising edge pulse are shown in Figure 5.45.

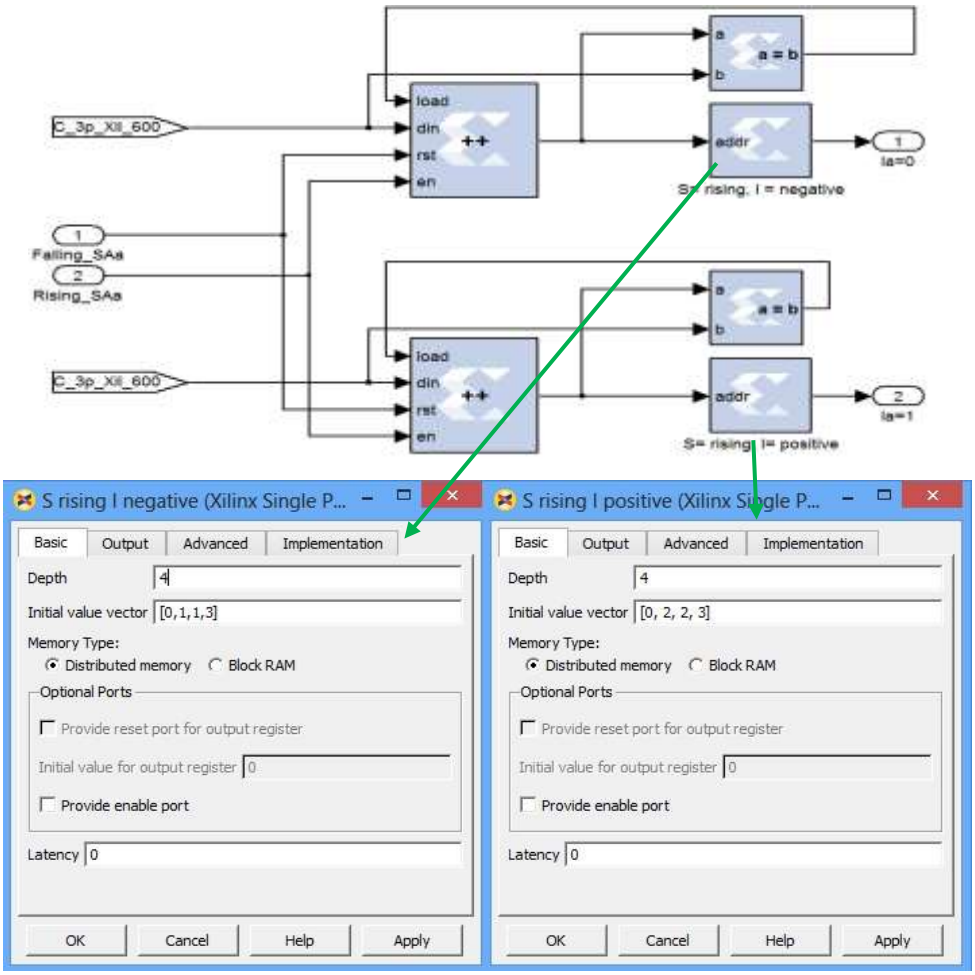


Figure 5.45 Commutation sequence generator when a rising edge is detected

The scope results for the counter and memory blocks are shown in Figures 5.46 and 5.47 for negative and positive current respectively when a rising edge is detected.

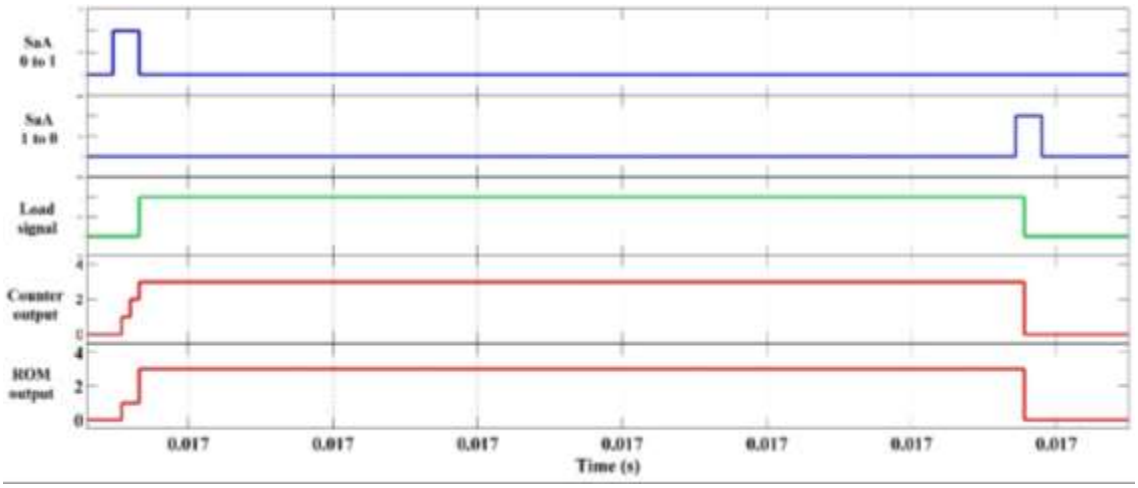


Figure 5.46 Counter and ROM output for the negative current when rising edge is detected

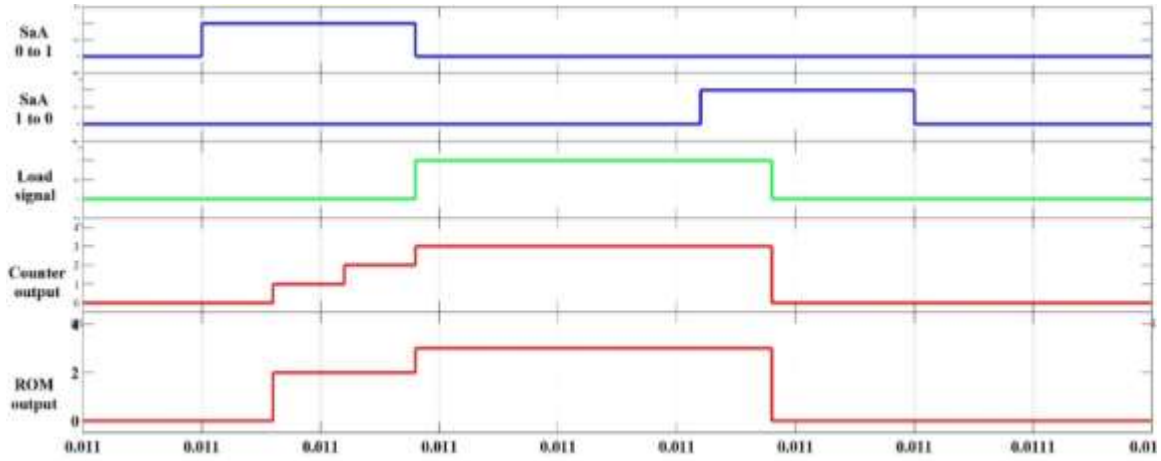


Figure 5.47 Counter and ROM output for positive current when rising edge is detected

The output of the ROM is obtained from the two blocks. The next step would be to select the ROM output corresponding to the current direction, which is done using Mux 1 and Mux 2. Finally, Mux 3 selects the output based on its state (high or low). Figures 5.48 and 5.49 show all the signals in the commutation sequence for a positive current with a falling and rising edge on SaA respectively.

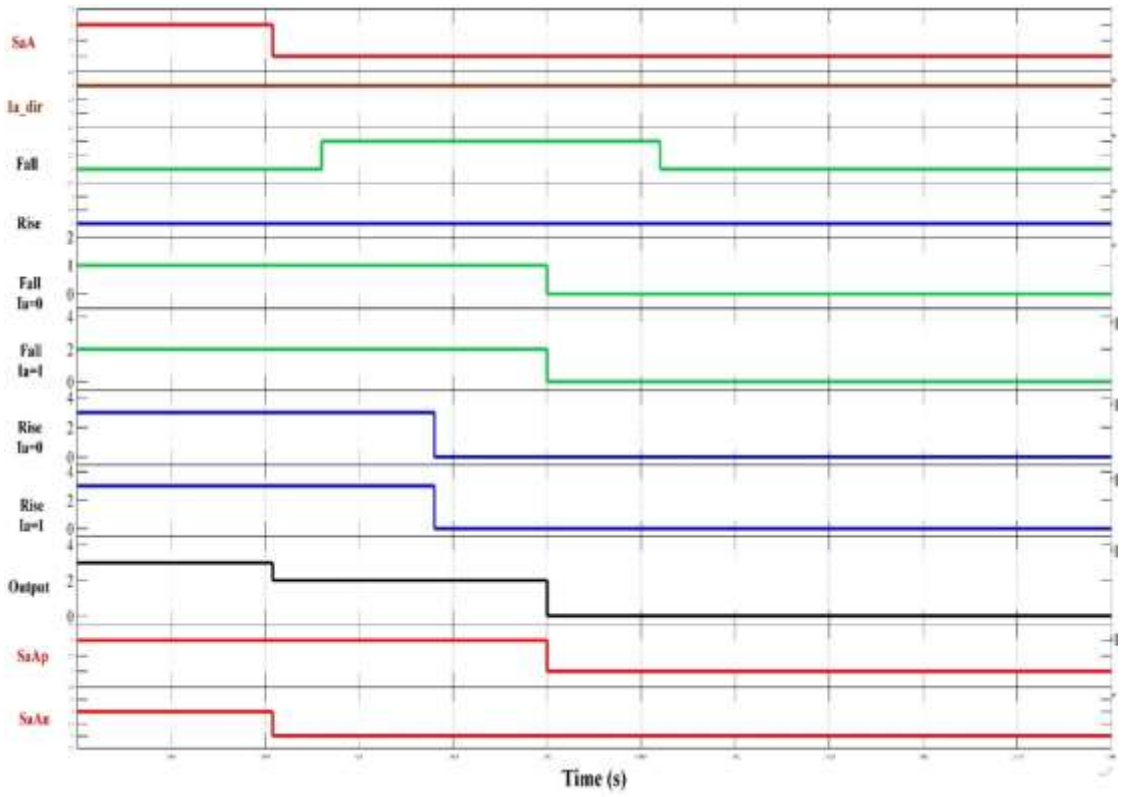


Figure 5.48 Pulses of switch SaA for a falling edge with positive current direction

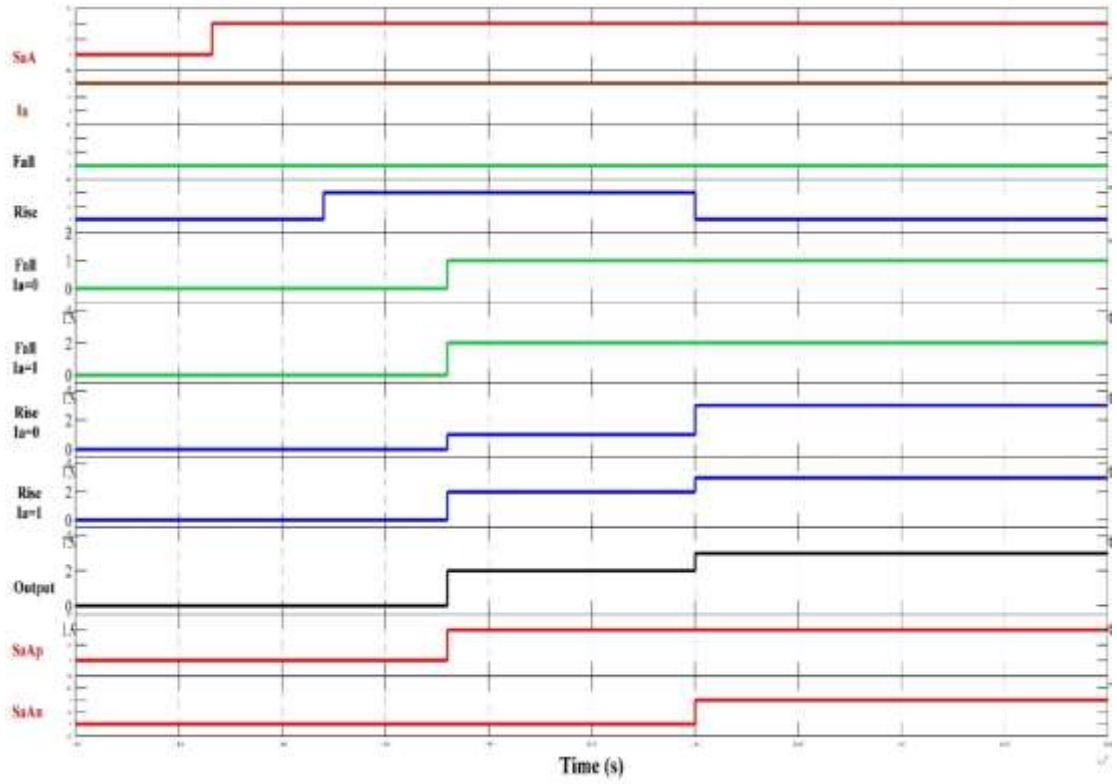


Figure 5.49 Pulses of switch SaA when a falling edge occurs with positive current

Until now, the generation of pulses for one switch alone has been discussed. The same applies for all the other eight switch modules. The complete four-step commutation module is shown in Figure 5.50.

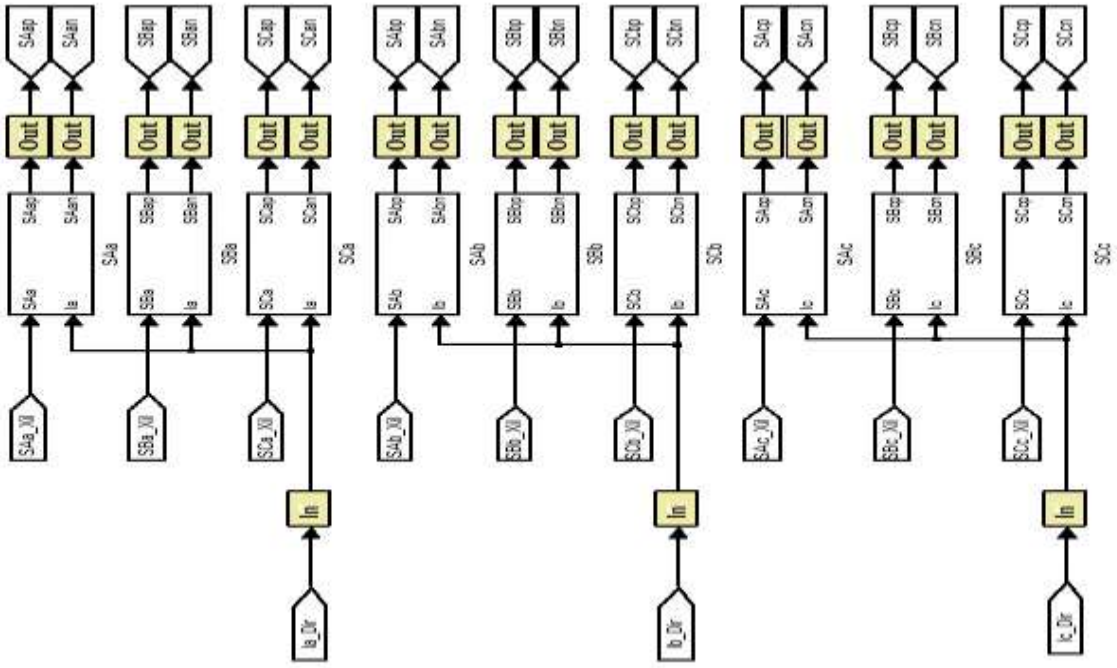


Figure 5.50 Four-step commutation for the nine bi-directional switches

The final pulses of the phase ‘A’ switches for a positive and negative phase ‘A’ current are shown in Figures 5.51 and 5.52 respectively.

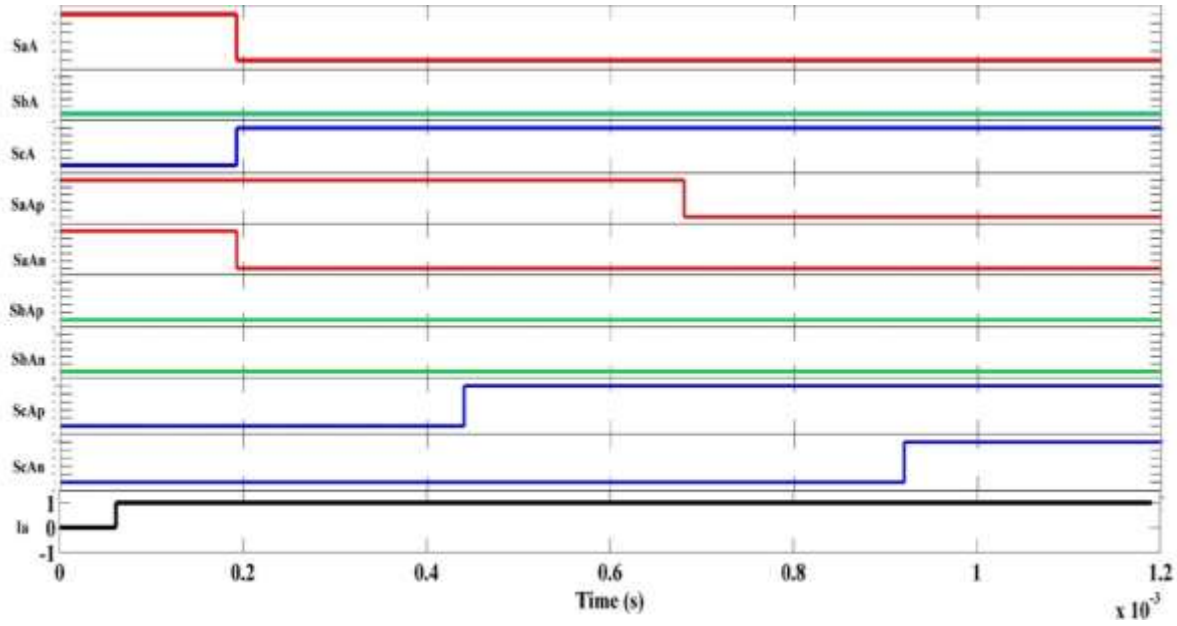


Figure 5.51 Final pulses to switches connected to load phase ‘A’ when current is positive

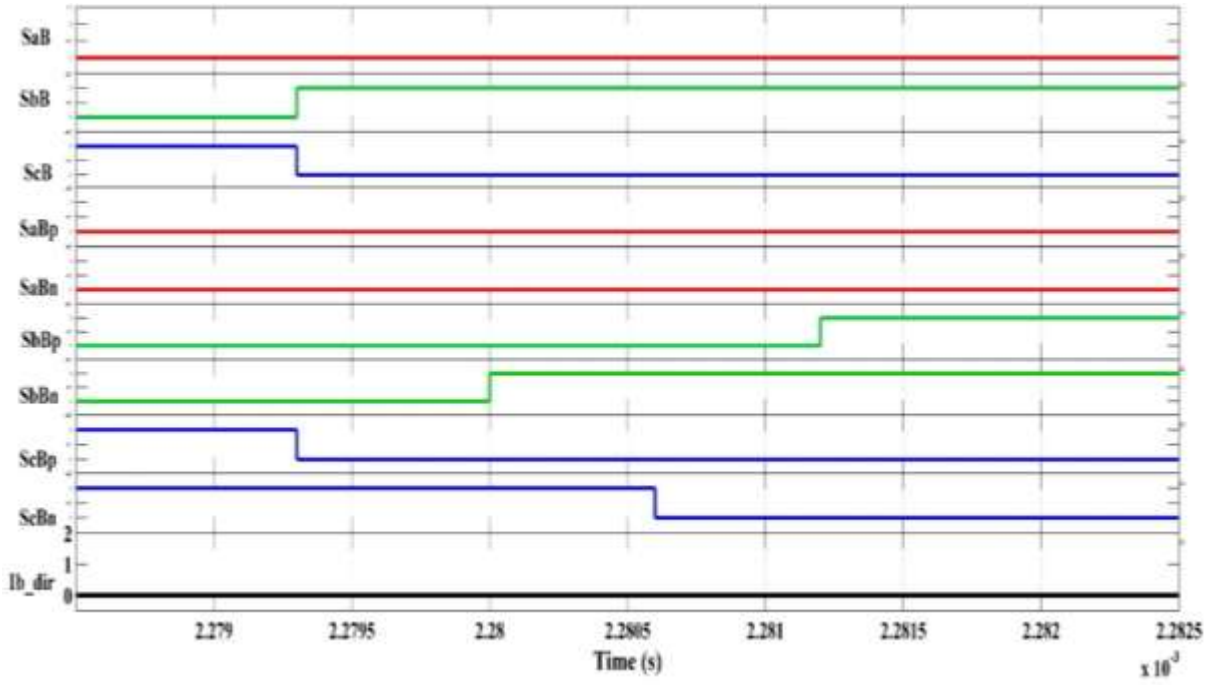


Figure 5.52 Pulses to switches connected to load phase ‘A’ when current is negative

Hence, the four-step commutation has been implemented in Xilinx and the VHDL code was generated successfully with System Generator.

CHAPTER 6

IMPLEMENTING ROTOR SIDE CONTROLLER FOR DFIG USING MATLAB/XILINX

6.1 IMPLEMENTING PI CONTROLLERS IN MATLAB/XILINX

The PI controller consists of two essential units (i) the proportional and (ii) the integral with saturation unit. The proportional unit is designed by a simple gain amplifier with the tuned proportional gain value. The integral unit is designed with an integral gain amplifier, summer, delay unit and the sample time gain amplifier. Figure 6.1 shows the implementation of the PI controller. Figure 6.2 shows the saturation block designed using simple comparator blocks to limit the values of the controller within limits.

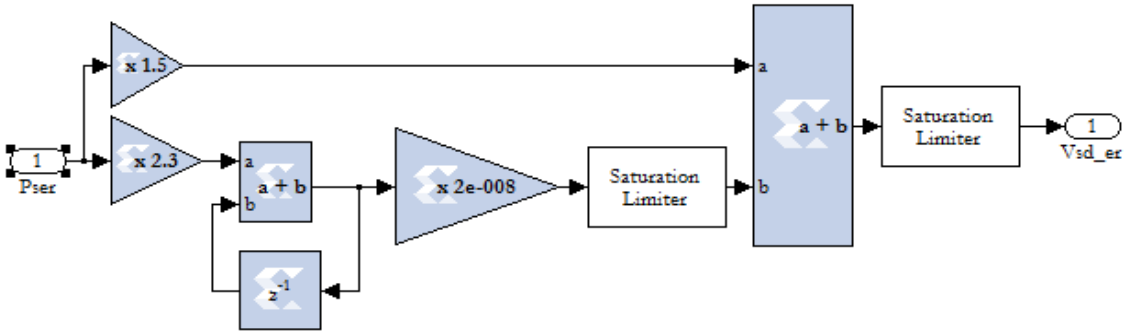


Figure 6.1 Matlab/Xilinx model for *the* PI controller implementation

The proportional gain, integral gain and saturation values that were tuned in the Matlab-Simulink environment are as follows: Kp = 1.5, Ki = 2.3 and saturation = 2.

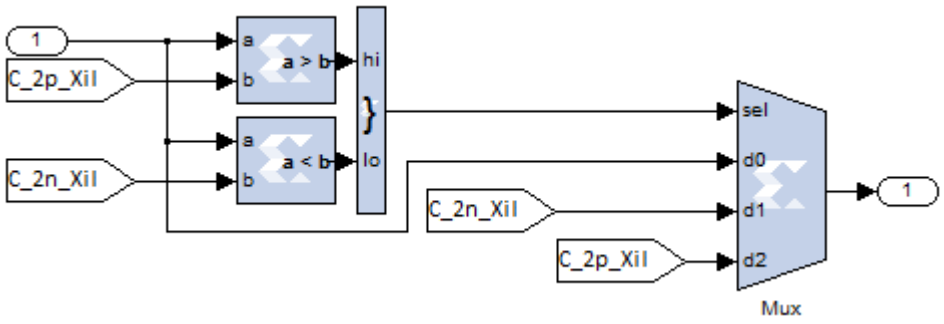


Figure 6.2 Matlab/Xilinx model of the saturation unit

6.2 IMPLEMENTING ACTIVE POWER AND REACTIVE POWER CONTROLLERS IN MATLAB/XILINX

Figure 6.3 gives the Xilinx model for the active power and reactive power controllers. The terms Ps_p_Xil and Qs_p_Xil refer to the actual active and reactive powers in p.u.

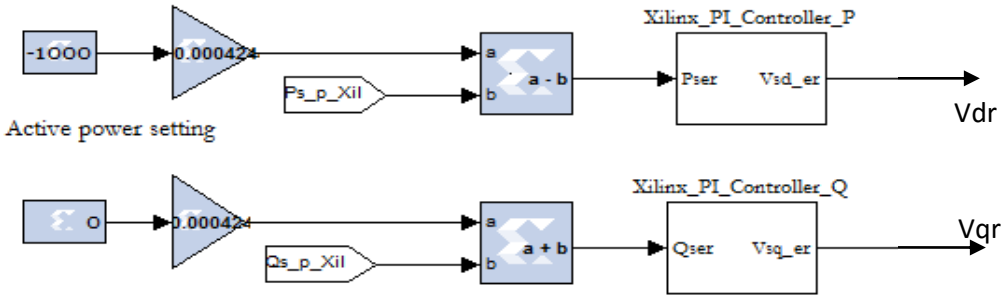


Figure 6.3 Matlab/Xilinx model of the active and reactive powers controller

6.2.1 Calculation of the Actual Real Power and Reactive Power

The actual real and reactive powers are calculated by converting the three-phase voltages and currents V_{abcs} and i_{abcs} into two-phase synchronously rotating voltages and currents, v_{ds}, v_{qs}, i_{ds}, and i_{qs} respectively.

Conversion of the three-phase voltages and currents into the two-phase synchronously rotating voltages: The three-phase voltages and currents are sensed using the voltage and current sensors

and given to the FPGA controller through the input ports. Figure 6.4 shows the Matlab/Xilinx model for obtaining the input from the voltage sensor for the FPGA controller. The terms Vsp_a, Vsp_b, Vsp_c denote the three-phase voltages in p.u. Figure 6.5 shows the Matlab/Xilinx model of getting the input from the current sensor to the FPGA controller. The terms Isp_a, Isp_b, Isp_c denote the three-phase currents in p.u.

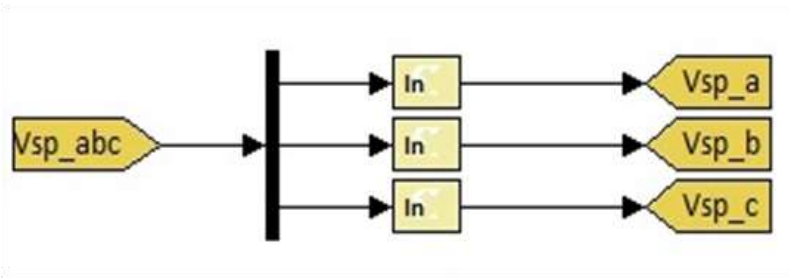


Figure 6.4 Matlab/Xilinx model of the stator voltages Vsp_abc

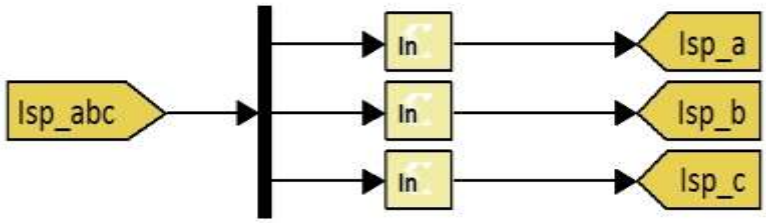


Figure.6.5 Matlab/Xilinx model of the stator currents Isp_abc

The angle theta is calculated in Matlab/Xilinx from the phase voltages in order to abc to dq transformation using Equations (4.1) and (4.2), as shown in Figure 6.6.

After calculating the angle theta, the voltages and the currents in three-phase are converted into the synchronously rotating dq voltages and currents by using Equations (4.1) and (4.3). This transformation equation involves many multipliers.

Use of Time Division Multiplexer (TDM) Block in Xilinx to reduce the use of Multipliers

The FPGA controller used in this project has a maximum of 20 multipliers. In order to reduce the use of multipliers, time division multiplexer is used. Figure 6.7 shows the use of TDM block in

order to perform abc transformation to dq transformations of voltages and currents using the time division multiplexing in Matlab/Xilinx.

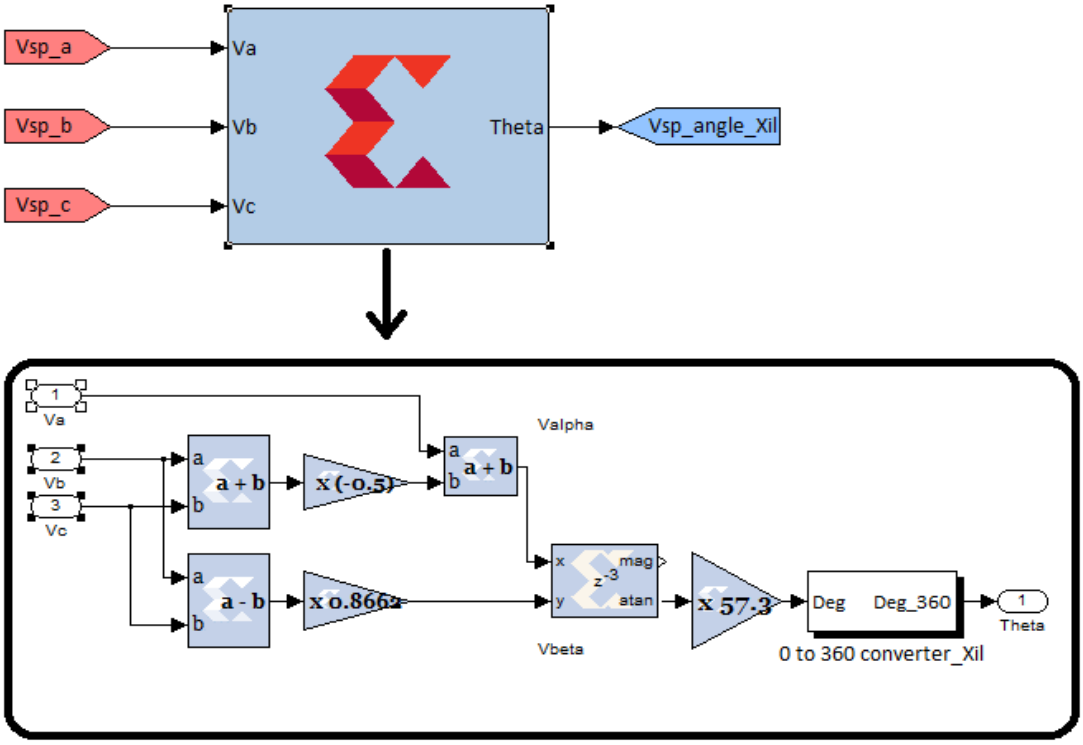


Figure 6.6 Matlab/Xilinx model for calculating theta

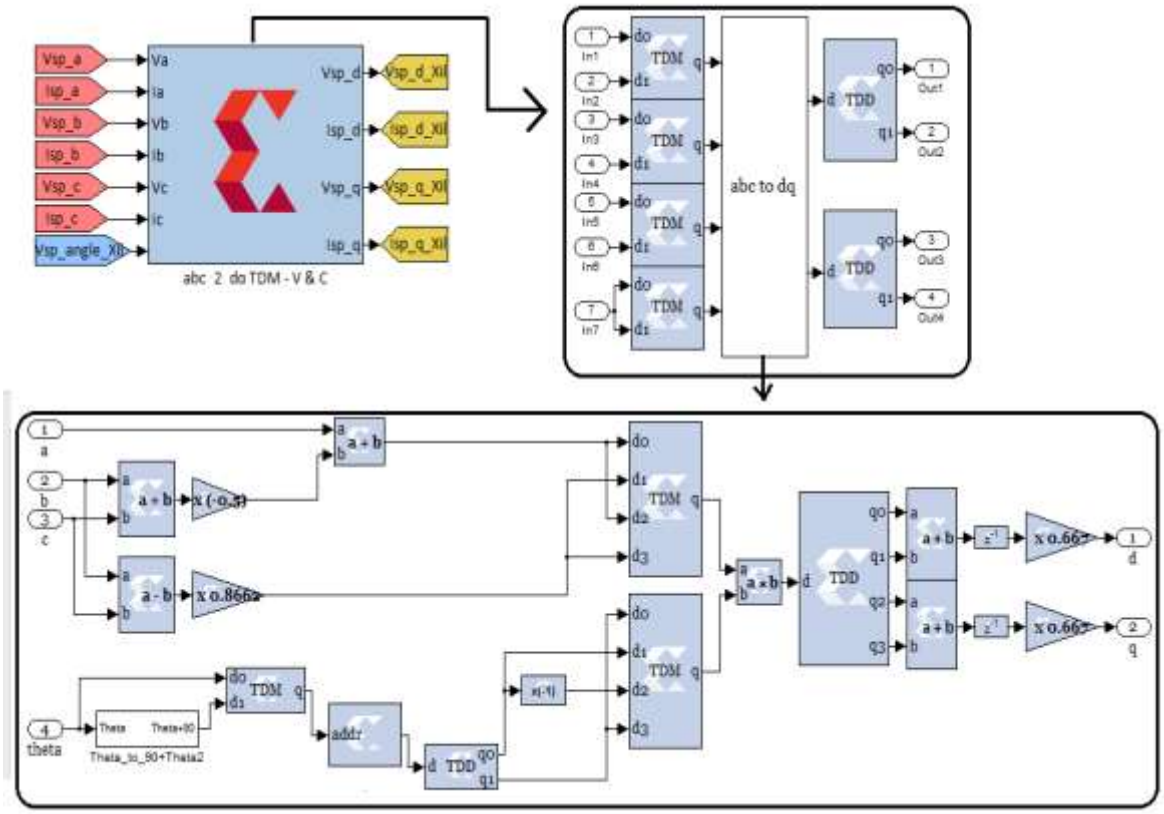


Figure 6.7 Transformation of the three-phase voltages and currents into two-phase synchronously rotating voltages and currents using the TDM

The next step is to calculate the actual real and reactive powers using Vsp_d_Xil, Vsp_q_Xil, Isp_d_Xil, and Isq_Xil, as shown in Figure 6.8.

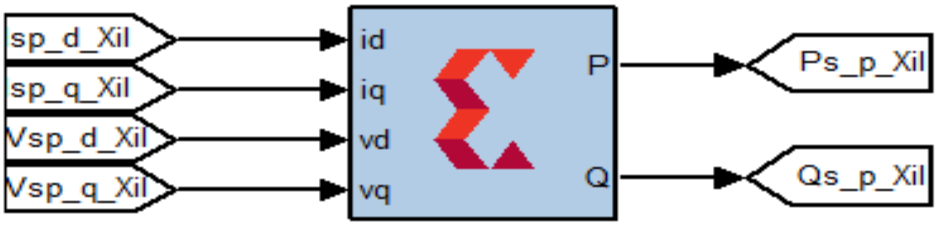


Figure 6.8 Sub-system to calculate the stator active power and reactive power in Matlab/Xilinx

Figure 6.9 shows the subsystem to calculate the stator active and reactive powers, which consist of two TDM blocks in order to reduce the use of multipliers.

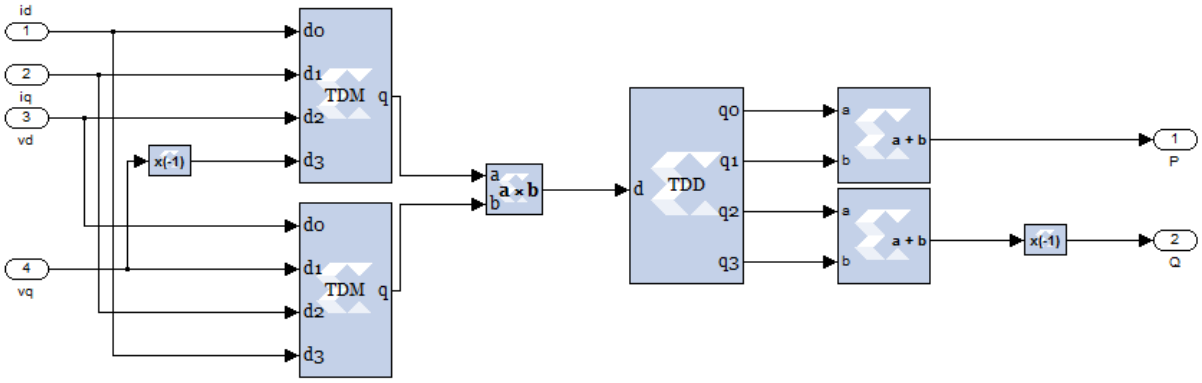


Figure 6.9 Use of TDM and TDD blocks to calculate the stator active and reactive powers

6.2.2 Generation of Reference Signals for the Matrix Converter

The stator active power Ps_p_Xil and reactive power Qs_p_Xil act as one of the inputs to the PI controller, as shown below in Figure 6.10.

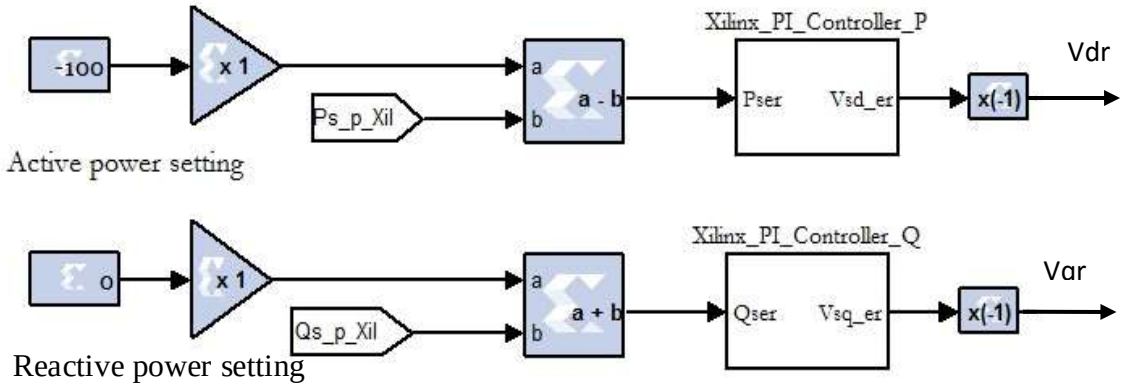


Figure 6.10 PI controller to control the stator active power and reactive power

The outputs of the active and reactive power controllers, V_{dr}* and V_{qr}*, act as one of the inputs to the transformation block. This clock transforms the two-phase synchronously rotating voltages into the three-phase rotating voltages V_{abcr}^{*}. In order to perform this transformation, we require the slip angle θ_r. The slip angle θ_r is calculated from the slip speed by computing the difference

between the stator speed ω_s (157.07 rad/s) and the rotor speed ω_r and multiplying it by the no. of pole pairs, as shown in Figure 6.11.

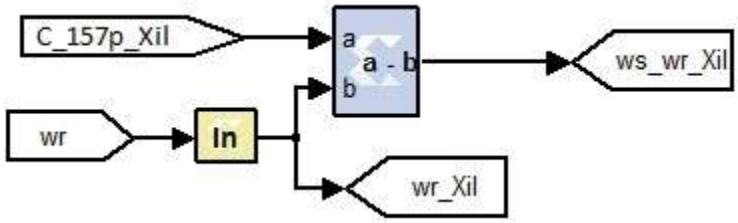


Figure 6.11 Calculation of the slip speed in Matlab/Xilinx using the stator and rotor speeds

6.2.3 Procedure to Integrate the Slip Speed for Obtaining the Slip Angle

After calculating the slip speed, ω_s-ω_r, the slip angle θ_r is calculated by integrating it. The integration operation in Matlab/Xilinx model is performed as follows. Figure 6.12 gives the Matlab/Xilinx model for the conversion of slip speed into θ_r.

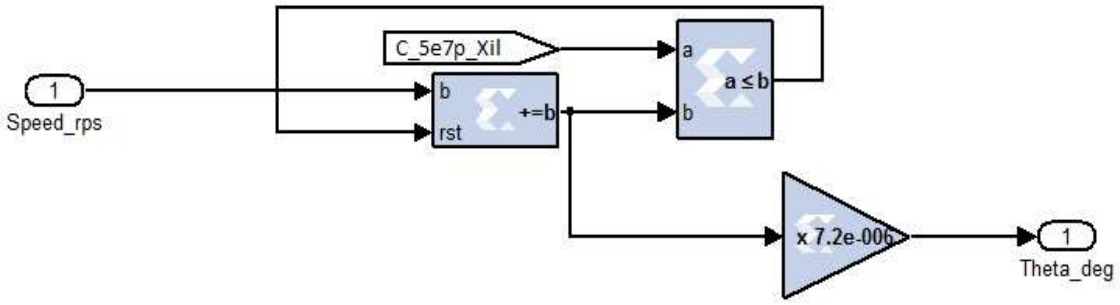


Figure 6.12 Matlab/Xilinx model for converting the slip speed to slip angle θr

The measured slip speed in rad/s is converted first to RPM and then to revolutions per second (RPS) by multiplying it by the factor 0.15922. The speed in RPS is stored in the accumulator b. Now the accumulator should reset for every 360°. In order to account for that, a constant 5×10^7, tagged as C_5e7_Xil, is compared with the slip speed in RPS and the output of the comparator is used to reset the accumulator b.

6.2.3.1 Determination of the Factor 5×10^7

The maximum count value in the counter is given by Equation (6.2).

$$\text{Count value} = \frac{\text{Required time period}}{\text{Explicit period}} \tag{6.1}$$

Suppose, if 25 RPS is the sensed speed, then as per the above the Equation, the count value is found to be 5×10^7. The calculation is shown in the Equation (6.2).

$$\text{count value} = \frac{0.04\times25}{20\times10^{-9}} = 5\times10^7 \tag{6.2}$$

Similarly, if the sensed speed is 100 RPS, then as per the Equation (6.2), the count value is again found to be 5×10^7. Equation (6.3) gives the calculations.

$$\text{count value} = \frac{0.01*100}{20\times10^{-9}} = 5\times10^7 \tag{6.3}$$

Hence, the factor 5×10^7 is constant for all speed measured in RPS, which can be proved from the above calculations. The output of the accumulator is normalized to 360^o by multiplying the accumulator output by $360^o/(5\times10^7)$, which is 7.2×10^{-6}.

Procedure to convert the slip angle θ_r into $\sin\theta_r$ and $\cos\theta_r$:

Figure 6.13 shows the Matlab/Xilinx model of this part. The slip angle θ_r is added to 90^0 in order to compute its cosine counterpart. The Matlab/Xilinx part present in the subsystem named as Theta_to_90+Theta, is given in Figure 6.14.

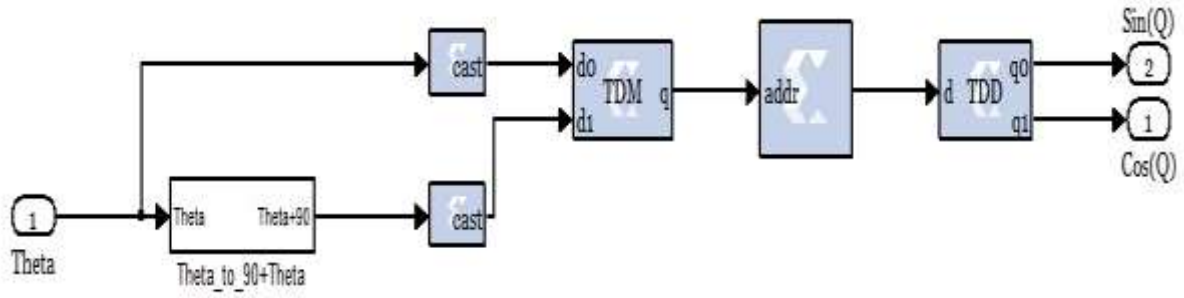


Figure 6.13 Matlab/Xilinx model to calculate $\sin\theta_r$ and $\cos\theta_r$ from slip angle θr

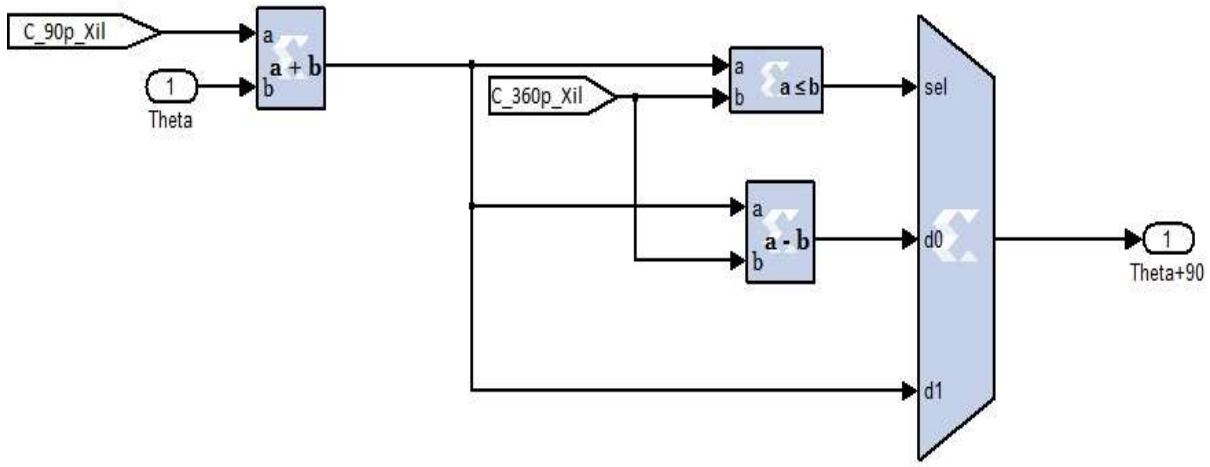


Figure 6.14 Conversion of theta to theta+90° in order to calculate $\cos\theta_r$

The constant 90 tagged as C_90p_Xil is added with the computed theta. If the value is within 360^0, we send the value, theta + 90^0. However, if the computed value is greater than 360^0, we send the value, theta+90^0-360^0. Figure 6.14 clearly explains these operations.

The next step is to send theta and theta+90^0 through the TDM block to the ROM block to calculate the $\sin\theta_r$ and $\cos\theta_r$. Figure 6.15 shows the ROM block parameters that are used to calculate the values of $\sin\theta_r$ and $\cos\theta_r$.

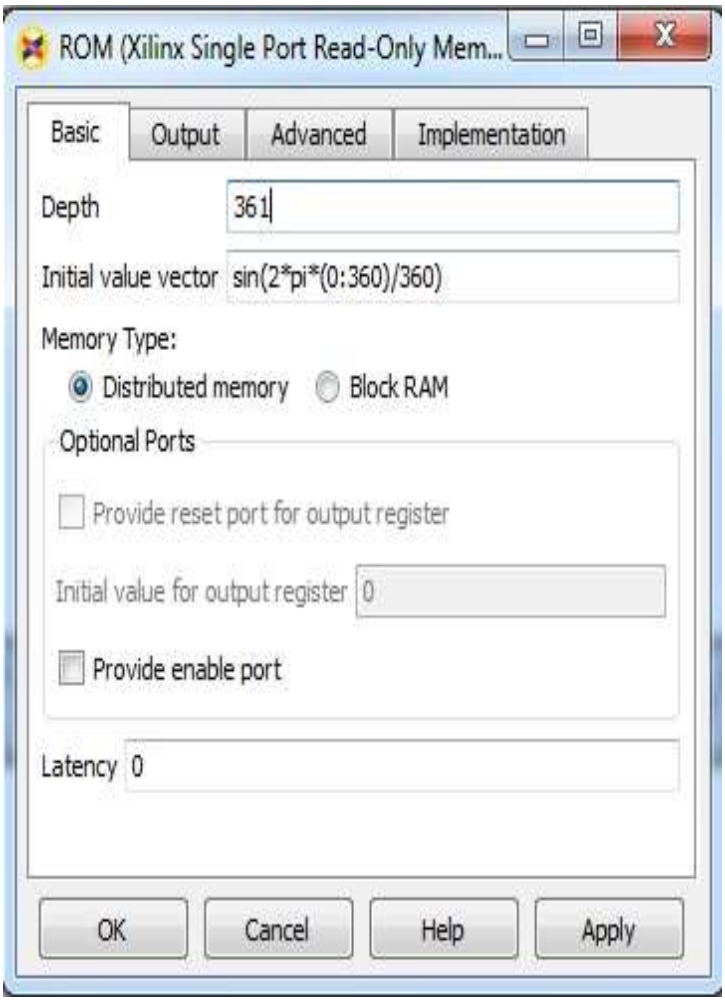


Figure 6.15 Parameters of the ROM Block to calculate $\sin\theta_r$ and $\cos\theta_r$

The output of the ROM block is connected to the TDD block in order to receive the $\sin\theta_r$ and $\cos\theta_r$ values in the same data line to ease further computation. The next step is to convert the two-phase rotating voltages in d-q frame to the two-phase stationary voltages in α-β frame and then to finally convert it to the three-phase voltages in the abc reference frame. Figure 6.16 depicts the Matlab/Xilinx model of the same.

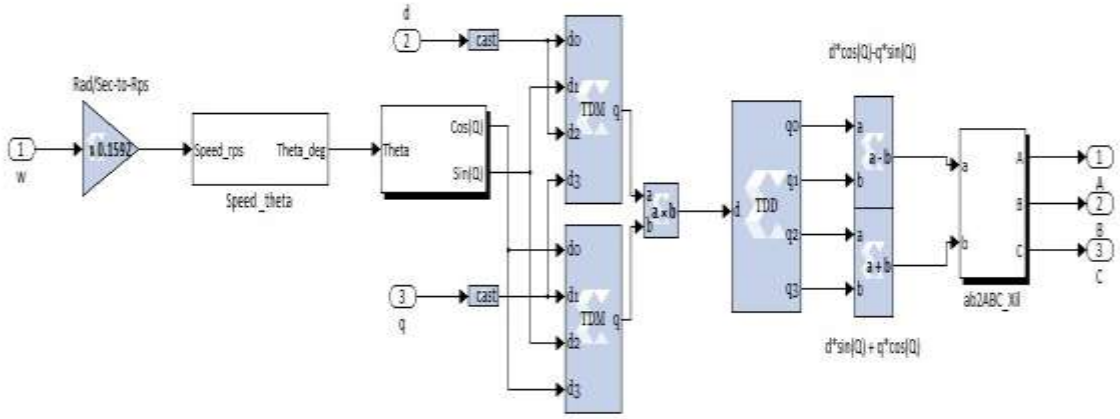


Figure 6.16 Matlab/Xilinx model to generate the reference voltages for the rotor side converter

Thus, the controller for the RSC is implemented in the Matlab/Xilinx model using the logic explained above. Figure 6.17 shows the complete Matlab/Xilinx model of the controller for the rotor side controller implemented in the DFIG machine connected to the matrix converter.

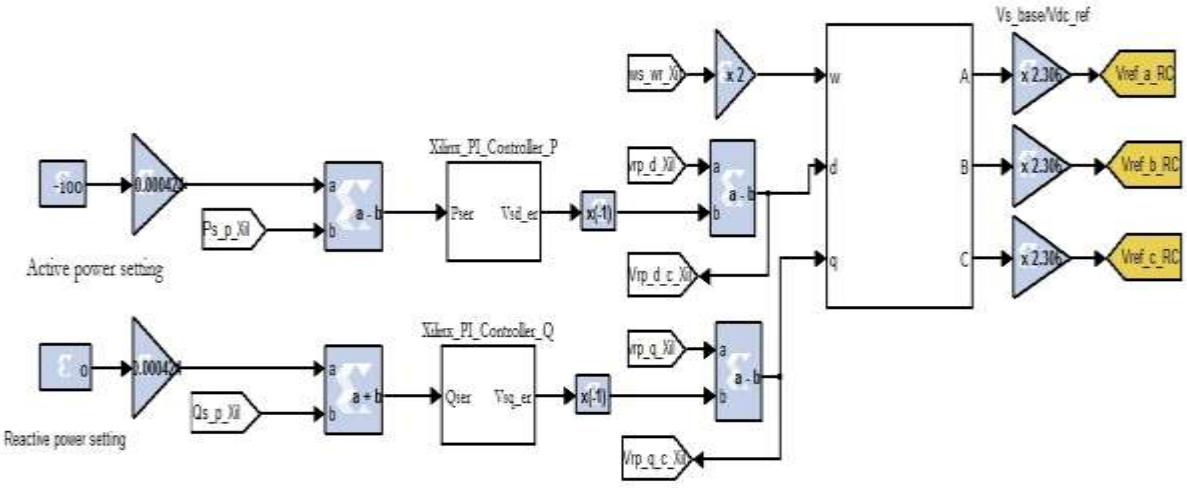


Figure 6.17 Active power and reactive power controllers and generation of the reference signals for the matrix converter fed DFIG based wind energy conversion system

CHAPTER 7

PMOD AD1 FOR DIGILENT NEXYS2 BOARD

7.1 INTRODUCTION TO PMOD AD1 BOARD

The Digilent Nexys2 board is based on Spartan 3E FPGA. There is no on-board ADC, but it can be purchased along with the board. Digilent has a range of PMOD ADCs that can be connected at any one of the PMOD ports on the Nexys2 board. There are four PMOD ports with 12 pins on each port. These PMOD ports are provided to add features like motor control, A/D conversion, D/A conversion, audio applications, and numerous sensor applications.

The voltage levels on the PMOD ports can be set to either 3.3 V or 5 V using the PMOD jumper connector. The input bus on the FPGA operates at 3.3 V or below 3.3 V, but only the PMOD pins have the option of operating at higher voltage. The output signals of most of the available sensors in the market are at 5 V, hence this facility is provided. Figure 7.1 shows how one can change the voltage level on the PMOD pin, and hence the power level.

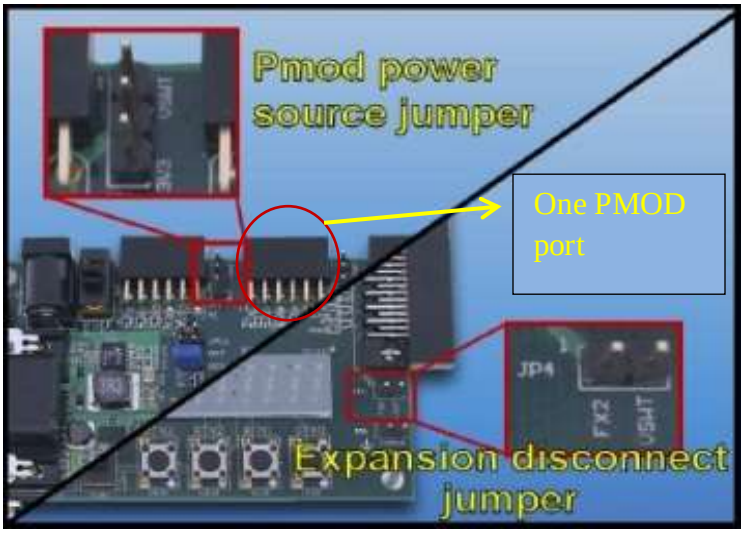


Figure 7.1 PMOD power source jumper

The jumper has three pins, the middle one is the common ground for the 3.3 V supply (3V3 pin) and the 5 V supply (VSW1 pin). For using the ADC, one has to first decide the voltage on these pins based on the voltage level of the ADC that performs the conversion. So, before we get into the design, it is recommended to thoroughly study the 'Digilent PMOD AD1 ADC Module Converter board' reference manual available in the Digilent website.

Figure 7.2 shows the PMOD AD1 module and its pin configuration. The board uses a 6-pin header connector, compatible with the PMOD port for various FPGA PMOD ports.

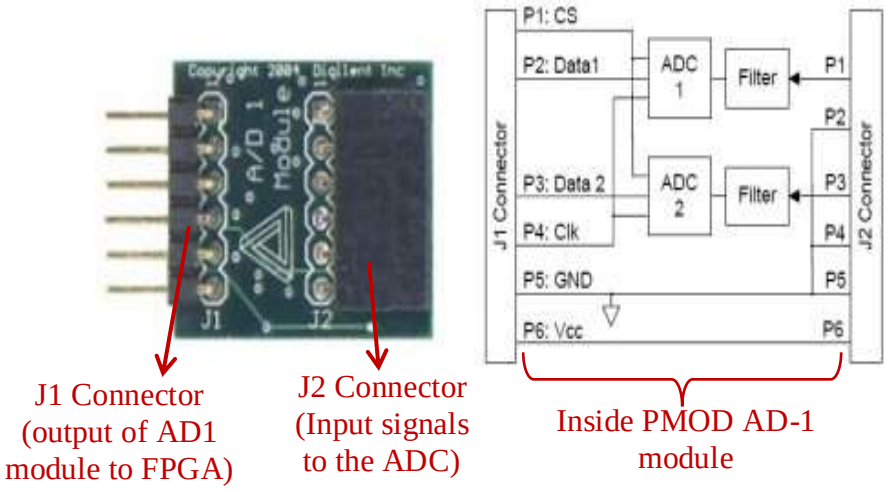


Figure 7.2 Digilent PMOD AD1 board and pin description

The PMOD AD1 board comprises of two ADCS7476MSPS 12-bit Analog to Digital Converter (ADC) chips. Hence, two analog data can be processed simultaneously. Table 7.1 shows the pin details of the PMOD AD1 module.

The two input data can be given to the module on the P1 and P3 pins respectively on the input side, and the corresponding digital data obtained on the DATA1 (P2) and DATA2 (P3) pins respectively. The power supply to the board is given to the P6 pin (V_{CC}), and its corresponding ground to pin P5 (GND). The three pins DATA1, DATA2, and VCC have a common GND point. The CS and CLK signals are generated by the user, and this is what we will be doing in the Xilinx model.

Table 7.1 Pin description of PMOD AD1 module

PIN NO.	DESCRIPTION
P1	Analog signal – 1.
P2	GND (common)
P3	Analog signal – 2.
P4	GND (common)
P5	GND (common)
P6	V_{CC} (not exceeding 3 V)
P1 (CS)	Tells the ADC when it has to start the conversion process, and when to finish the conversion process. (Generated by the user)
P2 (DATA1)	Digital data 1 pumped serially from the ADC
P3 (DATA2)	Digital data 2 pumped serially from the ADC
P4 (CLK)	The rate at which the ADC performs conversion process. (Generated by the user)
P5 (GND)	Ground
P6 (V_{CC})	Supply to PMOD AD-1 board. Can be taken from the FPGA itself or an external supply, but never both simultaneously. V_{CC} should never exceed 3.3 V. On the safe side, it should have a maximum value of 3V.

7.2 ANALOG TO DIGITAL CONVERSION PROCESS

The AD7476 is a 12-bit ADC that converts an analog signal to a 12-bit digital value in the range (0-4095). As the V_{CC} is 3.3 V, the chip gives digital value 4095 when 3.3 V is applied on the P1/P3 pins, and 0 when 0 V is applied. All other intermediate values of voltage are converted to the corresponding digital value based on Equation (7.1).

$$\text{Digital value} = \frac{\text{Input voltage}}{3.3\ \text{V}} \bullet 4095 \tag{7.1}$$

From the AD7476 datasheet, the essential parameters for achieving the analog to digital conversion are noted and are listed below. Figure 7.3 shows the timing waveforms ($\overline{CS}$, SCLK, SDATA).

1. The maximum rate at which one data is sampled (20 MHz): This is nothing but the frequency of ADC clock, SCLK, which the user sets.

2. Dead time (t_{quiet}): Minimum time required between bus relinquish and start of the next Conversion – 50 ns.

3. No. of clock cycles required for conversion – 16 SCLK cycles.

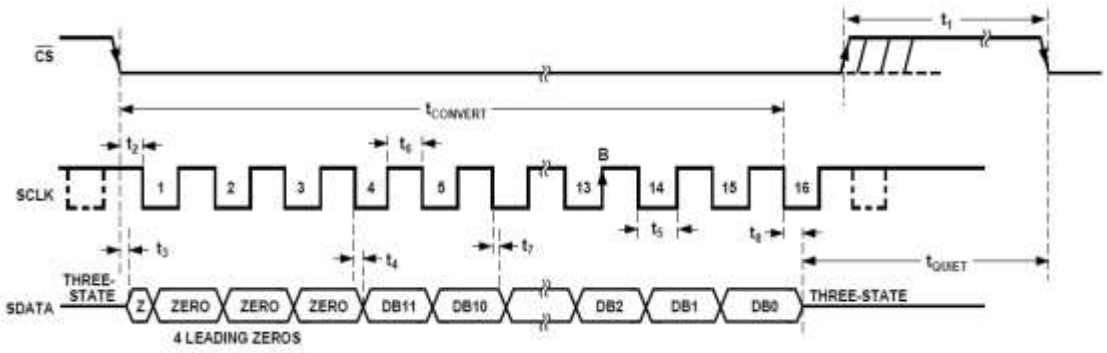


Figure **7**.3 AD7476 serial interface timing diagram

From Figure 7.3, it is can be understood that the ADC pumps the 12-bit digital data obtained in a serial fashion. It is our job to process the data bit by bit using a serial-to-parallel port to get the actual value. The datasheet carries the $\overline{CS}$, SCLK timing diagrams to specify how this serial-to-parallel process has to be carried out. We also see from Figure 7.3 that there are various time instants given: t_1 to t_7, $t_{CONVERT}$ and t_{QUIET}. From the list, $t_{CONVERT}$ = 16 SCLK cycles, and the minimum dead time t_{QUIET} = 50 ns.

7.3 THEORY OF OPERATION OF AD7476

There are two modes of operation of AD7476: normal and power-down modes. In the normal mode, the user need not worry about powering the ADC if it was powered down earlier. Hence, we go for the normal mode where the device is powered at all times, and hence faster throughput rates can be achieved.

7.3.1 Significance of $\overline{CS}$ and SCLK

Chip Select is an active low logic input. It provides the dual function of initiating conversions on the AD7476 and framing the serial data transfer. The SCLK is the serial clock and logic input and provides the serial clock for accessing data from the ADC.

Figure 3 shows the conversion initiated on the falling edge of $\overline{CS}$n. As said earlier, 16 SCLK cycles are required to complete the conversion process and access the conversion result. $\overline{CS}$ should not become high during these 16 SCLK cycles, i.e., during the conversion process. If it does, the conversion is terminated. Once a data transfer is complete, another conversion can be initiated after the quiet time (t_{QUIET}) has elapsed by bringing $\overline{CS}$ low.

The serial clock provides the conversion clock and controls the transfer of information from the ADC during conversion. With a very small SCLK period, the falling edge clocks out the data from the AD7476. If a slow SCLK is used, the data can be clocked out on the rising edge of the clock.

7.3.2 Process

A low $\overline{CS}$ signal initiates the data transfer and conversion process. At this instant, the AD7476 provides the first leading zero that is read by the FPGA PMOD port. By the time this clock cycle is complete, the second zero is also clocked out, i.e., only during the first SCLK cycle, two zeros are provided on the serial port. The reason is obvious: As soon as $\overline{CS}$ goes low, one zero is provided by the AD7476. At this instant, from Figure 7.3, it can be observed that SCLK is high. Hence, one zero has already been clocked out. This is called as the "tri-state" of the SDATA line. Hence, in the first clock cycle, two zeros are clocked out. In the subsequent two clock cycles, the remaining two zeros follow, one during each clock cycle.

During the fourth SCLK cycle, the MSB of the 12-bit data (D 11) is provided at the PMOD port of the FPGA. The remaining 11 bits are provided at the rate of one bit per clock cycle. after which the 12-bit digital data is provided serially every clock cycle. At the end of the 15^{th} cycle, the LSB (D 0) will be clocked out. Hence, during the 16^{th} cycle, the SCLK is made deliberately high to force the SDATA line to the "tri-state" again. Whatever data appear on the serial port in this clock cycle is discarded.

When the data is clocked out serially, a serial-to-parallel interface is provided by the user in the FPGA code to capture the data one by one, to obtain the full value. This is carried out either with the equidistant sampling rates ($\overline{CS}$) or using a timer along with interrupts to control the sampling rate of the ADC (non-uniform sampling).

7.4 DESIGN OF SYNCHRONISATION LOGIC CIRCUIT

The first step will be to set the SCLK frequency and the t_{QUIET} of the $\overline{CS}$ signal. The Nexys 2 board FPGA's clock frequency is 50 MHz. Using this as the base frequency, $\overline{CS}$ and SCLK are generated using the counters with explicit period setting. The counter's time-period has to be an integer multiple of the FPGA clock period (20 ns). Xilinx allows us to use counters with clock periods 40 ns, 60 ns, 80 ns, etc. Hence, 50 ns cannot be specified as the SCLK period in the Xilinx. In addition, it is always a good practice to operate any chip at a level tad higher than its operating limit, i.e., > 50 ns.

To be on the safe side, we have set t_{QUIET} as 360 ns and the SCLK period as 240 ns. Hence, Equation (7.2) gives the total time taken for 1 conversion.

$$\text{Time for 1 conversion cycle} = (16 * \text{SCLK period}) + t_{QUIET} \quad (7.2)$$

$$= (16 * 240 \text{ ns}) + 360 \text{ ns}$$

$$= 3.84 \text{ μs} + 360 \text{ ns} = 4.2 \text{ μs}.$$

Let us see how many times the ADC can sample a sine wave of 50 Hz using this conversion rate.

$$\text{No. of times an ADC can sample a 50 Hz signal} = \frac{0.02 \text{ s}}{4.2 \text{ μs}} = 4761.9 \approx 4762 \text{ samples}.$$

This is more than sufficient to accurately reconstruct the sine wave digitally. Hence, the conversion rate, we have chosen is reasonable and within the allowable limits.

Now, we shall draw the $\overline{CS}$ and SCLK signals for the time-period we have assumed. Only if we do so, it will be possible to generate these signals in XILINX. Figure 7.4 shows the timing diagram of the control signals of the ADC for a t_{QUIET} = 360 ns, and SCLK period = 240 ns. In addition, one can see how the signals are generated in Xilinx using four counters. Table 7.2 gives the list of counters used and their purpose.

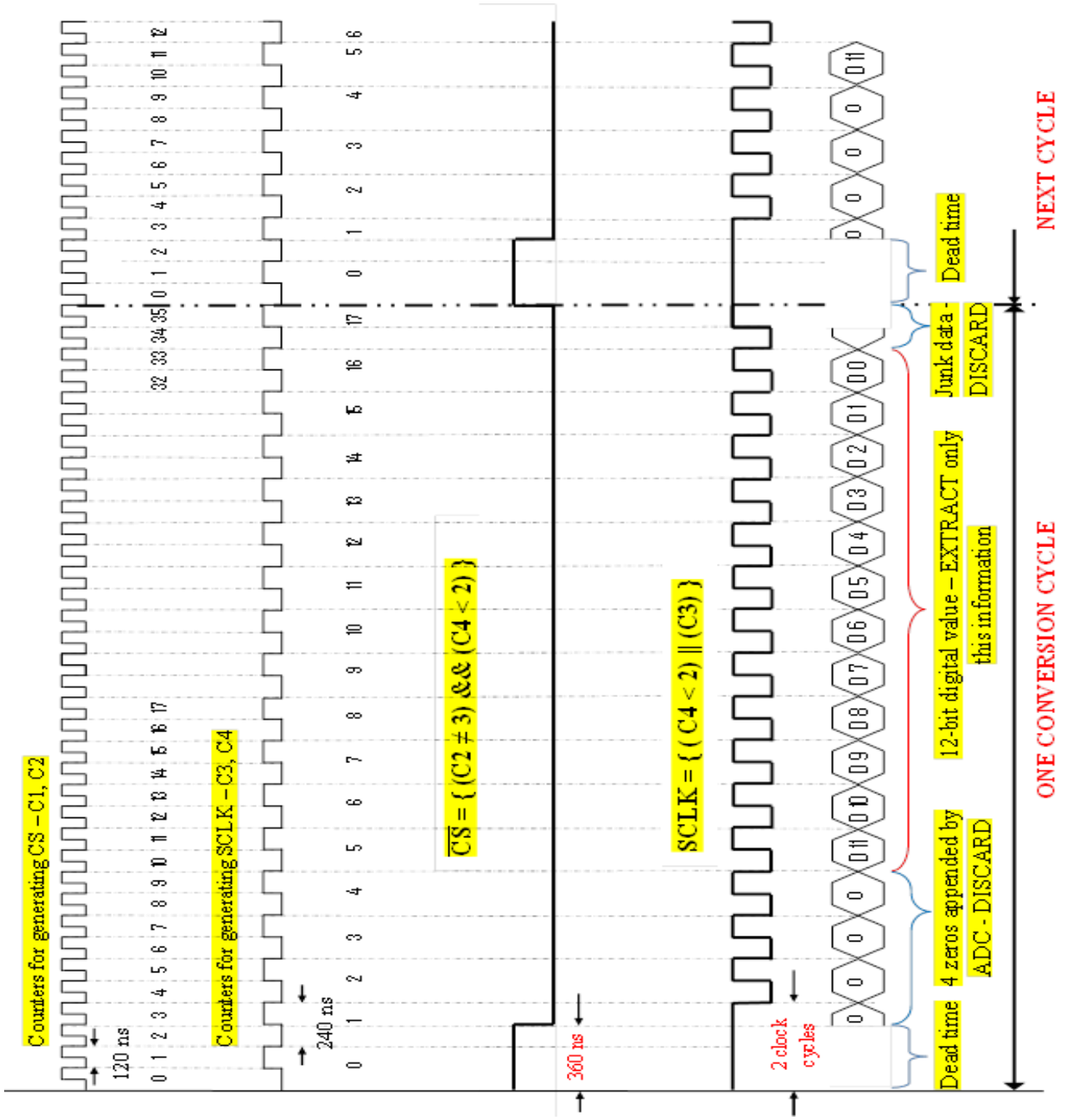


Figure 7.4 PMOD AD1 serial interface timing diagram with SCLK period of 240 ns

Table 7.2 Counters used to generate Chip Select and SCLK

Counter No.	TYPE	EXPLICIT PERIOD	DESCRIPTION
C1	One bit free-running counter. Initial value – 0	60 ns	› C1 & C2 are used to derive the dead time we have decided to set (360 ns) on $\overline{CS}$. › The output of C1 is the "Enable" line of C2. › Initially, C1 is set to "zero". Hence, the output is zero in the first 60 ns. C2 is not enabled, and output of the C 2 is also zero › In the next 60 ns, when C1 counts to "1", its output is "1", and hence, C2 is enabled and counts to "one". Output of C2 becomes "one". › The next instant of C1 being high leads to C2 incrementing by one-step at a time, until C2 reaches 35. When the value in C2 reaches 35, it resets to zero, and the process repeats. › The reason for setting the maximum limit to 35 can be explained only after understanding how SCLK and SDATA work.
C2	Count-limited counter with max. value 35 and Enable line. Initial value - 0	120 ns	
C3	One-bit free-running counter Initial value - 0	120 ns	› C3 and C4 are analogous to C1 and C2 respectively, though the explicit periods and maximum count values are different. › C4 is set to count every 240 ns in order that the SCLK signal is generated with a time-period of 240 ns. This could have been done with just C4, but if one looks closely, C3 is needed to generate the low and high pulses of the SCLK. As SCLK is low for 120 ns and high for the remaining 120 ns, the time-period of C3 is set to 120 ns.
C4	Count-limited counter with max. value 17, and Enable line. Initial value - 0	240 ns	

$\overline{CS}$ has to be high for the first 360 ns, i.e., until C2 ≤ 2, and low thereafter. The instant when the $\overline{CS}$ goes "high" again is when the counter C4's value is 17, to indicate that data has been extracted. If we have the condition C2 ≤ 2 alone, that instant would be missed by 120 ns. Hence, the only signal that carries information about the instant of completion of data extraction is C4. When C4 completes two cycles, $\overline{CS}$ has to go high (at the completion of conversion part), but this does not hold true for starting the conversion. For the AD7476 to start conversion, $\overline{CS}$ should go low at the instant when C2 value is 2. Hence, the $\overline{CS}$ signal is generated using C2 and C4, as given in Equation (7.3).

$$\overline{CS} = (C2 \neq 3) \;\&\&\; (C4 < 2) \tag{7.3}$$

The SCLK signal is generated using counters C3 and C4. This is quite simple when compared to the $\overline{CS}$ signal. Until C4 completes two clock cycles (value = 1), SCLK is "high" at the start of conversion. When two clock cycles are completed, the clock for the AD7476 has to be generated with a time period of 240 ns. This information is carried by the counter C3, which is a one-bit counter with explicit time period 120 ns. Hence, every 120 ns, a one and a zero are generated alternatively. Once 18 clock cycles are complete, (C4 = 17) the SCLK has to go high, indicating that the conversion is complete. Hence, the conditions given by Equation (7.4) suffice to generate the SCLK. Figure 7.5 gives The Xilinx model for generating the Chip select and SCLK signals.

$$SCLK = (C4 < 2) \;||\; C3 \tag{7.3}$$

Hence, as long as C4 <2, SCLK will be high, indicating that the conversion should not be started as $\overline{CS}$ will be low. Once C4 < 2 becomes false, the clock signal for conversion is generated by passing C3. Once C4 reaches 17 and resets to zero, C4 <2 condition becomes true, and SCLK goes "high" again, indicating that conversion is over, and $\overline{CS}$ has to go high in order to provide the dead time before the start of the next conversion. Figures 7.6 and 7.7 show the waveforms of $\overline{CS}$ and SCLK signals, respectively.

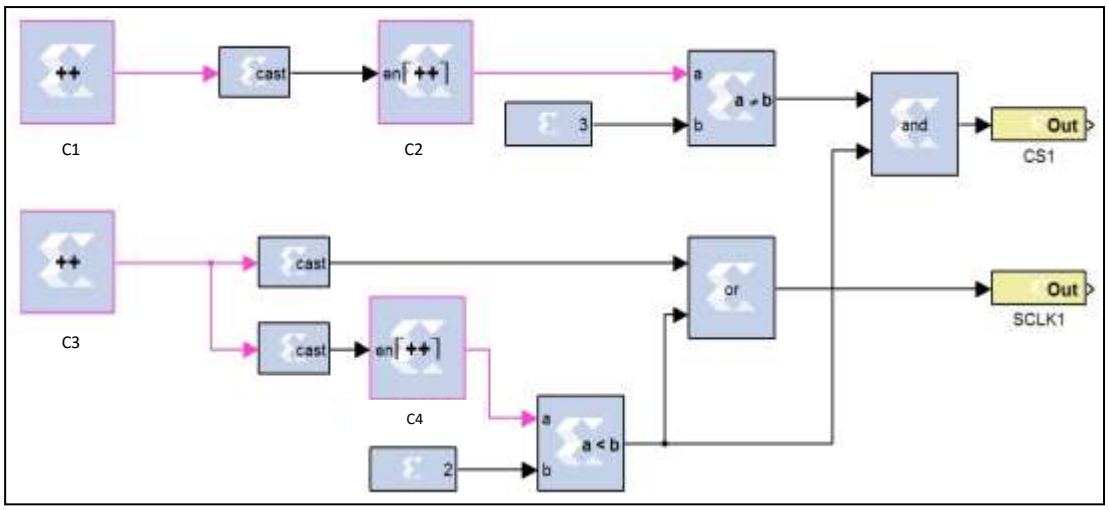


Figure 7.5 Xilinx model to generate Chip Select & SCLK

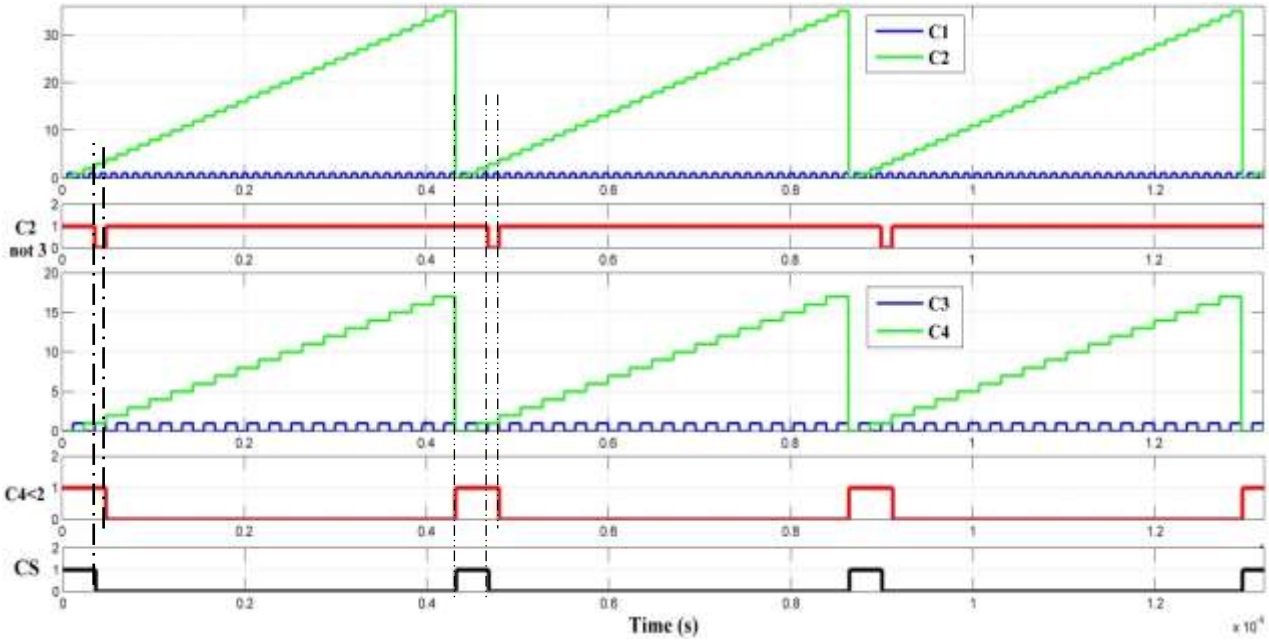


Figure 7.6 Generation of the Chip Select signal

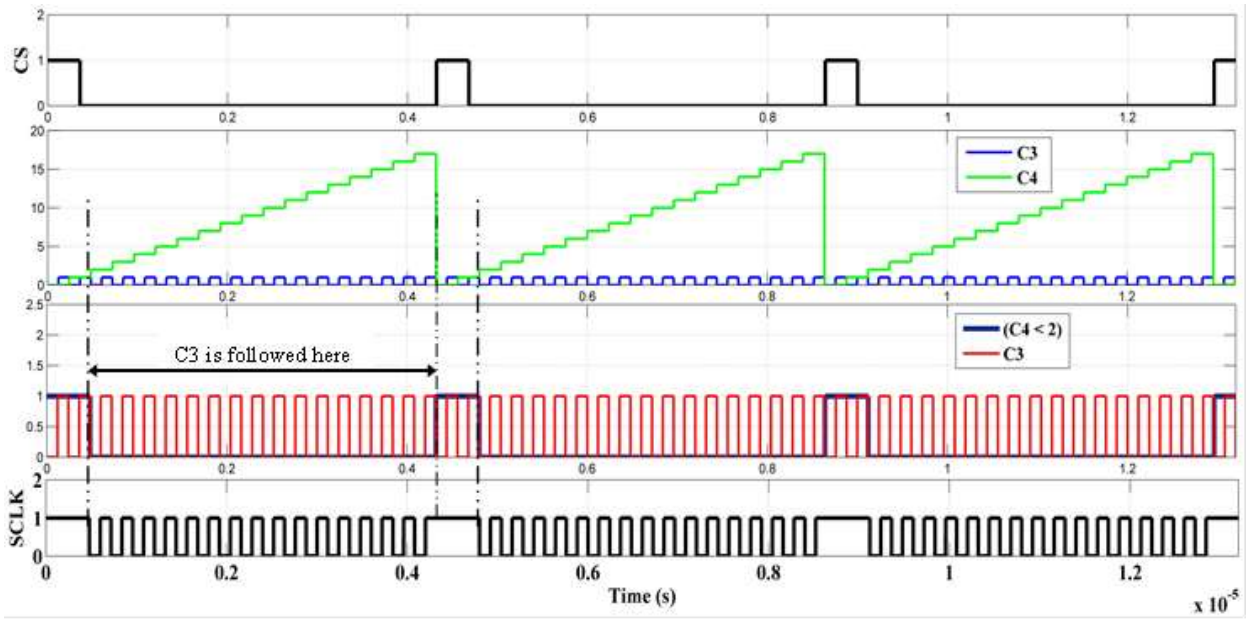


Figure 7.7 Generation of the SCLK

The serial data from the SDATA pin of the AD7476 is captured on every falling edge of the SCLK. The total number of bits generated by the ADC is 16 –> 4 leading zeros, and the 12-bit data. Nevertheless, we should remember that C4 is idled for the first two 240 ns. Hence, we need to assume that "18 bits" of the data are actually pumped out serially from the ADC for generating the SCLK and $\overline{CS}$ signals. This is the reason for setting the C4 counter limit to 17. As $\overline{CS}$ has to be low for another 120 ns before going high from the instant SCLK goes high, C2 counts one value extra, to reach 35. Hence, the maximum limit for C2 has been set to 35.

To extract the actual 12-bit data, a "serial-parallel" port available in the Xilinx block-set has been used to convert the incoming serial data to a parallel 12-bit output data. Figure 7.8 shows the serial parallel block in Xilinx with random SDATA input signals.

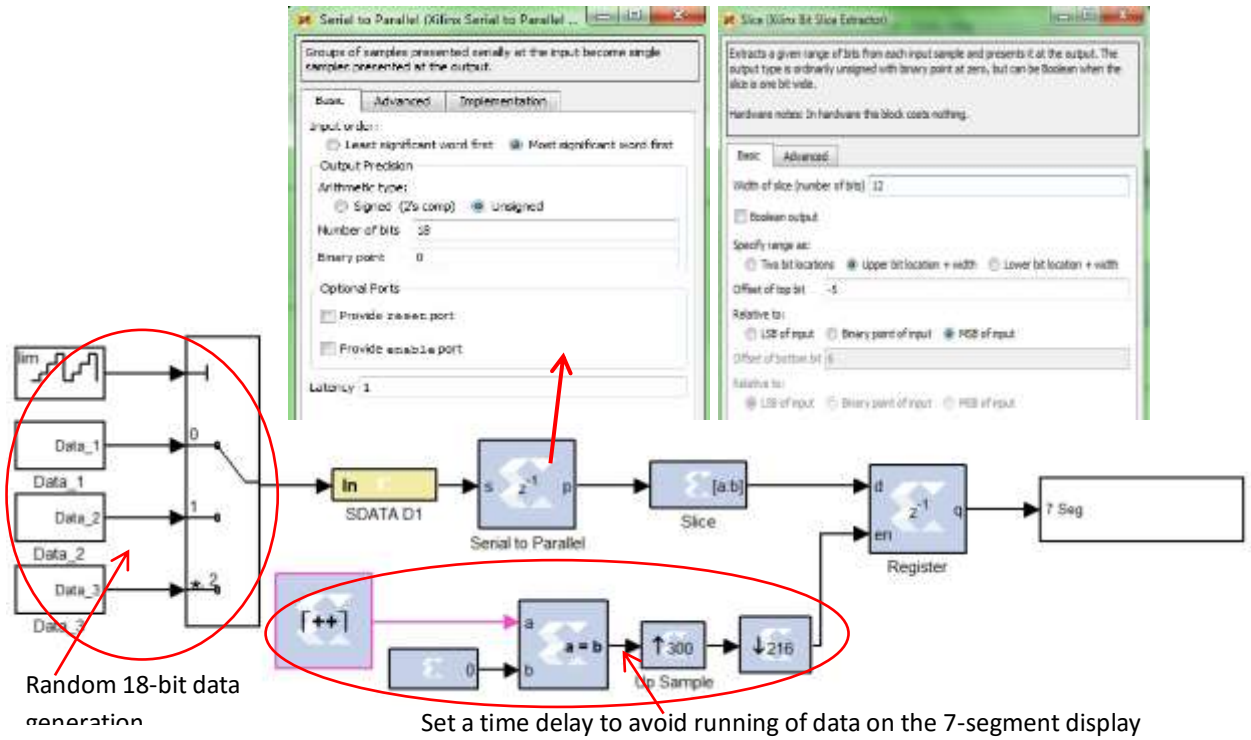


Figure 7.8 Serial to parallel block in Xilinx

The first two SCLK periods are idle and hold no information of the actual data. The following three clock cycles have the leading zeros, which are again meaningless. When the fifth clock cycle is over, the actual data comes in. Hence, the output of the serial-parallel port is sliced using the “Slice” block at position -5 with reference to the MSB to obtain the 12-bit data. One has to note that the last one bit is ignored inherently during the slice process.

It has to be noted that the data is processed at the rate of 240 ns. If the 7-segment display were to display the data from the serial-parallel port at such a rate, the last two digits of the data could be displayed due to the fast turn-on and turn-off of the segments. Hence, we have used a register to hold the data for half a second, so that all digits of the data can be seen clearly.

To set the time period for the hold action, a counter is used with a count period of 240 ns, and the maximum limit of 2083333. Whenever the counter resets to zero, the register is enabled. When the register receives the enable signal, it reads the data on its data line, and holds it until it

receives the next enable line (after 0.5 s). Figure 7.9 shows the operation of the serial-parallel port for the settings in Figure 7.8.

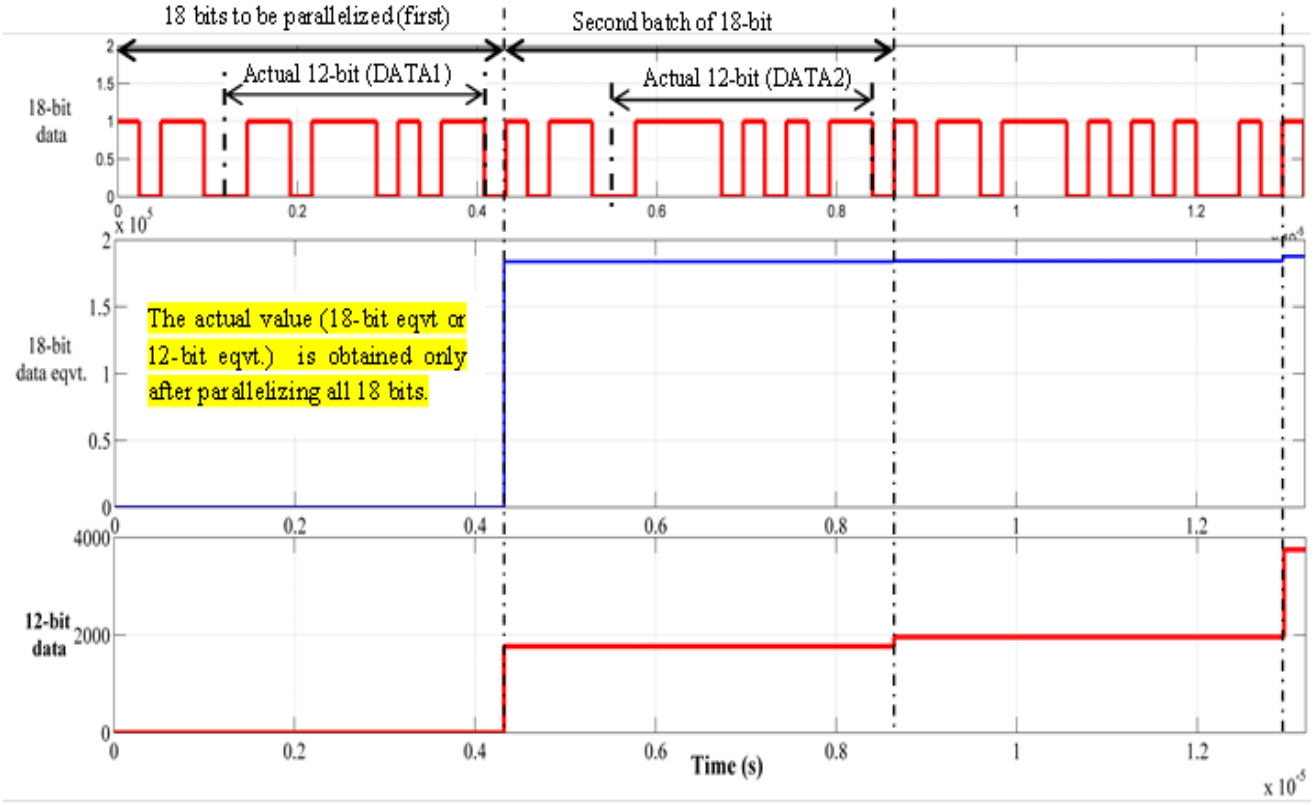


Figure 7.9 Working of serial-parallel block

We have given a continuous 18-bit input data stream to the port in order to understand the operation of the block. The first five bits and the last bit are eliminated, as they are not corresponding to the actual 12-bit data. From the sixth bit, the actual data is extracted using the "slice" block. The output of the block is the decimal equivalent of the 12-bit binary data. Figure 7.10 shows the three signals, Chip Select, SCLK and Output of serial-parallel port.

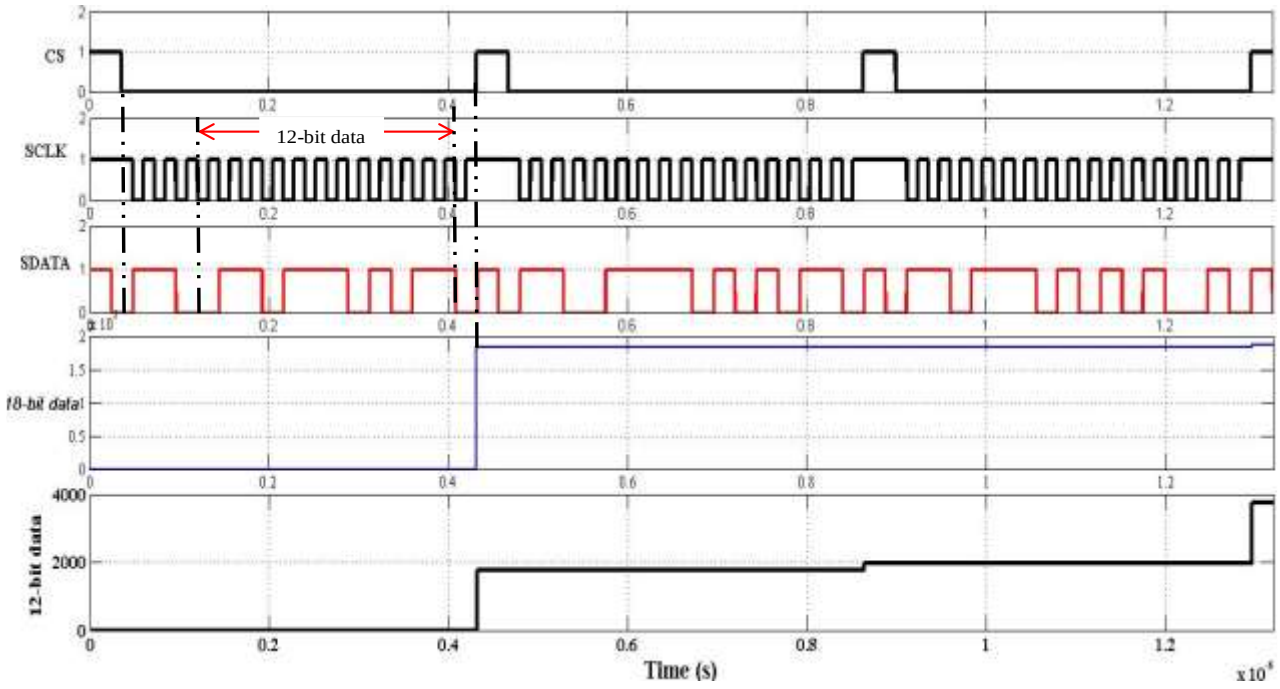


Figure7.10 Final Output

7.5 REAL TIME TESTING OF THE CODE

An analog signal (preferably DC to test the code) of magnitude not more than 3.3 V is given to the SDATA pin. One can perform this using a simple potential divider circuit. The ADC will convert the voltage on the SDATA pin with respect to its GND to a proportional value between 0-4095, in the binary form. Once the Chip Select is low, it sends four zeros followed by the actual data, one bit at a time to the FPGA. The SCLK starts clocking out these bits, one per clock cycle. The serial-parallel block receives these bits and holds them until 18 clock cycles are over (literally reading 18 bits). Once the 18 bits are read, the slice block extracts the required data and its value is obtained in decimal in the LED display. Another way to check if the code is working is to use the 8 LEDs and the 4 seven-segment displays to display the 12-bit data in binary form itself. To do this, one should slice bit-by-bit the extracted 12-bit data.

CHAPTER 8

ELIMINATION OF THE CURRENT AND VOLTAGE SENSORS USING A SIMPLE COMPARATOR CIRCUIT

8.1 INTRODUCTION

The most positive and the most negative of the three phase voltages are detected using the external hardware (with the Op-Amp circuitry). Each of these signals is then used in the FPGA controller to measure the period/frequency of the incoming AC voltage. The procedure for generating the reference current signals and its implementation is discussed in below sections.

8.2 PROPOSED METHOD TO ELIMINATE THE VOLTAGE SENSORS:

In this novel method, three comparators are placed, one for each phase of the input voltage. The most positive instant of the incoming 'R' phase and the most negative instant of the incoming 'Y' phase of the input voltages are measured for every 60°. This information is given to the FPGA controller to reconstruct the three-phase voltages, which is discussed in this chapter.

8.2.1 Logic to Extract the Information on Three-Phase Voltages for Every 60^0

Figure 8.1 shows the Matlab/Xilinx model for reconstructing the three-phase voltages from the logic signals. The steps involved extracting the three-phase voltages for every 60° is as follows:

Step 1: The three-phase currents are made to follow the three-phase voltages to maintain the power factor as unity.

Step 2: The most positive instant for R Phase and the most negative instant of Y Phase is obtained every 60^0. Figure 8.2 shows the Matlab model for the same.

This is implemented in hardware through a separate circuit, which uses LM 741 Op-amp circuits. The digital pulses that result at the output of the comparators are sent to the FPGA for generating the reference signals for the currents.

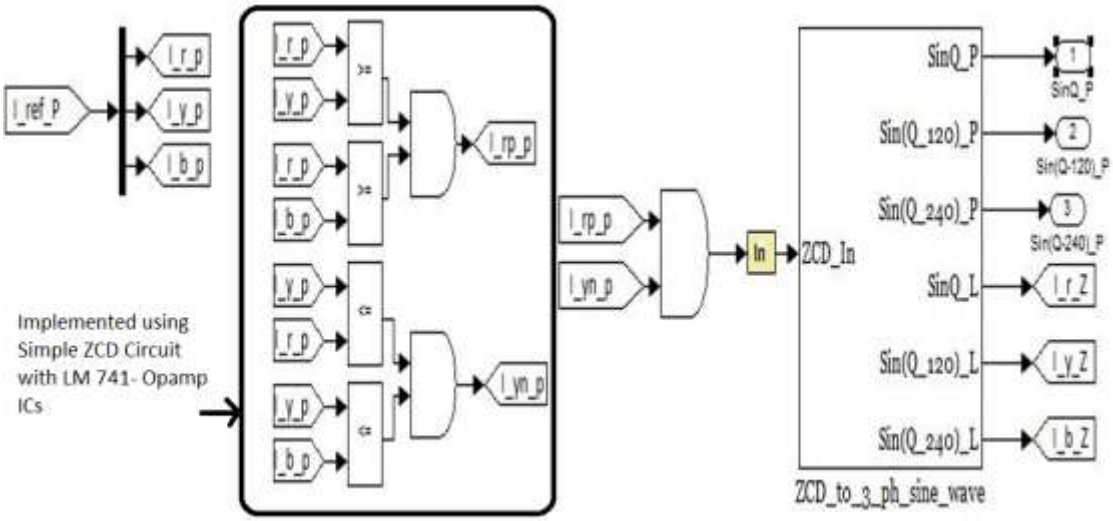


Figure 8.1 Matlab/Xilinx model to reconstruct the reference signals for the currens.t

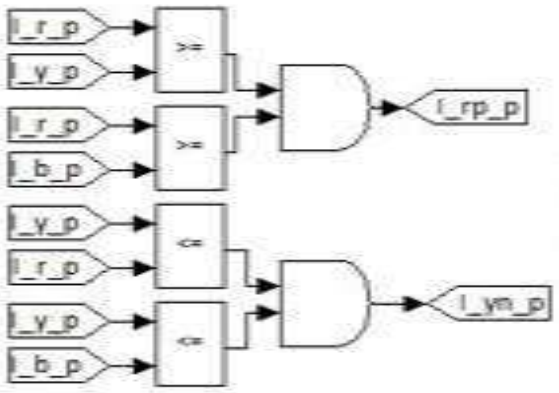


Figure 8.2 Matlab/Xilinx model to acquire the most positive and the most negative instants of the three-phase current signal

Step 3: The most positive instant for R phase and most negative instant for Y phase are observed, as shown in Figures 8.3 and 8.4.

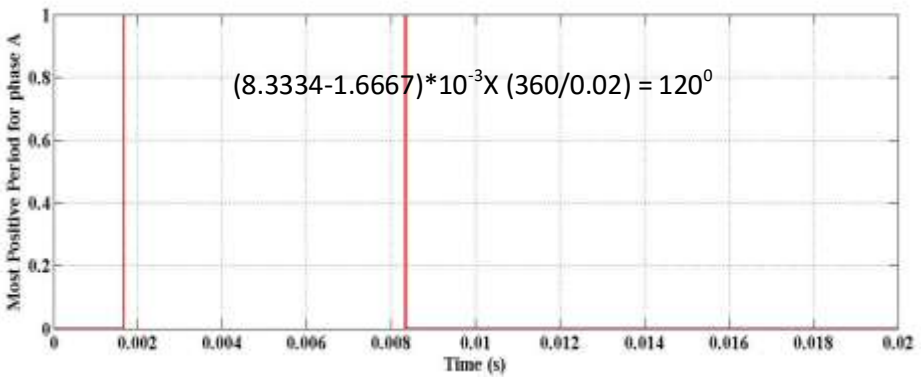


Figure 8.3 Most Positive Instant of R Phase

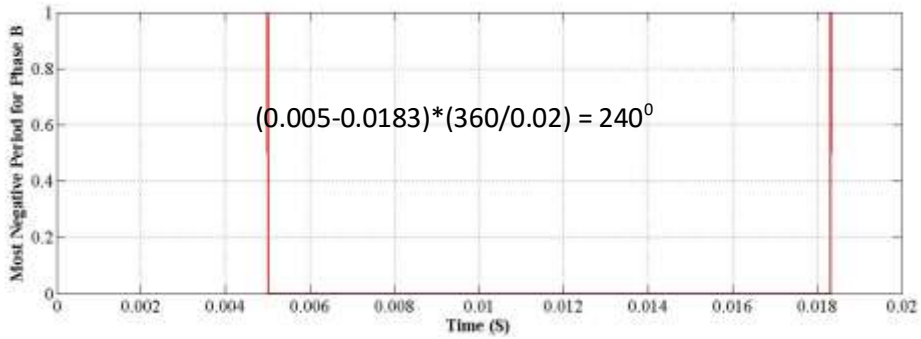


Figure 8.4 The most negative instant of the Y Phase

Step 4: These two signals are ANDed (the output of the AND signal,) as shown in Figure 8.5 and are used as the reference signal for the reconstruction of the three-phase reference current.

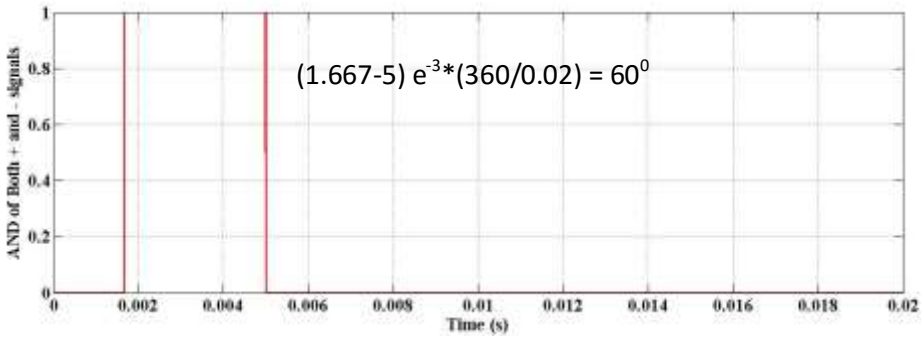


Figure 8.5 'AND' of the most positive and negative instant

Step 5: The information from the AND signal is captured in order to obtain the frequency and the angle (theta) information. The pulse obtained in Figure 8.5 is sent to a counter as shown in Figure 8.6. Figures 8.7 and 8.8 show the output of the counter and the inverted enable signal.

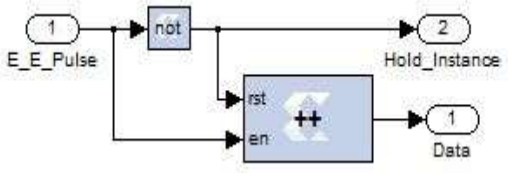


Figure 8.6 Matlab/Xilinx model to capture the Edge Pulse

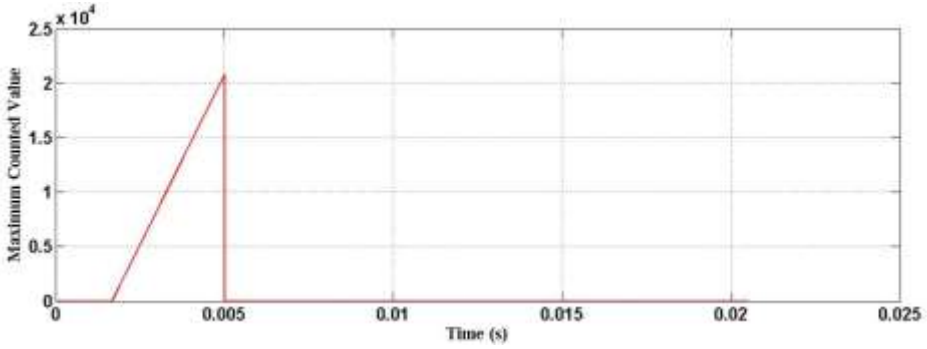


Figure 8.7 Maximum counter value

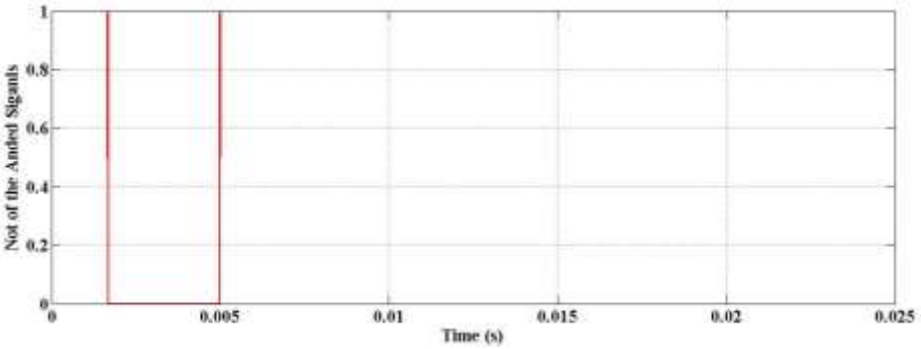


Figure 8.8 'AND' signal inverted

Step 6: The next step is to capture the maximum value in the counter by pushing it into a register, as shown in Figure 8.9. This is carried out by sending the counter maximum value to the

register by delaying it. The enable signal for the register is generated using the 'NOT'signal (as shown in the Figure 8.8). That is, the maximum value is sent out of the register at the rising edge of the NOT signal. Figure 8.9 shows the rising edge of the NOT signal. Figure 8.10 shows the method to detect the rising edge of the NOT signal.

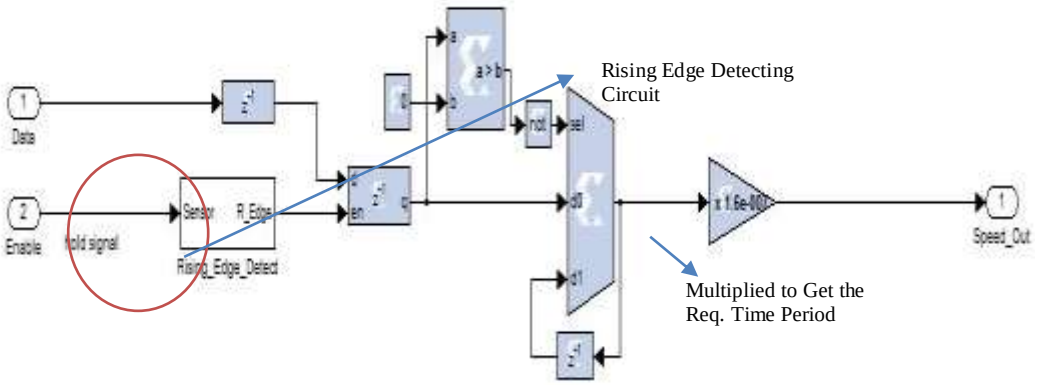


Figure 8.9 Matlab/Xilinx Model to calculate the Time Period of the Captured Signal

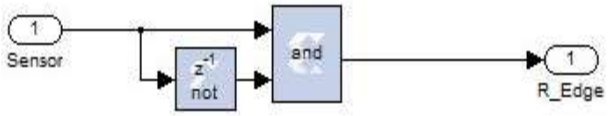


Figure 8.10 The rising edge detecting circuit

The NOT signal and the Delayed NOT is passed through the AND gate, which helps to detect the rising edge, as shown in Figure 8.11.

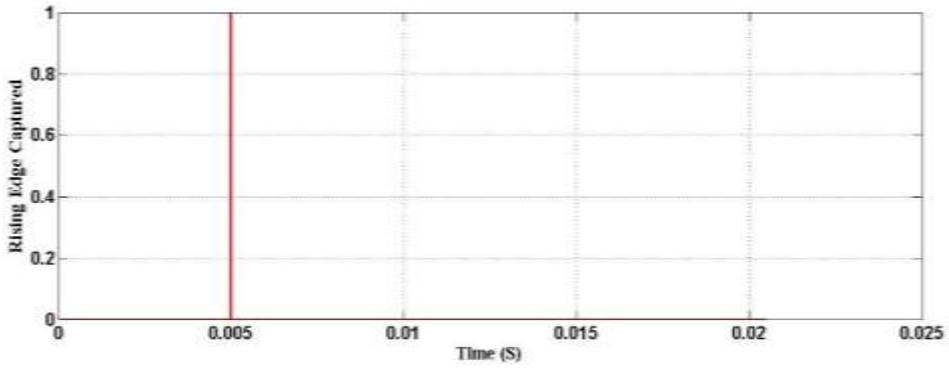


Figure 8.11 The captured rising edge

Step 7: The maximum value in the counter is pushed into the register when the rising edge is detected and is multiplied by a gain value of 1.67 $*10^{-7}$ (which is the clock period of the counter) to obtain the time-period of the signal. Figure 8.12 shows the signal after being multiplied by the explicit period.

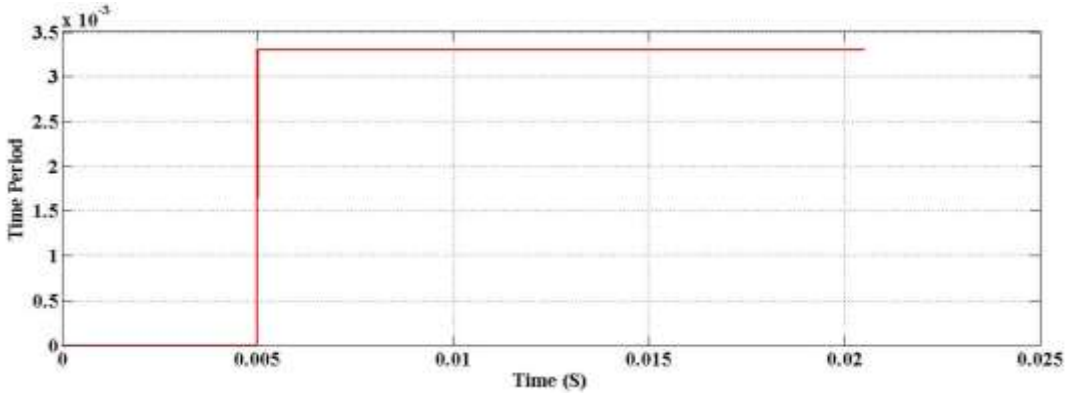


Figure 8.12 Calculated time-period for the signal from the comparator

Step 8: The signal obtained in Figure 8.12 is multiplied by the constant 6 as the counter counts for a sample-time equal to 60°, while the required time-period is for a full cycle of 360°. Figure 8.13 and 8.14 show the Matlab/Simulink model and the result after the multiplication, respectively.

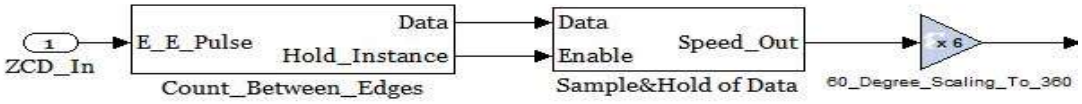


Figure 8.13 Matlab/Xilinx model for obtaining the time-period of the signal

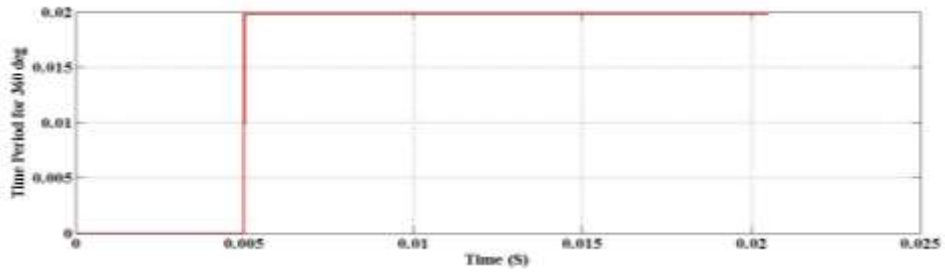


Figure 8.14 Calculated time-period (normalized 6*60° = 360°)

Step 9: Figure8.14 finally gives the total time-period of the three-phase currents. From this time-period, we calculate the frequency of the three-phase currents, which is the reciprocal of the time-period obtained (1/0.02s). Since division is not possible in the FPGA fixed point processor, it is carried out by repeated subtraction logic, as shown in Figure 8.15.

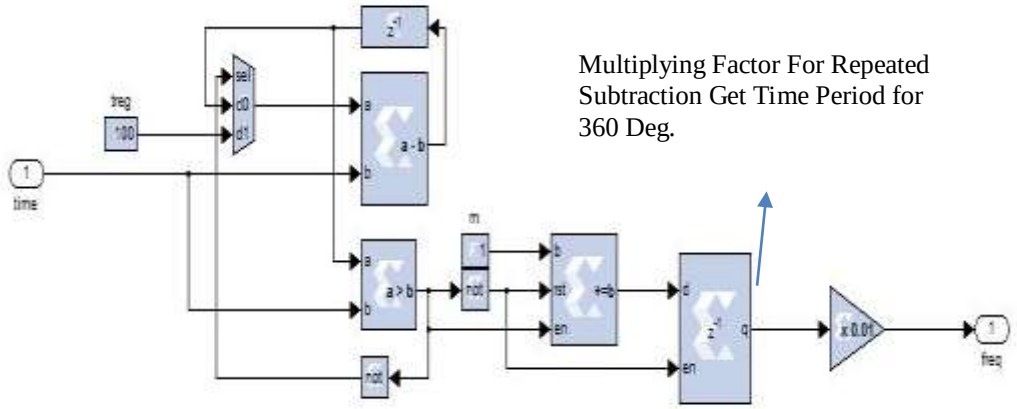


Figure 8.15 Matlab/Xilinx model to calculate the frequency of the signal from the calculated time-period using repeated subtraction

Example for understanding the repeated subtraction in FPGA The required time value to be inverted and a high arbitrary value (here it is chosen as 100) is taken as the inputs to the selector switch. At the first instant, the output of the comparator is zero and its NOT is 1. Hence, the d1 input of the multiplexer is selected. Te arbitrary value, 100, stored in the Treg (Temporary register) is selected at first. Consider now that the time value is 0.001 s and 100-0.001 = 99.999 is the result after the subtraction operation. Now this value 99.999 is compared with the time value, 0.001 or 0.002, the output of the comparator is 1 and its NOT value is 0, so the 'd0' input of the multiplexer will be selected and now the subtraction will be between 99.999 and 0.001. This way the repeated subtraction takes place until the comparator output becomes false.

As shown in the Figure 8.15, the output of the comparator acts as the enable signal for the accumulator. The accumulator gets incremented by 1 whenever the subtraction takes place. The value in the accumulator is pushed to the register at the end of the subtraction (the enable signal for this register is obtained from the reset signal of the accumulator, as shown in Figure 8.15)

Choosing the multiplication factor for repeated subtraction procedure:

$$\frac{\text{Temp. Register value, } 100}{\text{Required Time Period, } 0.02} * \text{Multiplying Factor} = \text{Required Frequency, } 50 \text{ Hz}$$

$$\therefore \text{Multiplying Factor} = 0.01$$

Figure 8.16 shows the output after the repeated subtraction and Figure 8.17 shows the value stored in the register.

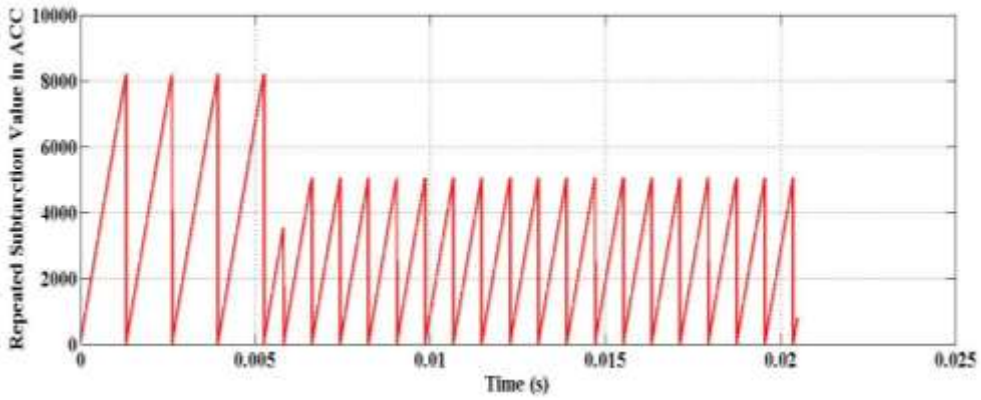


Figure 8.16 Results stored in the accumulator after every repeated subtraction

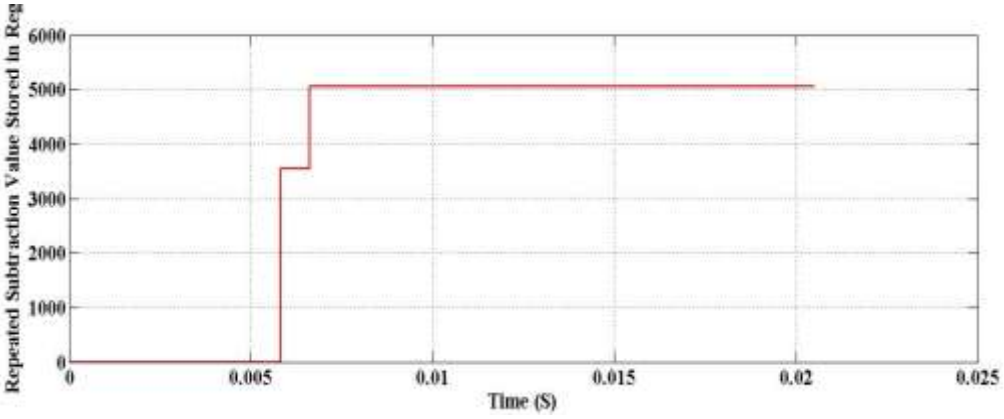


Figure 8.17 Repeated Subtraction Values Stored in a Register

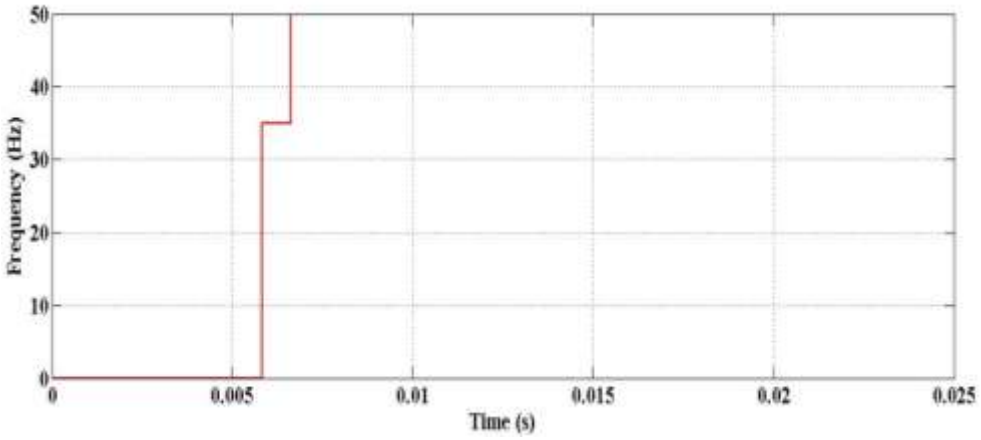


Figure 8.18 Calculated frequency of the input signals

Step 10: The next step is to extract the value of theta from the frequency information obtained from Figure 8.18. For this, the frequency signal is fed into an accumulator that performs the integration action, as shown in Figure 8.19.

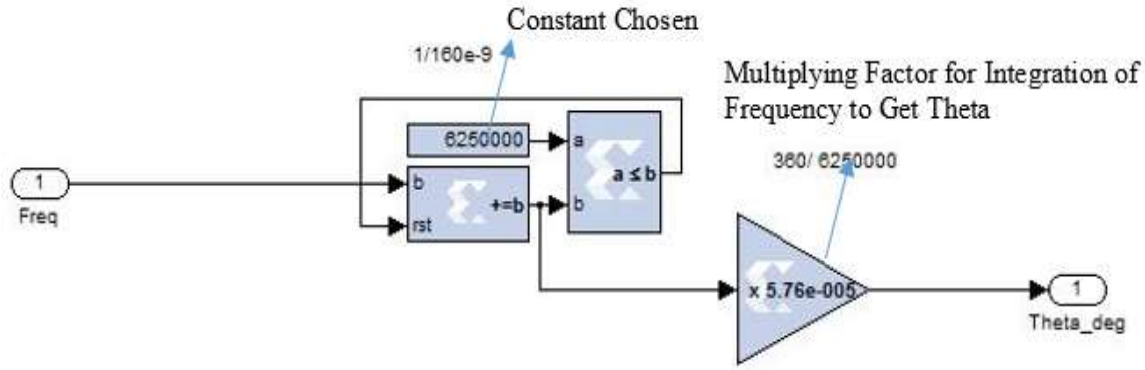


Figure 8.19 Matlab/Xilinx model to obtain theta from the frequency

(Note – The reason for choosing the constant as 625000, which is the 1/(Sample period of the accumulator. Note – Multiplying Factor chosen for the integration of the frequency to obtain theta is 360°/6250000.)

Step 11: This step is to generate theta for one of the phase with the lag correction (which is due to computation time i.e., 109°). Figure 8.20 shows the reconstruction of phase of the three-phase currents, which is used as the reference current signal for the rotor side DSVM controller.

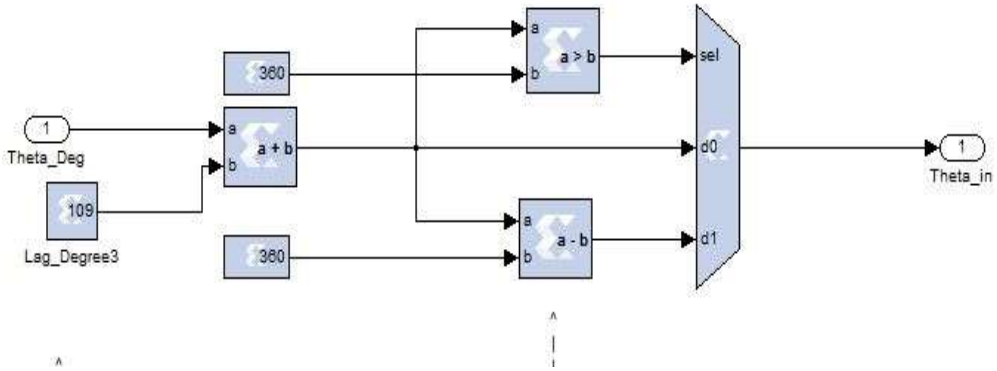


Figure 8.20 Matlab/Xilinx model for generating theta with the lag correction within the limit of 360°

Care has to be taken in Figure 8.20 to ensure that theta after lag correction should not exceed 360°. Figure 8.21 (a) shows the theta before lag correction. It was noted that the theta started at 0.0261s rather than 0.02s. Therefore, a lag correction of 109°. (Lag correction = [{0.0261-0.02}*{360/0.02}]) was added. It is also noted from Figure 8.21(b) that after the lag correction, the theta starts exactly at 0.02 s and finishes at 0.04 s.

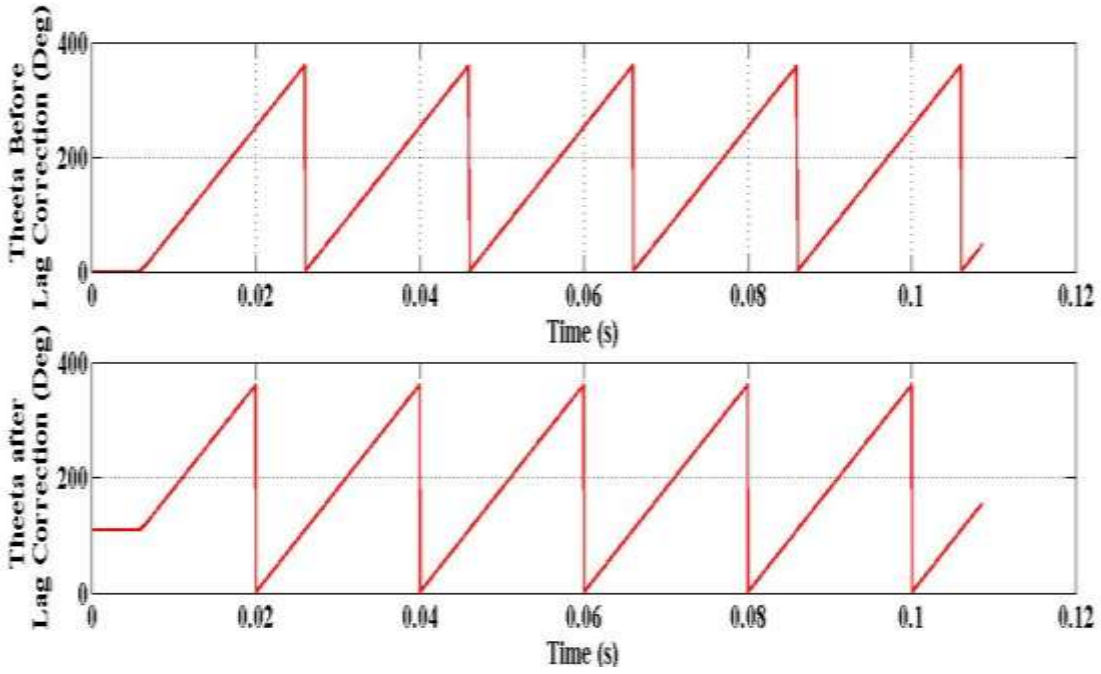


Figure 8.21 (a) and (b): Results of the theta obtained with and without lag correction

Step 12: This step describes the reconstruction of the three-phase current reference signals for all the three-phases, as shown in Figure 8.22. The theta obtained from the previous section is phase shifted by 120° and 240°, as described in Figure 8.22, for generating the three-phase waveforms.

Step 13: The next step is to generate the three-phase sine waves by passing it to the ROM block with the time division multiplexing, as shown in Figure 8.23.

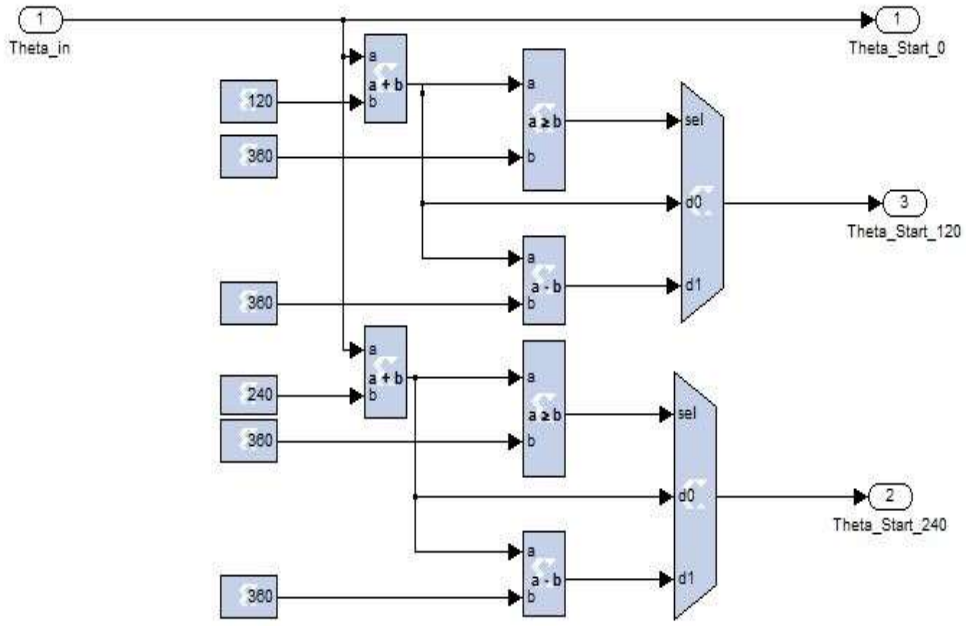


Figure 8.22 Matlab/Xilinx model for generating theta for the three-phase system

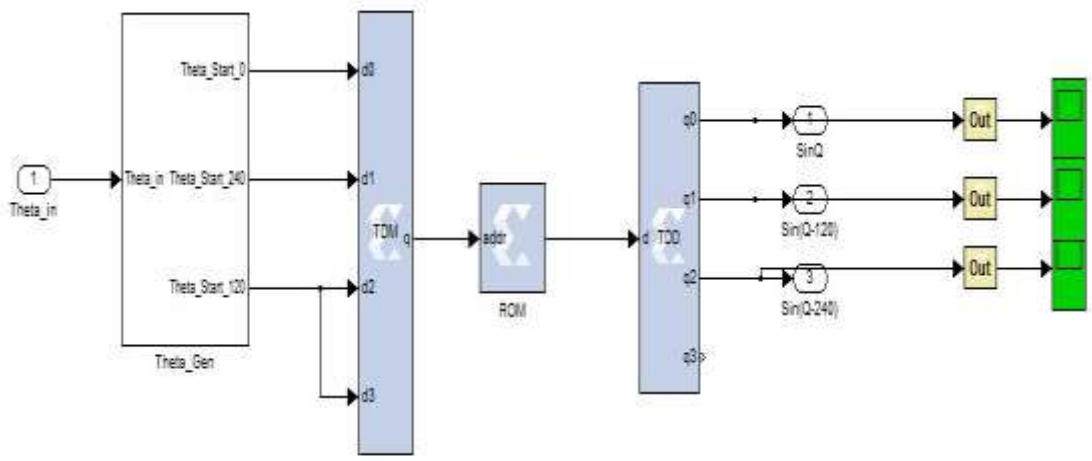


Figure 8.23 Matlab/Xilinx model for generating the sine wave using ROM, TDM and TDD blocks

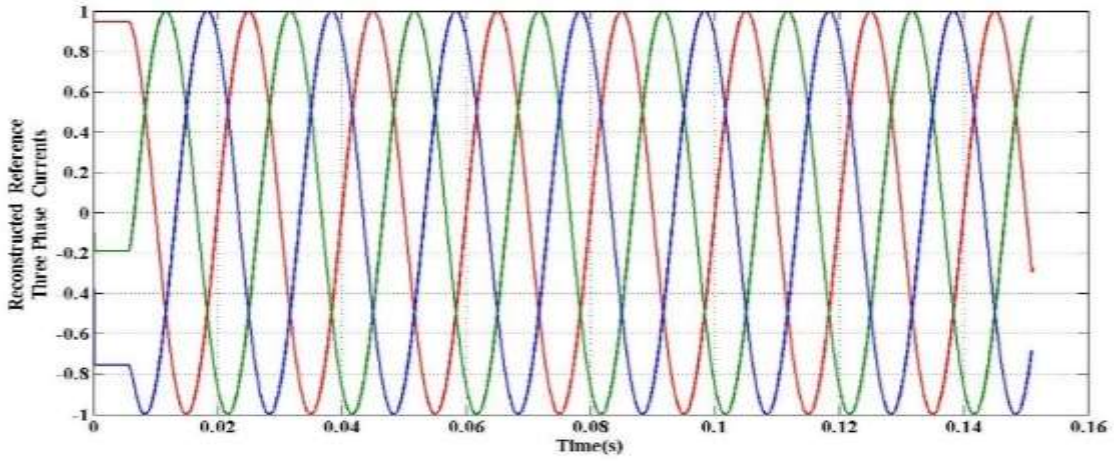


Figure 8.24 Reconstructed reference three-phase currents

(Note - Conventional Method: The conventional way of measuring the three-phase voltages is to employ two voltage sensors on the input side. These sensors deliver the current signal, which is converted into the voltage signal and filtered using a differential amplifier to reject the common mode signals that are superimposed on the desired signals. Also, in order to obtain improved accuracy, the measured voltage signals are filtered using an external filter circuit).

CHAPTER 9

IMPLEMENTATION OF SPEED SENSING LOGIC IN XILINX

9.1 INTRODUCTION

The speed sensor gives a pulse for every rotation of the rotor shaft. The number of pulses per minute gives the speed of the machine. The purpose of this module is to interpret the pulse train from the speed sensor and display the actual speed in rpm using sequential logic circuits designed in MATLAB/XILINX.

Implementation in XILINX:

For simplicity, let us consider that the speed of the machine is 1500 rpm for a period of time. It is useful to review some basic relationships before proceeding.

No. of rotations per minute (rpm) = 1500

No. of rotations per second (rps) = 1500/60 = 25

Hence, the time taken for one rotation = 1/(1500/60)=1/25 = 0.04 s.

The pulse from the sensor would correspond to the duration of one rotation at a time. Hence, the pulse width corresponding to 1500 rpm is given as the time taken for one rotation.

9.2 LOGIC BEHIND THE SPEED SENSING CIRCUIT

We need to obtain the duration of the input pulse, which will directly give us the time for one rotation, from which the speed can easily be obtained as per formula. Here, we know that for 1500 rpm, the duration of one pulse is 0.04 s. Let us see how to obtain this value for the given pulse shown in Figure 9.1. The pulse width can be set to a small value, as this does not play a significant role in measuring the speed.

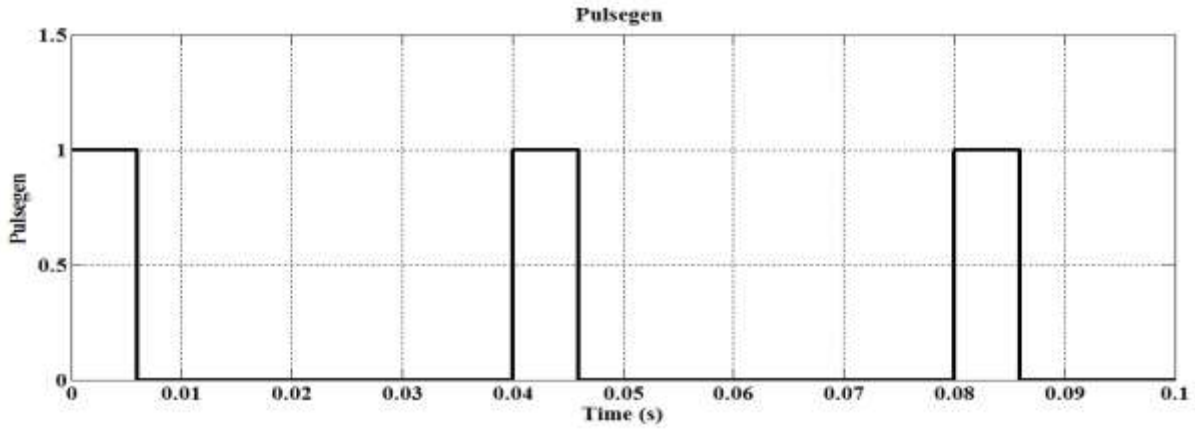


Figure 9.1 Pulse corresponding to 1500 rpm

The rising edges of the pulses are captured using a simple logic circuit. From Figure 9.2, it can be seen that a rising edge is detected when the pulse is high and the delayed inverted pulse is high. This occurs only at the rising edge of the pulse.

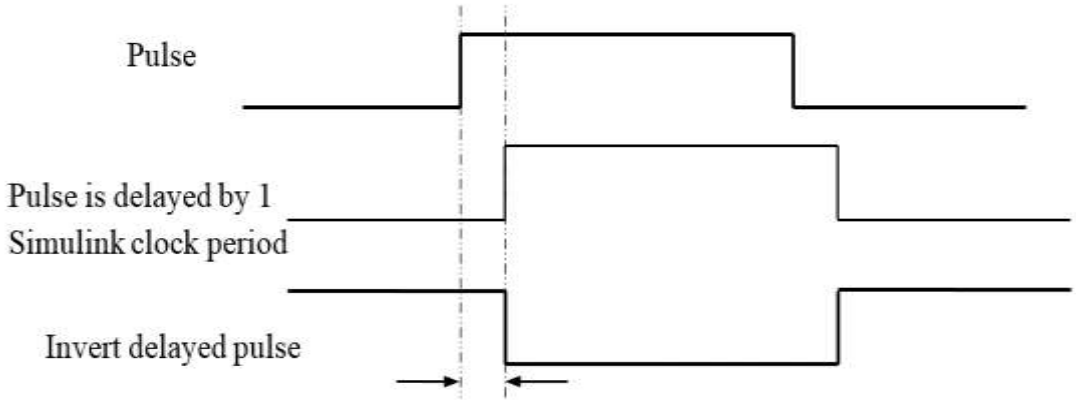


Figure 9.2 Raising edge detection logic

Hence, an AND logic circuit can be used, as shown in Figure 9.3. Figure 9.4 shows the captured edges.

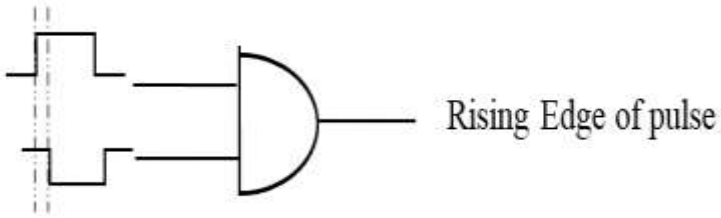


Figure 9.3: AND gate to detect the rising edge of any pulse

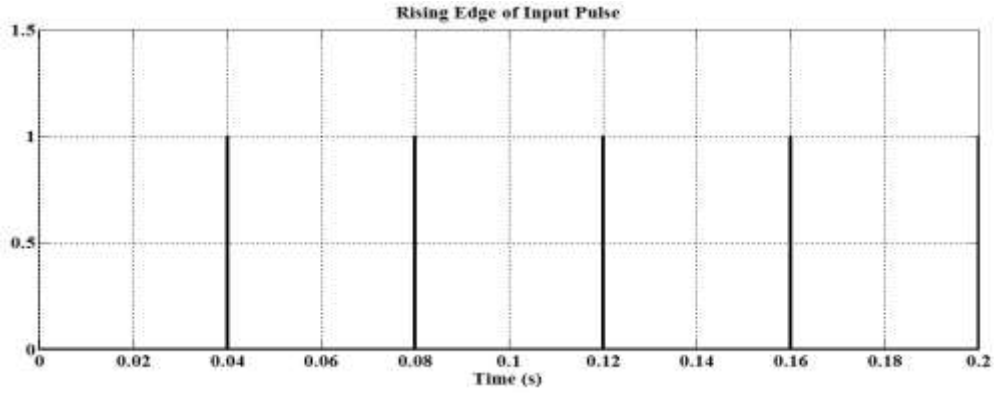


Figure 9.4 Rising edges of the pulse train

The waveform in Figure 9.4 consists of only spikes wherever a rising edge occurs. However, it does not give the time-period of the pulse directly. If this waveform can be converted to a square wave of unit magnitude for 0.04 s (period of the pulse), we can use a counter with a specified clock period and obtain the count value for finding the distance between the rising edge (0 to 1) and falling edge (1 to 0) of the square wave. From the count value and the counter's clock period, we can calculate the time-period of the pulse. This is explained step-by-step in the following sections.

9.3 CONVERTING THE RISING EDGE WAVEFORM TO A SQUARE WAVE

The detected rising edges are converted to a square waveform using a one-bit free running counter with time-period inferred from its input signal. This can be carried out using a counter block from the Xilinx blockset, as shown in Figure 9.5. The enable signal to the counter is the rising edge waveform.

Figure 9.5 Free-running up counter for obtaining the time-period

For an n-bit up-counter, when an enable signal is received, the counter starts counting from the set initial value to 2^{n-1} or in the reverse if it a down-counter. As we use a one-bit counter, it counts from 0 to 1 only as long as the enable signal is present.

Note that a reset signal has not been given to the counter. If we had used a reset signal, the counter will wrap to the initial value once it overflows. As we require a signal of unit magnitude until the next rising edge for deriving the time period of the pulse, we do not give a reset signal to the counter. Hence, the count value at the instant of removal of the enable line is held until the enable line goes high again.

Initially, the enable line of the counter is zero. Hence, the counter is not enabled, and the output is also zero. At 0.04 s, when the enable line goes high, the counter is enabled, and starts counting (from 0 to 1). As there is no reset signal, the final value 1 is obtained at the output of the counter. Once the enable line goes low, the count value is retained, i.e., 1 in our case. Hence, we obtain unit amplitude from 0.04 s to 0.06 s. At 0.06 s, the enable line of the counter goes high. From its previous value 1, it starts counting. As it can count only from 1 to 0, the count value becomes 0. As soon as the counter is disabled, the value 0 is retained and is obtained as the output of the counter. Hence, from 0.06 s to 0.08 s, we obtain a 0. Figure 9.6 shows the square wave thus obtained.

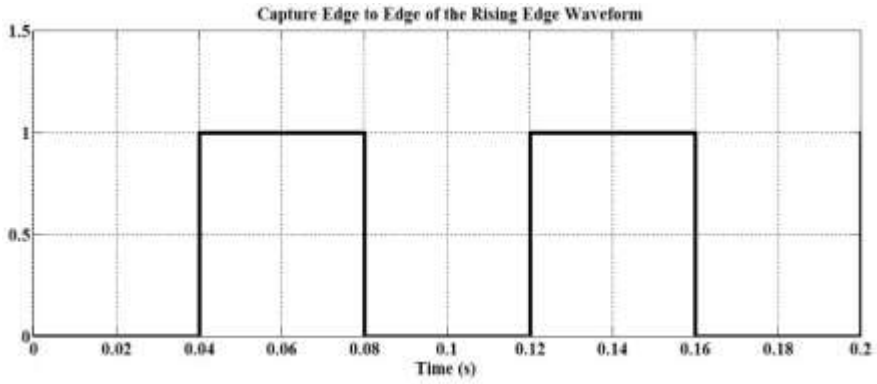


Figure 9.6 Rising edges converted to the square wave

9.4 OBTAINING A FIXED INTEGER VALUE TO INTERPRET THE TIME PERIOD

From the waveform of Figure 9.6, it can be seen that the duration of the unit magnitude of the square wave is equal to the time-period of the pulse from the sensor (0.04 s to 0.08 s). In order to extract the information about the duration of the pulse, a free-running up-counter of width 21 bits and explicit clock frequency of 20 kHz, with enable and reset signals is used.

The purpose of this counter is to start counting once it receives the enable signal (the square wave). When the enable signal is removed, it has to reset to zero. We invert the enable signal and give it as the reset signal to the counter. In doing so, as long as the enable signal is available, the reset signal is low. Once the square wave goes low, the enable line also goes low. Now, if the reset line goes high, then at the next enable line, the counter will start counting from 0 again.

The idea is to capture the value in the counter at the instant the enable line goes from high to low. The counter increments by one for every clock cycle (time period 5×10^{-5} s). The counter increments by one every 5×10^{-5} s. As it is a 21 bit counter, it can count from 0 to 2097151. The choice of the number of bits was 21 for obtaining the speed measurement with a resolution of 0.5 RPM. More the number of bits, the more is the accuracy in speed obtained. For finer speed measurements, one can go for higher bit numbers at the cost of longer simulation time and program memory. Figure 9.7 shows the settings of the counter and Figure 9.8 shows the counter output.

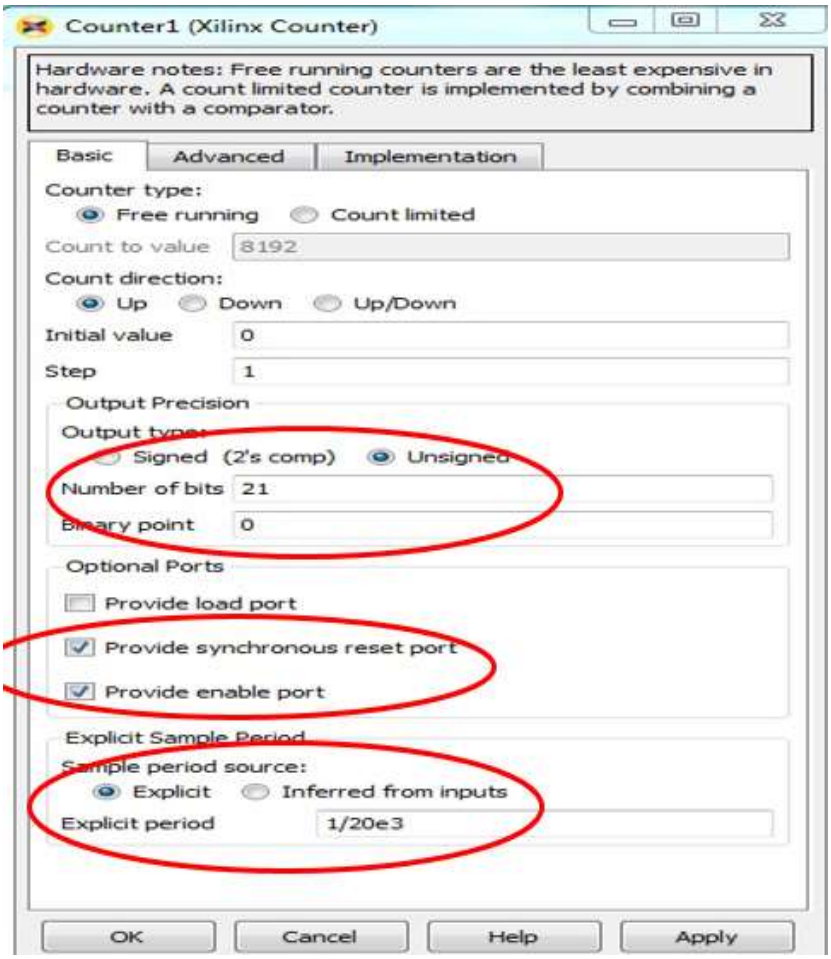


Figure 9.7 Counter settings to obtain the count between edges

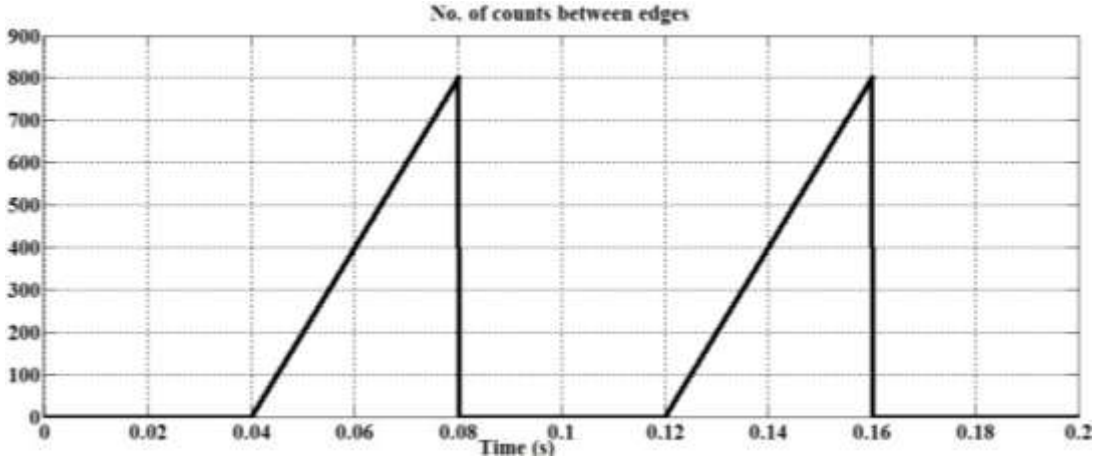


Figure 9.8 Count between edges

If we capture the final value in the counter using a sample and hold circuit (S & H), we can obtain the number of counts for the duration of the pulse. Figure 9.9 shows the output of the S&H circuit.

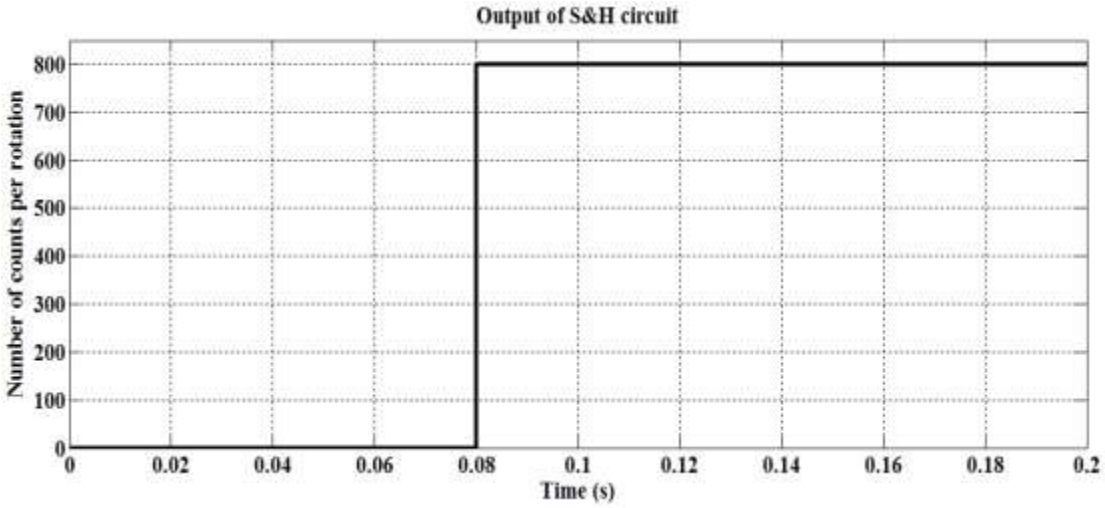


Figure 9.9 No. of counts obtained from the S&H circuit

A simple calculation gives the time-period of the pulse is given below.

The count value obtained from the S&H circuit : 800

Time for one-step increase in count : 5×10^{-5} s

Time taken for the counter to reach final value = $800 * 5\times10^{-5} = 0.04$ s.

Thus, we have obtained the time-period for one rotation of the machine shaft. The number of such rotations in one second = 1/0.04 = 25.

9.5 DIVISION IN XILINX

There are two blocks that support division: Cordic Divider & the Divide Generator, but they are complex. The basic concept behind division, which is repeated subtraction, is used here. The output of the S&H circuit is repeatedly subtracted from a large number (10,000 initially). For every subtraction performed, the value in the accumulator is increased (±b). This goes on as

long as the value from S&H circuit is greater than that obtained after repeated subtraction. Hence, a comparator is used to check for the sign of the variable.

The output of the comparator acts as the enable line of the accumulator. As long as the comparator output is high, repeated subtraction takes place, and the value in the accumulator is incremented. The reset line of the accumulator is set as the "Synchronous reset line". This is done so that the value of the multiplexer that passes the value for subtraction resets to 10,000 once the comparator output goes low. In addition, the value in the accumulator is reset to its initial value at the same time. By doing so, the circuit is now ready for the next cycle of repeated subtraction.

The value in the accumulator keeps changing, but we require the value at the end of repeated subtraction, which gives us the actual information we need. In order to capture this information, a register with an enable line is used. The output of the accumulator is the input to the register. The Reset line to the accumulator is given as the Enable line to the register. When the accumulator gets a reset signal, it means the end of the division. At the same instant, when the register is enabled, the data in the accumulator are passed onto the register. The register holds this data until the next enable line is received. Figure 9.10 shows the XILINX for division.

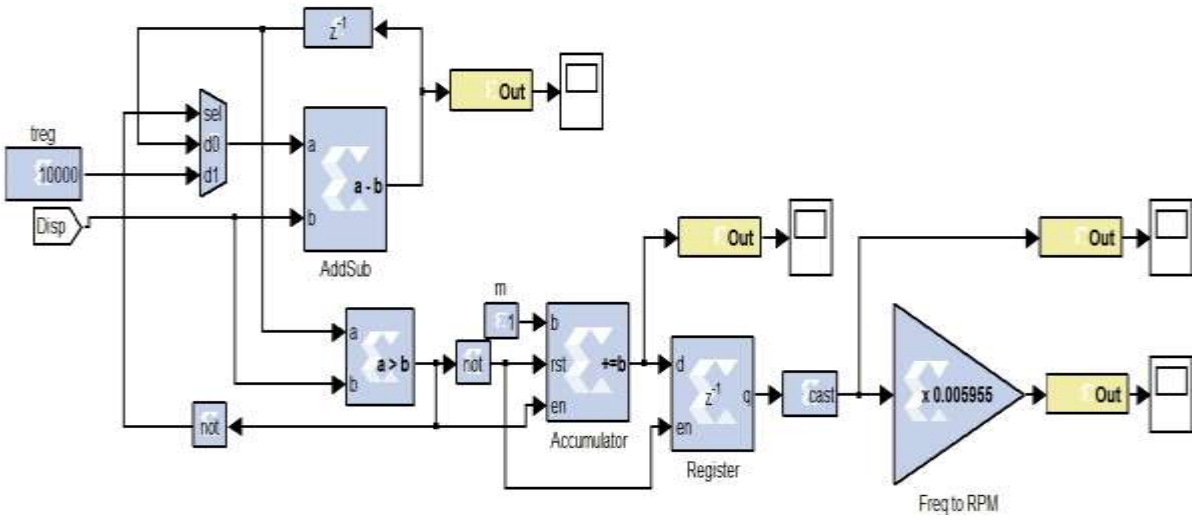


Figure 9.10 Division in XILINX

Figures 9.11 and 9.12 show the settings of the multiplexer and subtraction blocks, respectively. The number of bits assigned is important here. As the time-period is only 0.04 s, when we

subtract from 10,000 we get decimal point results. For higher values of speed, the time-period can have more number of decimal points. For this reason, the number of bits to be assigned for the binary points should be high. In addition, the number of bits required for numbers up to 10,000 is 14. To include the binary points also, the number of bits is usually set at a high value with 14 bits assigned for the whole number and the remaining for the binary points. Here, we take the total number of bits to be 80, and number of bits for binary point as 50. It is an exaggerated value, but for now, we stick to this.

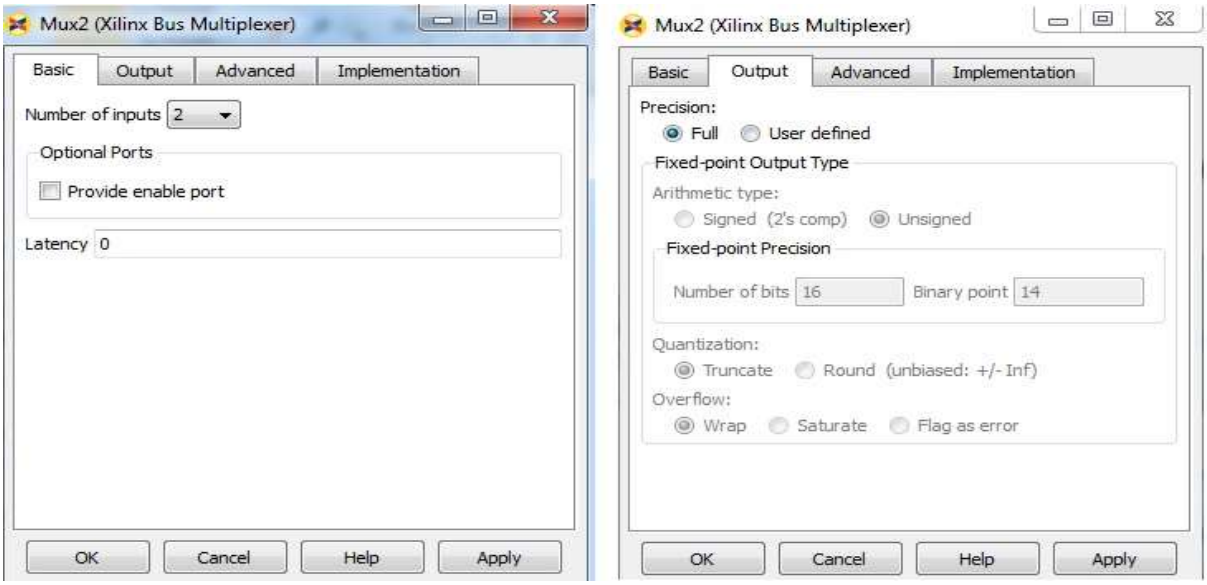


Figure 9.11 Multiplexer settings

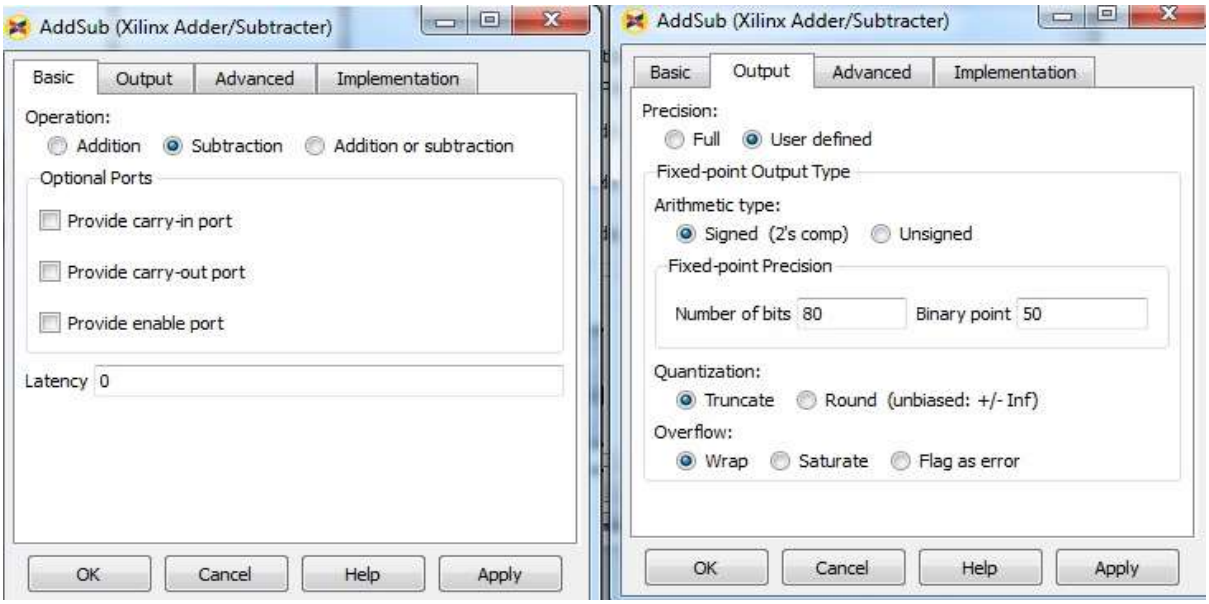


Figure 9.12 Setting for the Add-Sub block

Figure 9.13 shows the settings obtained for the accumulator.

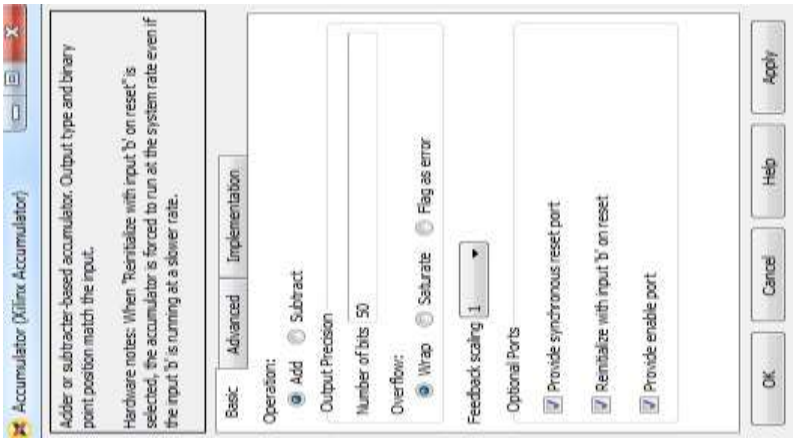


Figure 9.13 Accumulator settings

The value stored in the accumulator corresponding to very high speeds (> 2000 rpm) can be a large value. Hence, a large number of bits are assigned. Note that reset and enable ports are provided. The outputs of the subtractor, accumulator and the register should be observed carefully for a good understanding of the working of the division block, which is inferred from Figures 9.14 to 9.16.

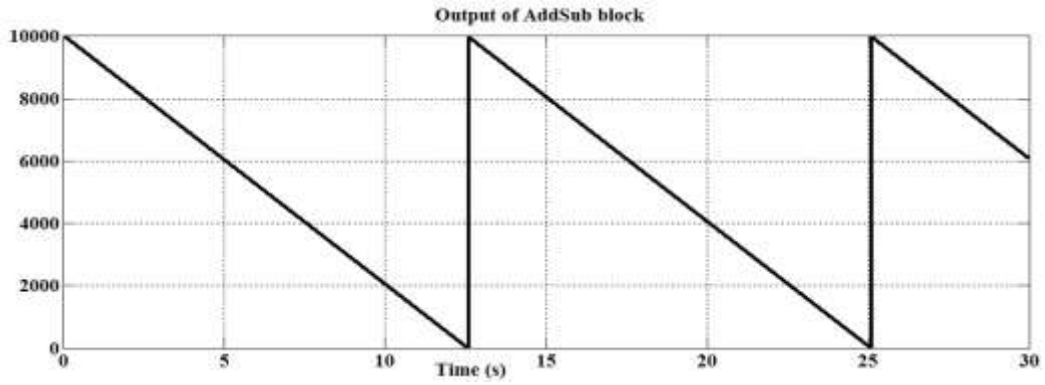


Figure 9.14 Output of the Add-Sub Block

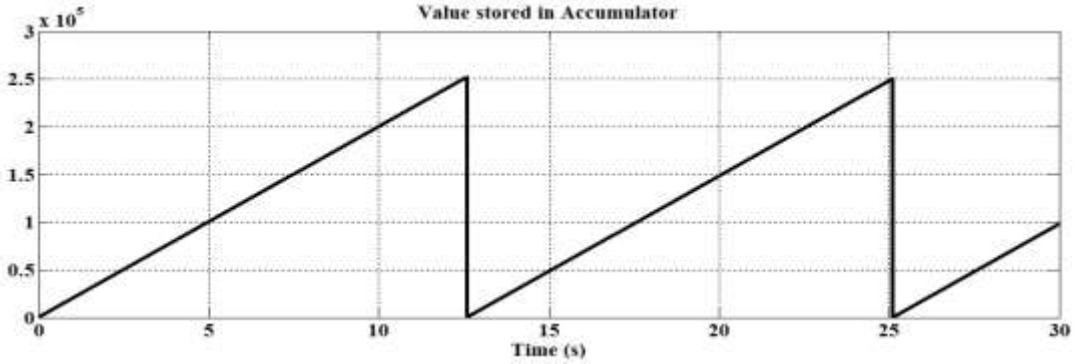


Figure 9.15 Value stored in the accumulator during repeated subtraction

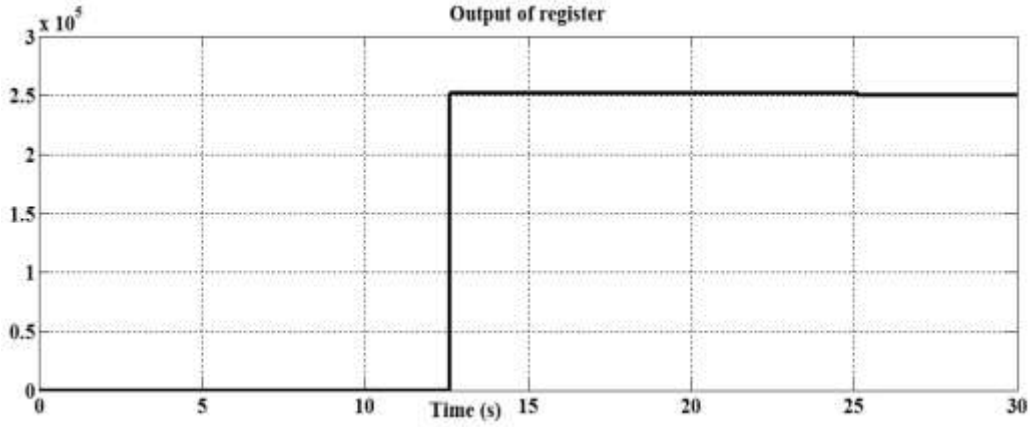


Figure 9.16 Quotient of division obtained from the register

The subtraction and accumulation process takes place in very fine steps. The output of the subtractor is zoomed to show the minute steps, as shown in Figure 9.17.

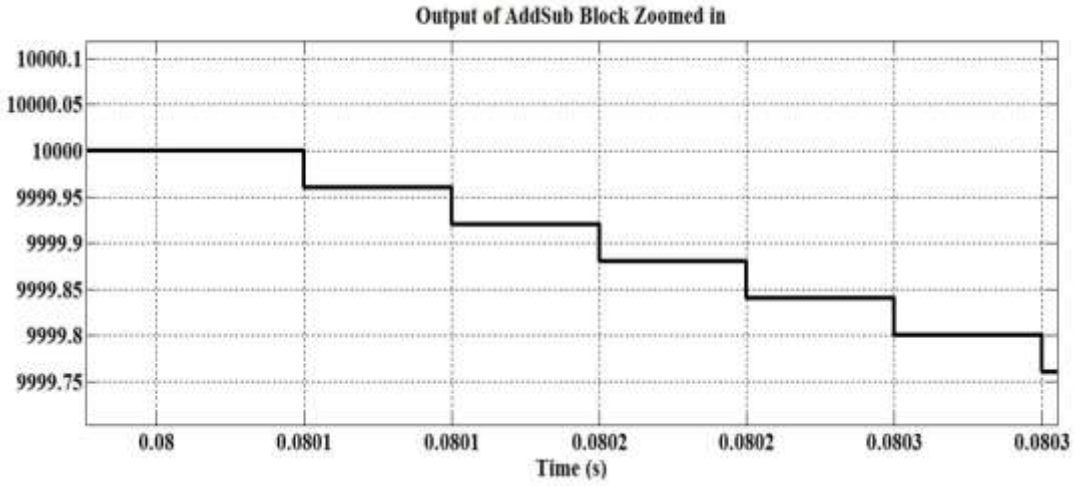


Figure 9.17 Portion of the Add Sub-block output

The value in the register is 251920. It has to be remembered that this result has been obtained by subtracting from 10,000. Actually, we should have performed repeated subtraction from 1. If we had done this, for very small speeds (<700 rpm), the time for 1 rotation is pretty close to 1. Repeated subtraction from 1 would have resulted in an error. The next step is to deduce the speed from this value. On multiplying the count value in the register by a proportional value, we will get the speed. As we know the speed of 1500 rpm, the result of the division is 251920 and the multiplication factor for the register value is 1500/251920 = 0.005955.

This is clearly an approximation, but gives the speed close to the actual values with an error of ±10 rpm for any value of speed with a resolution of 0.5 rpm. Figure 9.18 shows the speed obtained. Figure 9.19 shows the complete logic model. Figure 9.20 shows the speed values obtained from the module for the pulses corresponding to various input speeds.

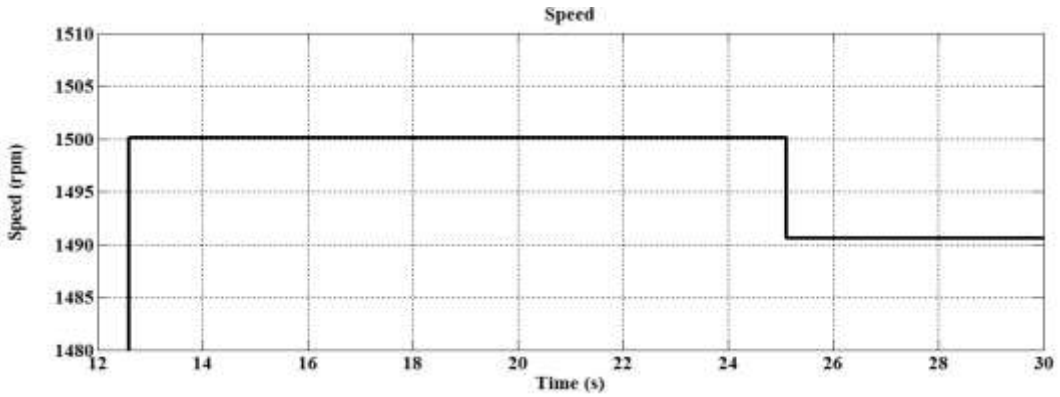


Figure 9.18 Speed value obtained

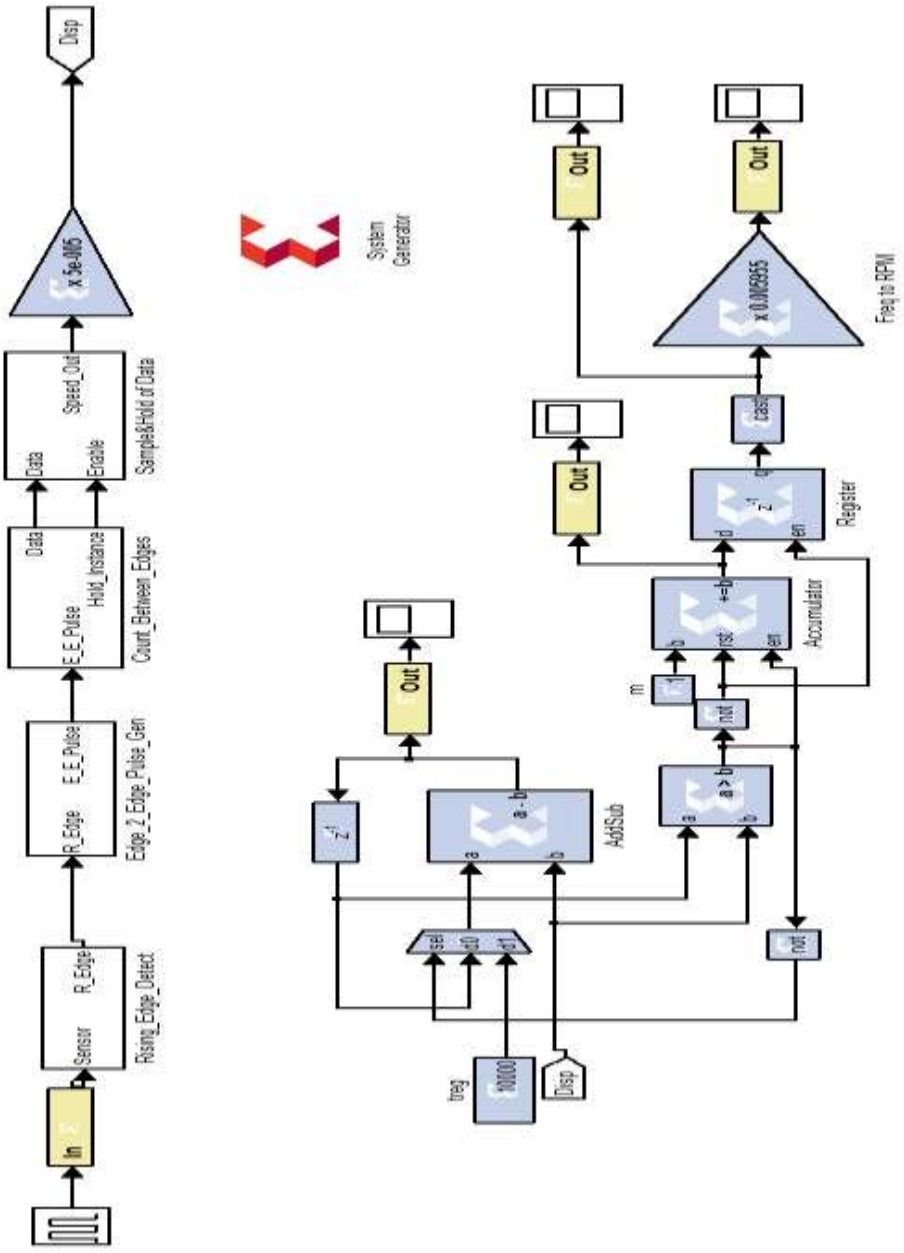


Fig 9.19 Speed sensing

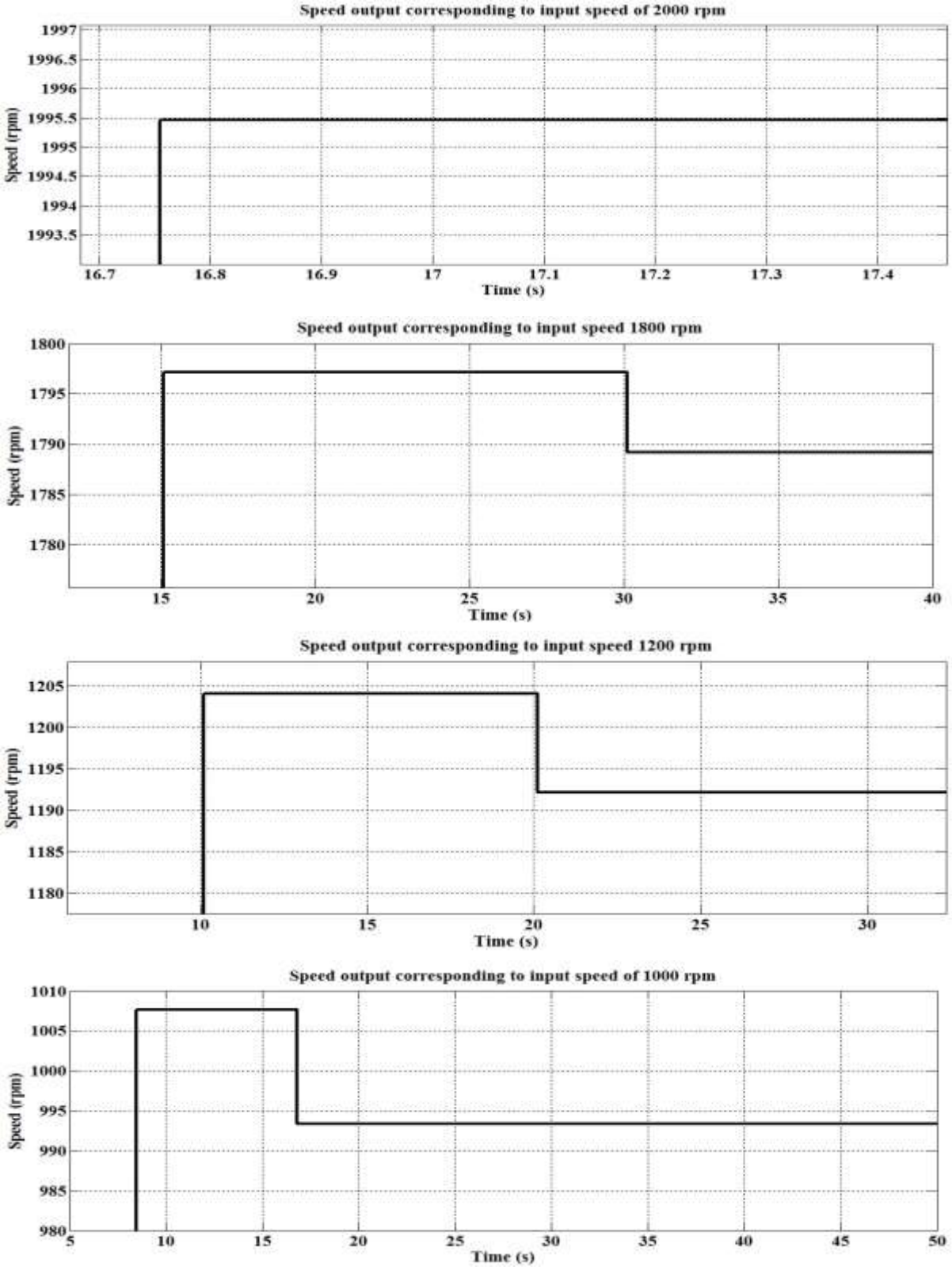


Figure 9.20 Speed values obtained from the module for various input values of speed

CHAPTER 10

HARDWARE IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

10.1 INTRODUCTION

The operation of various hardware units used in this work for experimental verification is discussed and the integration of these units to validate the concept behind the work is described in detail. The hardware results are presented along with the scope of this work is future.

10.2 LIST OF HARDWARE UNITS USED IN THE WORK

1) Induction motor coupled to Slip ring Induction generator
2) Variable Frequency Drive – YASKAWA
3) Power switches – APTGT150DU120G (Micro semi)
4) Driver module – Concept 2SD106AI
5) Clamp Circuit – Matrix converter Protection
6) Filter circuit - Matrix converter Input filter
7) 3 phase- Comparator Circuit – Generating internal current reference
8) Four-step Commutation circuit - output current Direction sensor unit
9) Power supply Unit (+-15V, 5V)
10) FPGA Controller unit – Sparten 3E – 500K (Nexys 2)
11) Analog to Digital converters – Pmod AD1
12) Power and Voltage Transducers – MECO
13) Proximity sensor – Speed Sensing

10.3 INDUCTION MOTOR COUPLED WITH SLIP RING INDUCTION GENERATOR

The squirrel cage induction motor is used as a prime mover for the doubly fed induction generator. To simulate the dynamic wind conditions a variable frequency drive from YASKAWA is used to feed the squirrel cage induction motor. Figure 10.1 shows the motor generator setup used in the experiment. The machine rating of the induction motor – induction generator setup is given in Table 10.1.

Table 10.1 Machine rating of induction motor-induction generator setup

Type	Squirrel Cage Induction Motor	Slip Ring Induction Generator
Make	Crompton Greaves	Ramson
Hp	5	3
Phase	3	3
Stator Volts (L-L)	415V +10%	415 V
Current	7.4A	4 A
Exc. Volts	-	~ AC
Frequency	50Hz	50 Hz
RPM	1430	1440
Duty	S1	S1
Class	-	B

Figure 10.1 Induction motor - induction generator setup

The DC test, NO load test and blocked rotor test were conducted on the setup and the machine parameters were estimated. Using the estimated machine parameters the steady state torque-slip characteristics and power-slip characteristics were obtained as is shown in Figure 10.2.

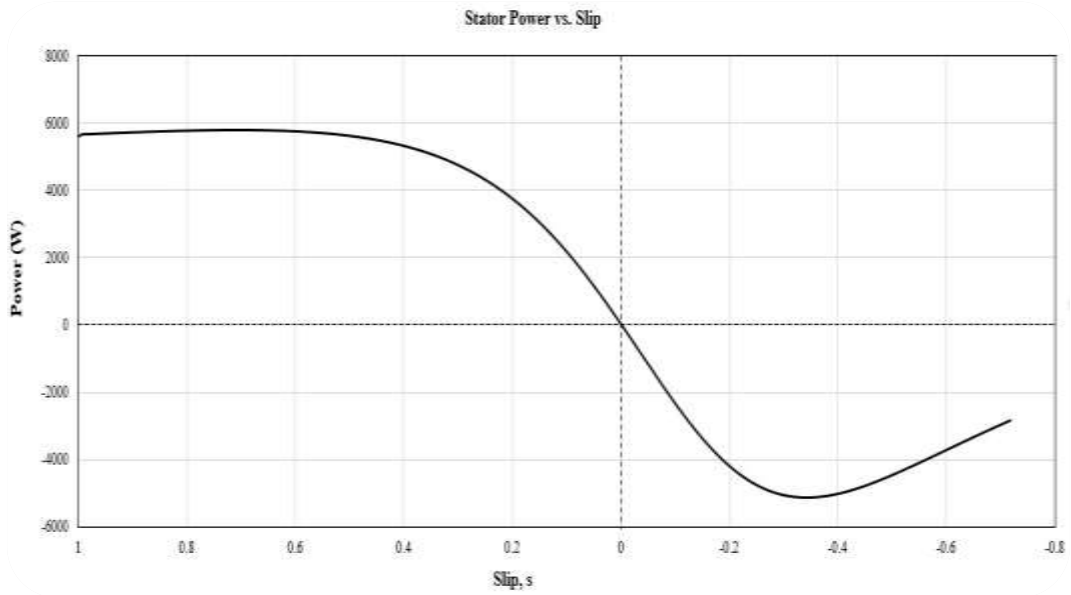


Figure 10.2(a) Power-slip characteristics of the induction generator used

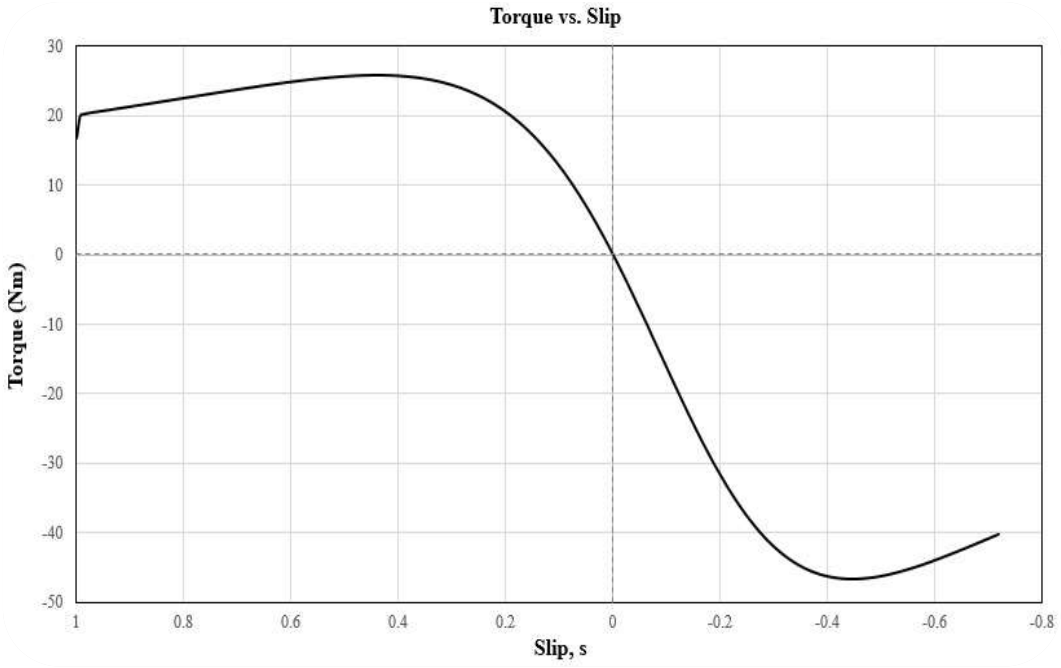


Figure 10.2(b) Torque-slip characteristics of the induction generator used

10.4 YASKAWA VARIABLE FREQUENCY DRIVE

Figure 10.3(a) and Figure 10.3(b) shows the YASKAWA V-1000 drive and its connection diagram with peripheral devices and Table 10.2 gives the specification of the drive.

Table 10.2 YASKAWA-V1000 specifications

Parameter	Details
Manufacturer	YASKAWA electric Corporation, Japan
Model	CIMR – VT4A0011BAA 400V, 3Phase, 5.5KW/ 3.7KW
Inputs	3 phase AC, 380V-480V, 50 /60 Hz, 14 A/ 10.4A
Outputs	3 phase AC, 0V-480V , 0Hz – 400Hz, 11.1 A/ 9.2 A
Mass	2.4 Kg

Figure 10.3(a) YASKAWA VFD Module

To simulate the dynamic conditions of the wind, the speed of the prime mover (induction motor) is required to be changed and this is achieved by changing the magnitude and frequency of the supply to the prime mover. The output frequency and magnitude of the YASKAWA V1000, which feeds the induction motor, can be varied by applying a variable DC voltage ranging between 0 V to 10 V to its control terminal. A simple potential divider circuit placed on its control terminal achieves variable voltage.

The VFD is programmed to generate frequency outputs from 30 Hz to 60 Hz that corresponds to different speed levels between sub-synchronous to super synchronous speeds. The command input 10 V corresponds to the minimum speed and 0 V corresponds to maximum speed.

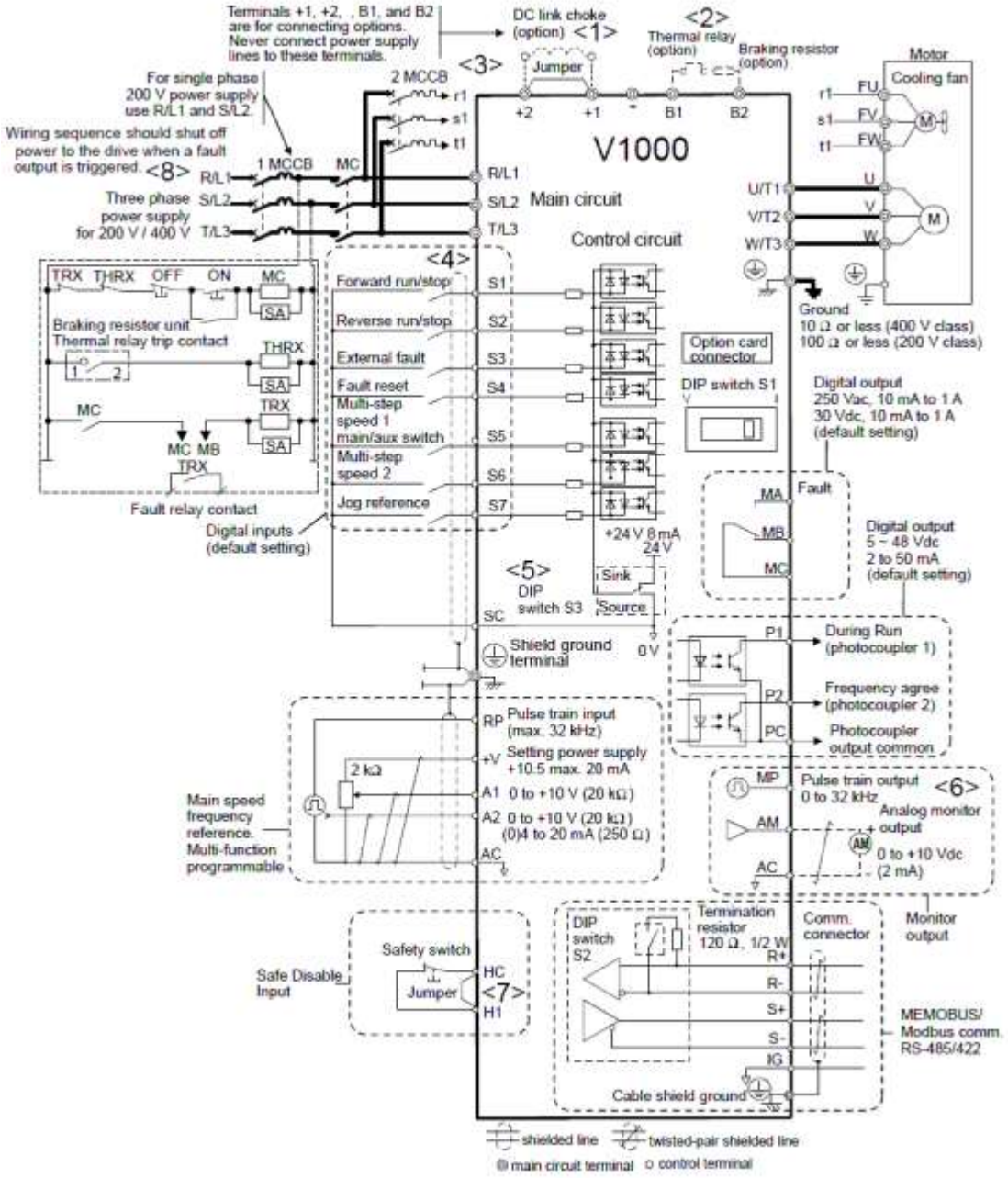


Figure 10.3(b) Connection diagram of the YASKAWA VFD drive

10.5 POWER SWITCHES – APTGT150DU120G

The power switch used in this module is a fabricated bidirectional switch designed by Micro-Semi whose part number is APTGT150DU120G. Each power switch consists of two IGBTs connected in a common emitter configuration and two diodes connected in anti-parallel to each IGBT. Figures 10.4(a) and 10.4(b) gives the power switch and the internal connection diagram of the power switch. Table 10.3 give the device specifications for maximum ratings.

Figure 10.4(a) APTGT150DU120G bidirectional power switch

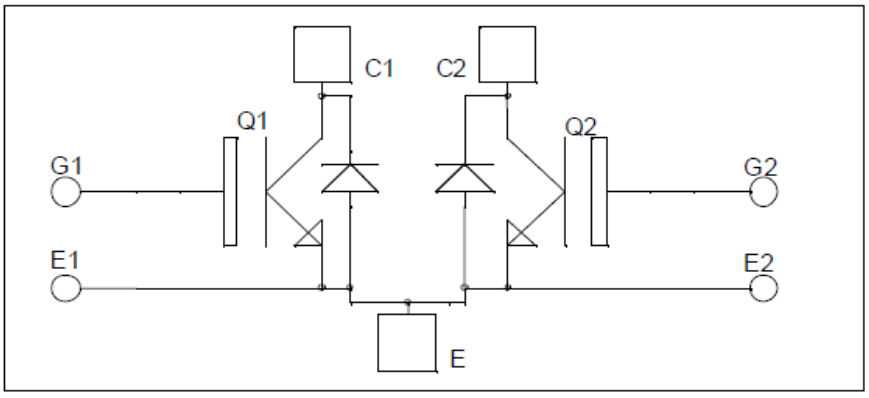


Figure 10.4 (b) Internal connection diagram of APTGT150DU120G

Table 10.3 Device specifications (for maximum ratings) of APTGT150DU120G

Symbol	*Parameter*		*Max ratings*	*Unit*
V_{CES}	Collector - Emitter Breakdown Voltage		1200	V
I_C	Continuous Collector Current	$T_C = 25°C$	220	A
		$T_C = 80°C$	150	
I_{CM}	Pulsed Collector Current	$T_C = 25°C$	350	
V_{GE}	Gate – Emitter Voltage		±20	V
P_D	Maximum Power Dissipation	$T_C = 25°C$	690	W
RBSOA	Reverse Bias Safe Operating Area	$T_j = 125°C$	300A @ 1150V	

Figures 10.5 and 10.6 give the turn-ON and turn-OFF characteristics of the power switches. Tables 10.4 and 10.5 give the data for calculating respective ON and OFF dead times for safe commutation of the switches. We require a "dead-time" period to allow the IGBT to turn-ON with a delay equal to four times observed value.

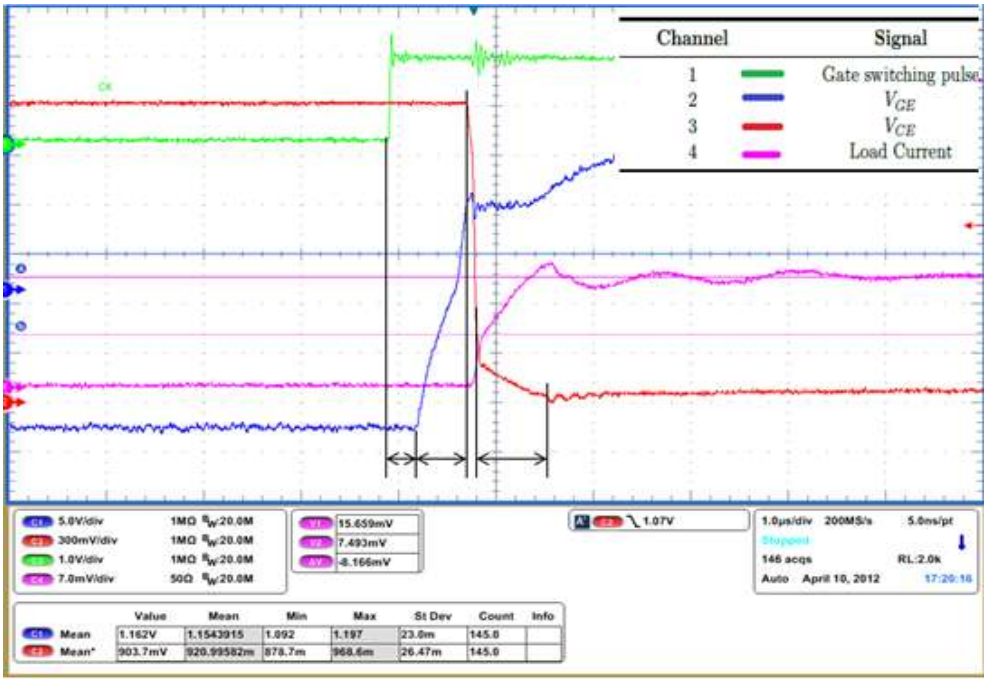


Figure 10.5(a) IGBT Turn-ON characteristics

Table 10.4 Dead time determination for turn-ON

Time Value	Value(ns)
t_1	280
t_2	575
t_3	145
t_4	720

Equation (10.1) gives the dead time for turn-ON of the device.

$$Td\_ON = t1 + t2 + t3 + t4 \quad = 1720ns \approx 1800ns = 1.8\ \mu s \qquad (10.1)$$

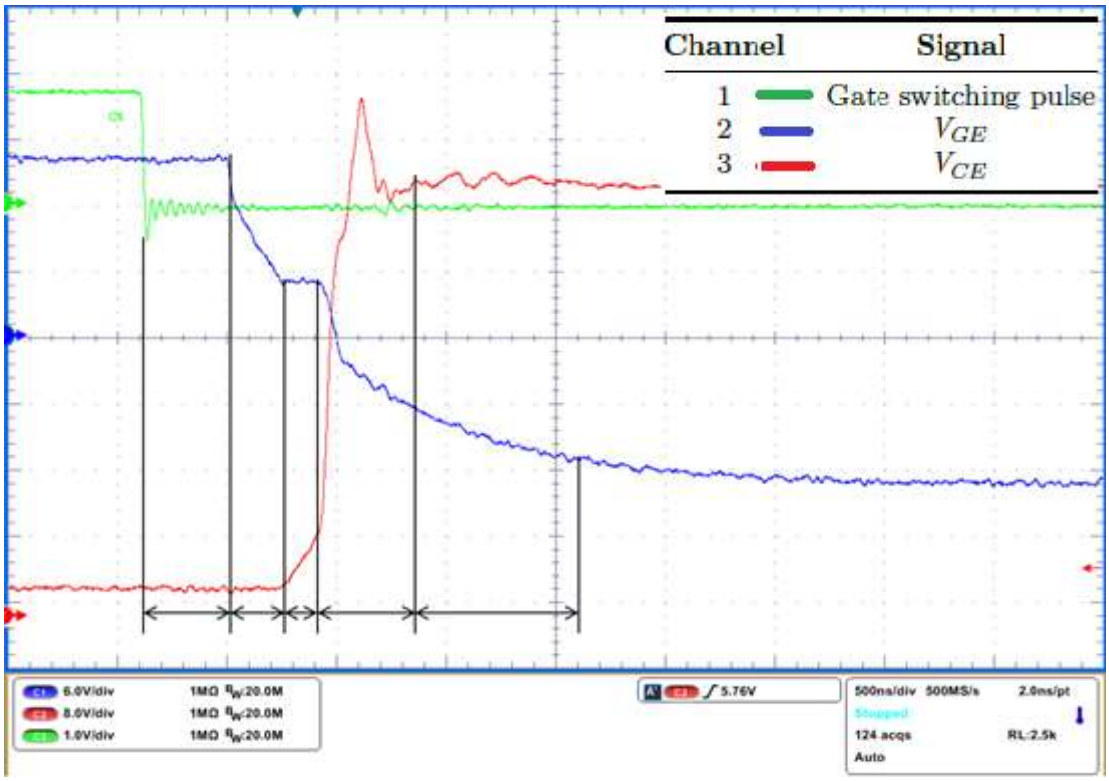


Figure 10.5(b) IGBT turn-OFF characteristics

Table 10.5 Dead time determination: Turn OFF

Time Value	Value(ns)
t_1	375
t_2	250
t_3	180
t_4	430
t_5	560

Similarly, the Dead time for Turn OFF of the device is equal to the sum of 5 times observed and is given by Equation (10.2)

$$Td\_OFF = t1 + t2 + t3 + t4 + t5 = 1795ns \approx 1800ns = 1.8\ \mu s \quad (10.1)$$

10.6 DRIVER MODULE – CONCEPT 2SD106AI

The concept driver ICs are specifically designed for safe and reliable operation of the IGBTs and the power MOSFETs. They are also called as dual SCALE divers, where 'SCALE' stands for Scalable, Compact, All-purpose, Low cost and Energy to use. This driver finds its applications in inverters, converters, traction, DC-DC converters and switched mode power supplies. The main functions are: driving, monitoring, status acknowledgement, isolated voltage supply, DC/DC converter and electrical isolation of all signals between the control electronics and the power section. Figure 10.6 shows the simple block diagram of the concept SCALE driver.

10.6.1 Overall Functions of the Chip

The chip accepts the PWM inputs from the control electronics through its second input pins and isolates it using the pulse transformer and then amplifies the received PWM signals and applies to the gate of the power semiconductor switch. It also allows it be operated in two different modes using its mod pin: half bridge/ direct mode. It also does the other important functions like the short circuit and the overload protection using the collector sense circuit, status acknowledgement signals through its status pins when the error occurs, power supply monitoring circuit, blocking time logic circuit which blocks pulses to the switch when the error occurs and V_L / Reset pin to erase the memories of the error after it has been cleared.

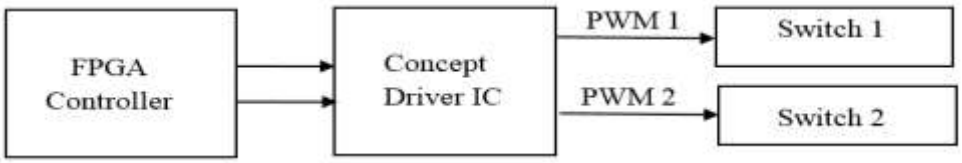


Figure 10.6 Simple Block Diagram of Concept Driver IC

Figure 10.7 shows the detailed block diagram of the concept scale driver IC 2SD106AI -17. It contains two channels to drive the two switches independently. The two major blocks of the IC are: Logic to Driver Interface – LDI and Intelligent Gate Driver- IGD (two channels). It also includes the other blocks like the pulse transformers, isolated voltage supply (DC-DC converter). The IC needs two different power supplies say 'VDD' and 'VDC' of 15-V, as shown in the block diagram. The IC is a 24-pin chip that is able to drive two switches independently at a time. The major pins are: 2 pins for the voltage supply, 2 pins for the GND, 2 pins for the PWM inputs, 2 pins for the dead-time generation, 2 pins for the status acknowledgement (to know about the error), 1 pin to define the mode of operation (either half bridge/direct mode), 1 pin to erase the memory of the occurred error after it has been cleared, 2 pins for the collector sense channel, 2 pins for the emitter channel, 2 pins for the gate channel, 2 pins for the reference resistor channel, and the remaining 4 pins are free. The following sections give the details of LDI, IGD, pulse transformer, and the description of the pins.

10.6.2 Logic to Driver Interface (LDI)

The LDI is the first building block of the SCALE chip, which interfaces to the control electronics. An LDI drives two channels. The PWM signals from the control electronics are applied to inputs A and B (PIN: InA & InB) and are processed so that the drive information can be fed to the pulse transformer for each channel. It is also used to evaluate the status acknowledgement transmitted in the coded form.

10.6.3 Pulse Transformers

There are two small-sized pulse transformers for the isolation of the two channels. They offer outstanding isolation properties and low coupling capacitances. The pulse transformers were selected because they offer the following advantages over all other designs: minimum delay times, no degradation effects, maximum service life and the ability to obtain isolation voltages of any desired magnitude.

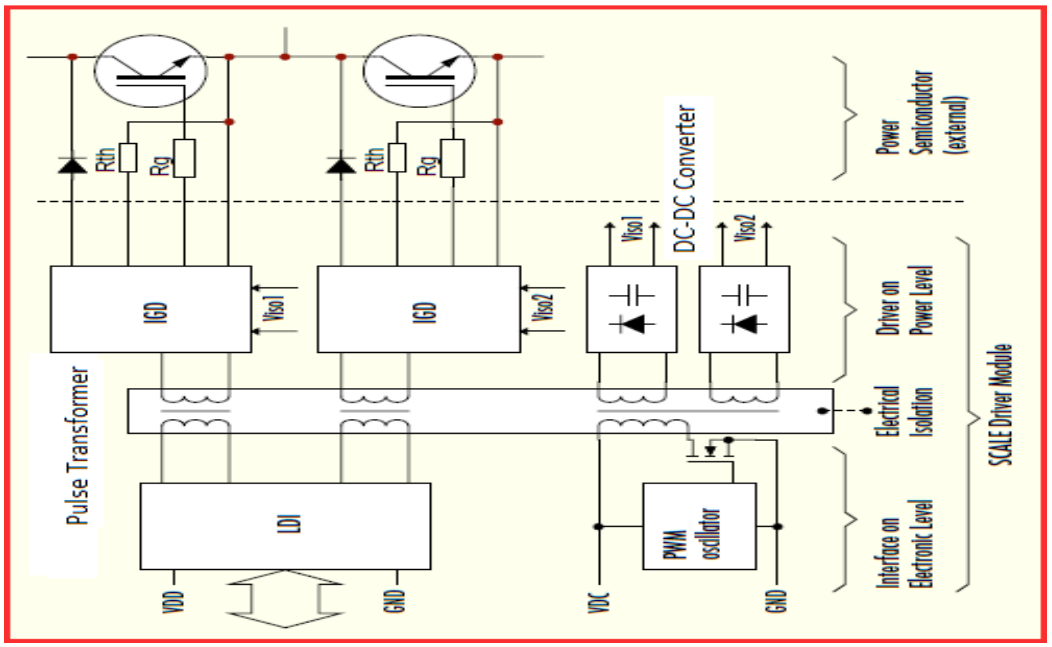


Figure 10.7 Block Diagram of the concept SCALE driver IC 2SD106AI-17

10.6.4 Intelligent Gate Driver

The next building block of the SCALE Driver is IGD. There are two IGDs present in this chip 2SD106AI, one for each channel. It receives the pulse-coded information from the transformers and reconstructs the original PWM signals from it. This signal is then amplified to drive the semiconductor. The other important functions of this block are the pulse transformer interface, overload and short circuit protection, blocking time logic, status acknowledgement, monitoring of the supply voltage, and the output stage. The protection functions that safeguard the power semiconductor from harmful operating conditions are discussed later in this report.

10.6.5 DC-DC Converter

This converter makes electrically isolated power supply available to the individual driver channels. Next, we will discuss about the descriptions of 24 pins. For ease of study, we will first study the description of the pins on the input side and later the pins on the output side as given in Tables 10.5 and 10.7.

Table 10.6 Descriptions of the pins on the input side

Pin No	Designation	Function
1	VDD	+15 V for electronic input side, that drives the 3.3 V input from the FPGA to the driver.
2	GND	GND for electronic input side
3	SO1	Status output channel 1
4	VL	Logic level/reset
5	RC1	RC network dead-time channel 1
6	InA	Input A
7	InB	Input B
8	RC2	RC network dead time channel 2
9	MOD	Mode input
10	SO2	Status output channel 2
11	GND (dc)	Ground for the DC – DC converter
12	VDC	+15 V for DC- DC converter

10.6.6 Detailed Descriptions of the Pins on the Input side

i. **VDD:** A stabilized voltage supply of +15V with respect to GND is connected to the terminal VDD.

ii. **GND:** Pin GND is connected to the ground of the electronic power supply.

iii. **SO1 and SO2:** The output of SO1& SO2 consists of an open collector transistor. The output is pulled to GND if an error has been detected on the channel 1 & 2 respectively. The transistor goes high when no error is present.

iv. **VL:** This pin defines the logic level and also acknowledge for the error occurred. When the PWM signals have TTL level, pin VL is connected, as shown in Figure 10.8.

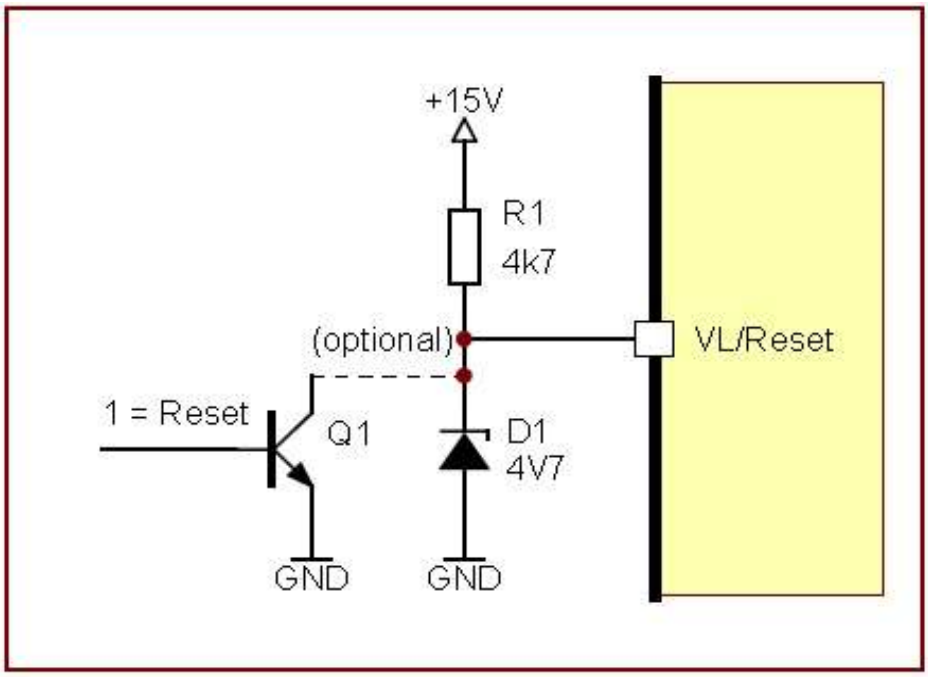


Figure 10.8 Circuit for input VL/reset for 5 V logic

Similarly, when the signals at inputs InA and InB have 15V level, the V_L pin should be connected via a resistor to +15V as shown in Figure 10.8. The switching thresholds of Schmitt trigger inputs InA and InB are then 5V and 10 V respectively.

v. **RC1 and RC2:** In half bridge mode, an RC network is connected to each of the RC1 and RC2 pins. It determines the dead time of the corresponding channel as shown in Figure 10.9. In addition, Table 10.6 gives the values of the dead-times of the corresponding channel.

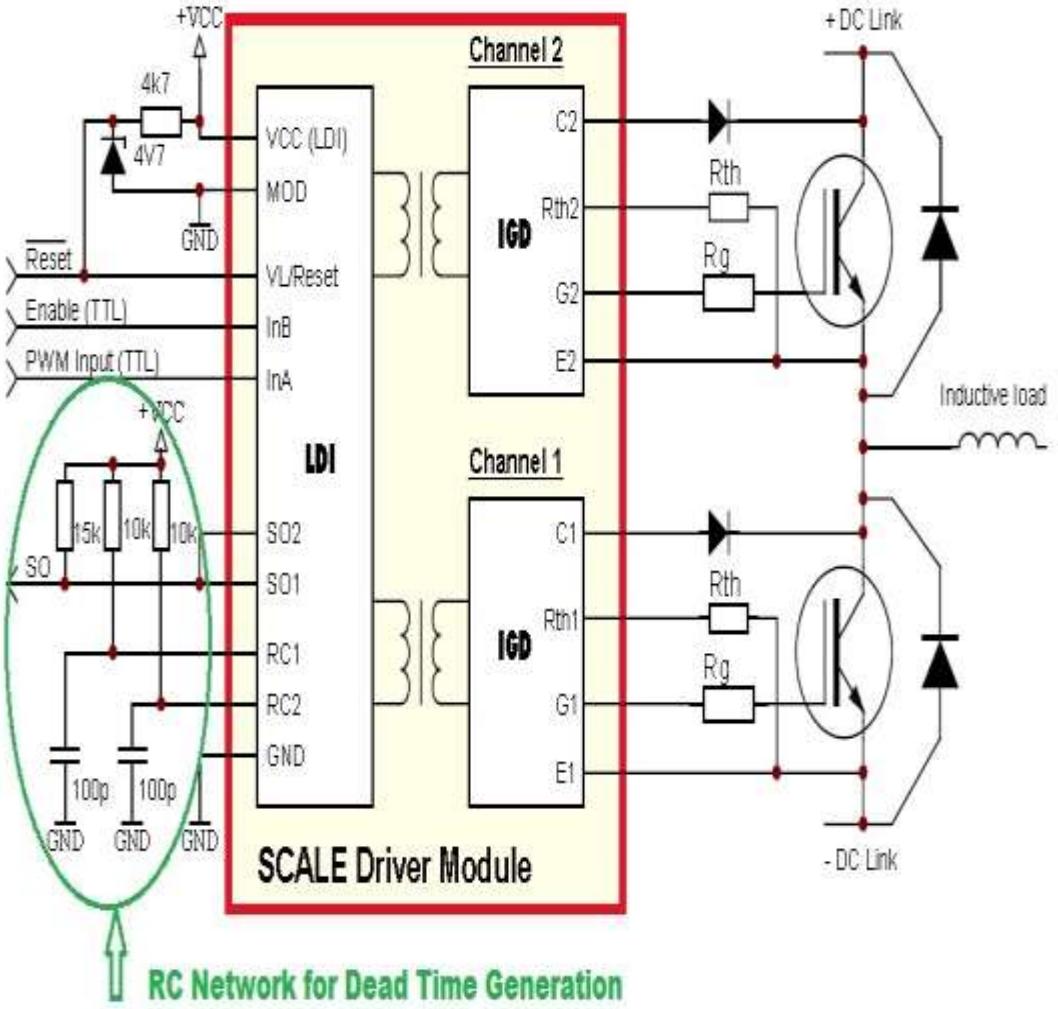


Figure 10.9 Pins RC1 and RC2 in the half bridge mode

Table 10.7 Values of the dead-times for the RC Network

R	C	typ. dead time
10k	47pF	≈ 200ns
10k	100pF	≈ 500ns
15k	120pF	≈ 1.1µs
22k	150pF	≈ 2.1µs
33k	220pF	≈ 4.6µs

The dead time shown in Table 10.6 produce the smallest scatter of dead times over the whole temperature range. Resistance values below 5 kΩ are not permissible.

In case of half bridge mode, the RC networks must be connected as shown in the Figure 10.9, by connecting the resistor to the VCC and the capacitor to the GND. In case of direct mode, all the RC networks are connected to GND.

vi. InA: In direct mode, the terminal InA drives channel 1 directly. The input A has a Schmitt trigger characteristic and corresponds to positive logic: a high level switches the power semiconductor ON and a low level switches the power semiconductor OFF. In half bridge mode, the PWM signals for the phase branch are connected to InA.

vii. InB: In direct mode, terminal InB controls the channel 2 directly. This input also has Schmitt trigger characteristics and corresponds to the positive logic (like InA). In half bridge mode, the release signal for the phase branch is connected to InB.

viii. MOD: This pin is used to select the operating modes of the LDI 001. The two operating modes are: half bridge and direct mode. In case of half bridge mode, the MOD pin is connected to GND and the pins 5 and 8 are connected to the RC networks (to enable dead time generation). In addition, in this mode, the inputs InA and InB are connected to the PWM signal and its release function respectively.

In case if direct mode, the MOD pin is connected to VCC and the pins 5 and 8 are connected to the GND (no need of dead time generation here!).If it is not connected to the GND, unexpected switching processes will result. There is no mutual influence between the two inputs InA and InB. The InA affects the channel1 and InB affects the Channel2. In each case, a high level at the input leads to switch ON of the corresponding IGBT.

Note: The direct mode is selected when the control electronics has already generated the dead times and a control signal is thus present for each semiconductor. In addition, in this mode, both the channels can be driven either simultaneously or in overlapping mode.

ix. **VDC:** This input supplies the internal DC-DC converter. It is recommended that a blocking capacitor be inserted between the VDC and GND.

10.6.7 Detailed Descriptions of the Pins on the Output side

Table 10.7 gives the description of the pins at the output side along with their pin numbers.

Table 10.8 Descriptions of the pins on the output side

Pin No	Designation	Function
13	-----	Free
14	G2	Gate channel 2
15	E2	Emitter channel 2
16	Rth2	Reference Resistor channel 2
17	C2	Collector Sense channel 2
18	----	Free
19	----	Free
20	G1	Gate channel 1
21	E1	Emitter channel 1
22	Rth1	Reference Resistor channel 1
23	C1	Collector Sense channel 1
24	----	Free

i. **G1 and G2 Gate Channel:** The pins G1 & G2 are the output of the gate drive. When the SCALE driver is supplied with 15 V, the gate is driven with +/- 15V. The negative gate voltage is generated internally. The maximum permissible gate current is found from the data sheet.

ii. **E1 and E2 Emitter Channel:** These pins are connected to the emitter or source terminal of the power transistor. This terminal is also used as the low end of the reference resistor Rth.

iii. **C1 and C2 Collector Sense Channel:** This terminal is used to measure the voltage drop across the turned ON power transistor in order to ensure the protection from short circuit and overload. It must be noted that it must never be connected directly to the drain or collector of the power transistor. A circuit with a high blocking diode Dm must

be included to protect the measuring the terminal from the high drain or the collector voltage of the turned OFF power element. The collector sense circuit for channel 1 & 2 are shown in the Figure 10.10.

iv. **Rth1 and Rth2 Reference Resistor:** A resistor is connected to this pin as reference. It defines the maximum voltage drop across the turned ON power transistor at which the protection function of the drive is activated. The protection function is always active when the voltage at collector sense terminal exceeds the voltage at the reference resistor terminal. The Voltage at the emitter terminal is taken as the reference potential. The Figure 10.10 shows the collector sense circuit showcasing the use of Rth and the current source of 150 µA present in the IGD module.

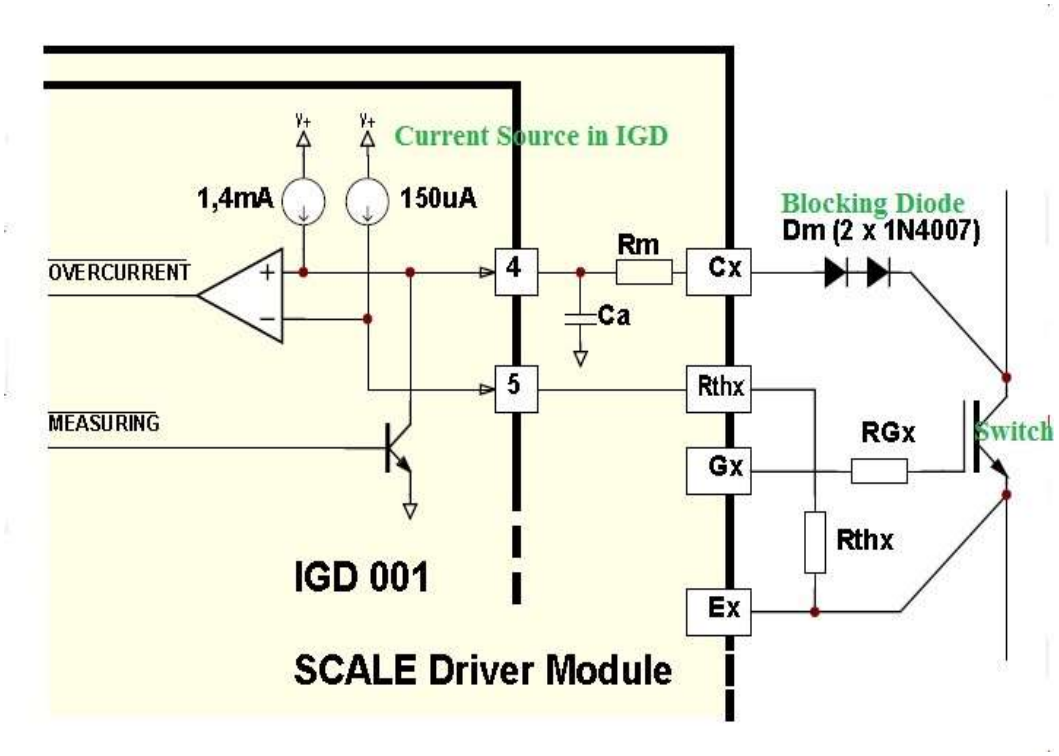


Figure 10.10 Collector sense circuit

The value of the reference resistor can be calculated as $R_{th}=\frac{V_{th}}{150\mu A}$,

where, V_{th} is the required threshold (here it is 5.85 V).

Therefore, $R_{th}=\frac{5.85}{150\mu A}=39K\Omega$.

10.6.8 State of the Protection Function

As shown in the Figure 10.9, there are two blocking diodes Dm. So the forward voltage drop of the two diodes is 1.2 V (2*0.6 V= 1.2 V). In addition, the voltage drop across the resistor Rm is found to be 250 mV. In addition, we know that the threshold voltage or the maximum allowable voltage across the switch is 5.85 V. Therefore, when the voltage across the switch exceeds than 4.4 V (i.e. 5.85 V - (1.2 V+250 mV)), the output of the comparator goes low and the over current error signal is thus received in the status acknowledgement pins and the driver blocks the further PWM pulses to the switch, by protecting it (happens when the protection function is activated).

Blocking Time Logic:

Every time an error (short circuit/ over-current error) and detected, a blocking time logic gets activated locally on the driver. When the error is detected, the error information is passed to the storage of LDI, whose status pins SO1 and/or SO2 become active LOW. After the status pins have gone LOW, the driver ignores any signals until the blocking time has elapsed. If no drive signal is applied, the error information continues to be stored in the LDI even after the blocking time. In this case, the error memory can be erased by briefly pulling the pin VL/Reset to GND. After the occurrence of short circuit fault, power semiconductor requires a “pause” in order to cool down before the next pulse is released, as shown in Figure 10.11

10.6.9 Concept driver board component list

Tables 10.8-10.10 give the list of components used to build the driver circuit. The PCB Board for the driver circuit was designed using ORCAD software, and Figure 10.12 shows the circuit diagram of the same. Figure 10.13 shows the developed driver module.

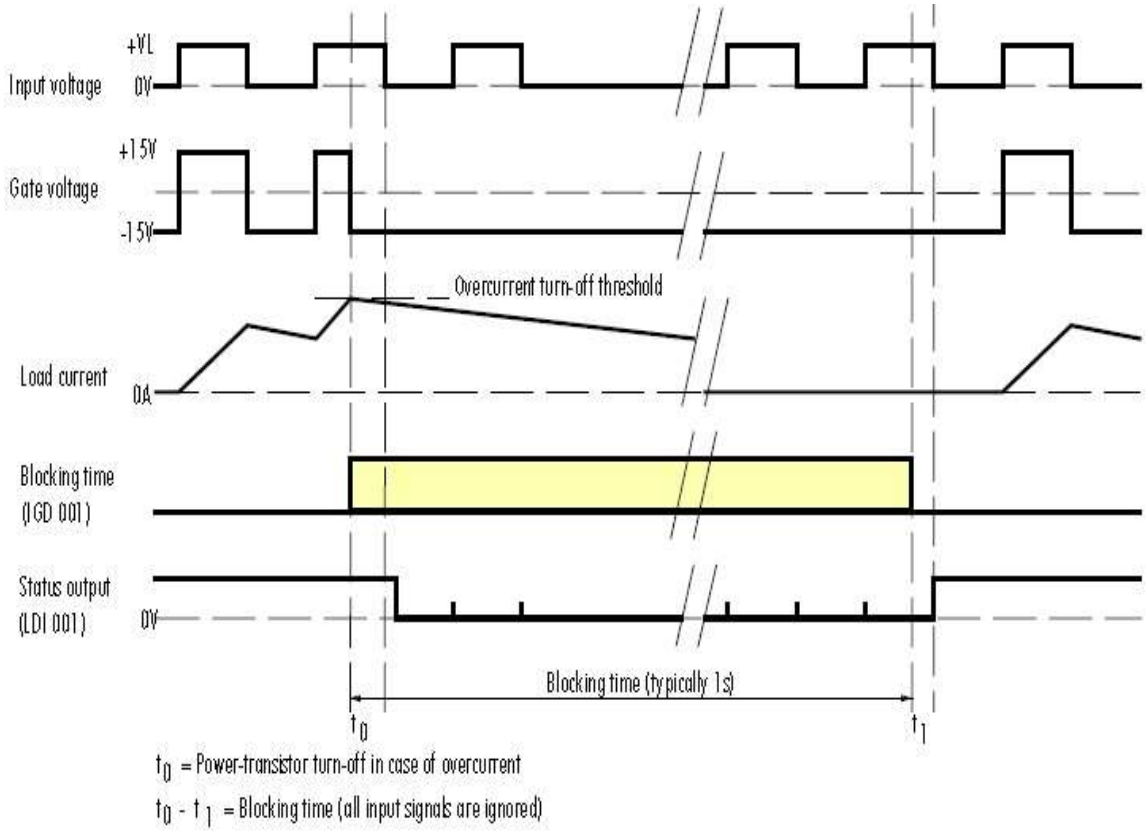


Figure 10.11 Short-circuit and over-current protection/ function of the blocking time

Table 10.9 List of components on the input side

Label	**Value**	**Purpose**	**Qty.**
C1, C3	0.1u	Power surge arrest	2
C2, C4	short	--	-
R3	1 kΩ	V_L pull-up resistance (to V_{DD})	1
R2	180 kΩ	Status pull-up resistance (to V_{DC})	1
R7	short	Mode pull-up resistance, connect to V_{DD}. Jumper J4 need not be soldered if R7 is shorted.	--

R10, R11	open	-	-
R12, R13	6.8 kΩ (dull)	Voltage dropping resistor for LED	2
LD1	Small LED	To indicate if V_{DC} is available to board	1
LD2	Small LED	To indicate if V_{DD} is available to board	1
J5	2-pin connect	V_{DC} supply point	1
J6	2-pin connect	V_{DD} supply point	1
J7	3-pin connect	Logic level signal (PWM)	1

Table 10.10 List of components on the output side

LABEL	VALUE	PURPOSE	Qty.
D4, D5	18 V	Gate protection Zener diodes	2
D6, D7	18 V	Gate protection Zener diodes	2
R6, R9	33 Ω (1/2 W)	R_G, Gate resistance	2
R5, R8	22 kΩ (1/2 W)	R_{th}, over-current protection in collector sense circuit	2
D2, D3	FR107	Reverse current protection in collector sense circuit	2
J1, J2	3-pin connect	Driver Output connectors (order from jumper number → CEG)	2

Table 10.11 List of components in the status circuit

Label	Value	Purpose	Qty.
R1	100 Ω	Reset transistor's base resistance	1
Q1	BC547	Reset transistor	1
D1	FR107	Bypass diode across reset transistor	1
R4	180 kΩ	Status pull-up resistance (to V_{DD})	1
J4	3-pin connect	Mode setting (not required as R7 is shorted)	1
J3	6-pin connect	Digital logic input side connector for Status and Reset	1

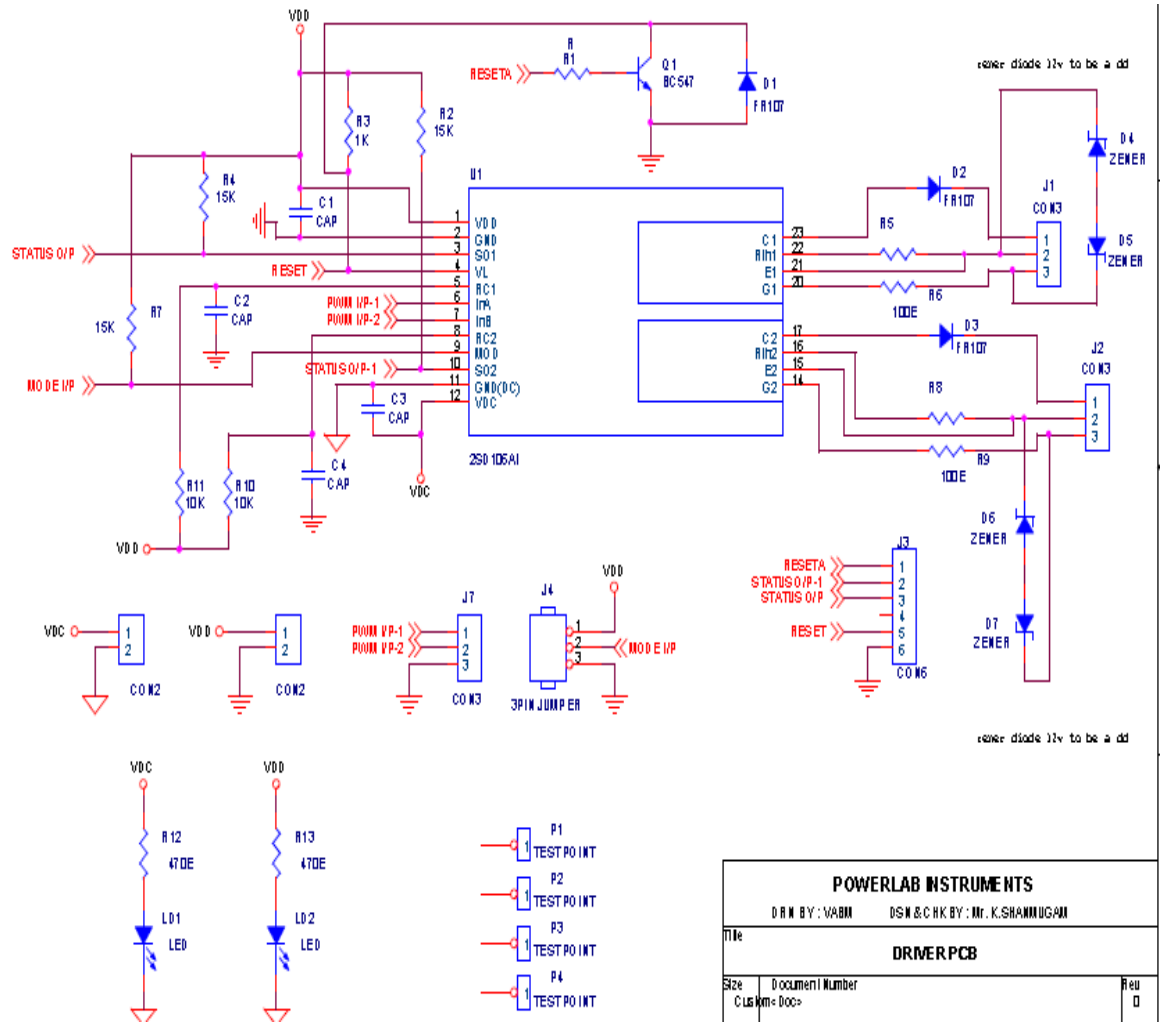


Figure 10.12 Circuit Diagram of the driver module

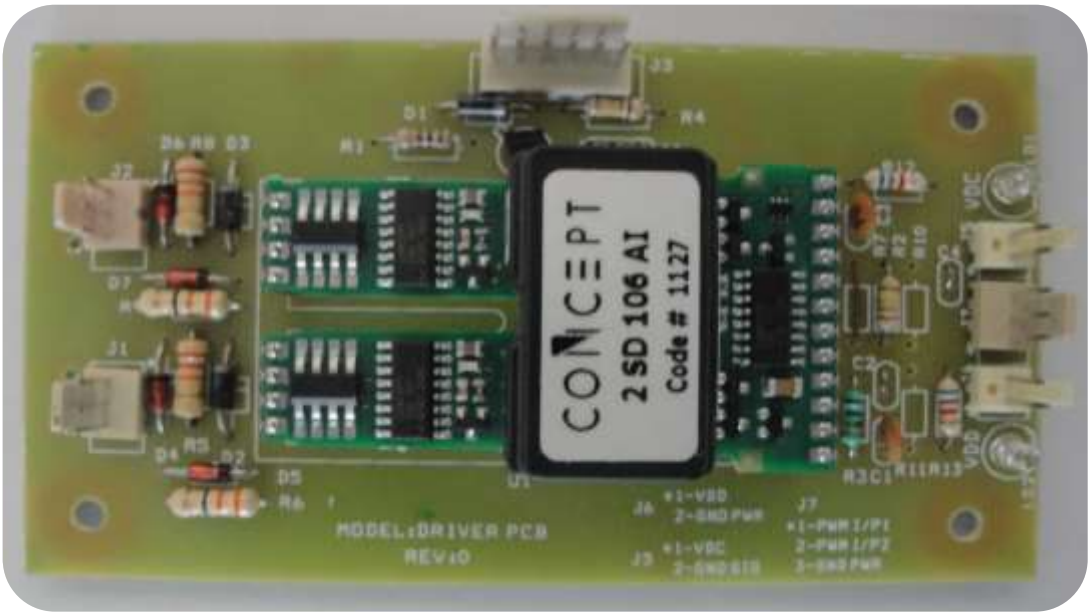


Figure 10.13 Concept Driver Module

10.7 CLAMP CIRCUIT – MATRIX CONVERTER PROTECTION

The conventional low frequency diode fails to clamp voltage spikes that appear during the operation of matrix converter. Instead, the high frequency diode - MUR 860 is used in the clamp circuit. The clamp capacitor of 1100 µf and a discharge resistance of 100 ohms were used in the clamp circuit for the protection of the matrix converter. The clamp circuit setup is shown in Figure 10.14.

Figure 10.14 Matrix converter clamp circuit

10.8 INPUT FILTER CIRCUIT

The input filter circuit consist of an LC circuit in all the three input phases. The value of the filter inductance is 4 mH and that of the filter capacitance is 20 µf. Figure 10.15 shows the setup..

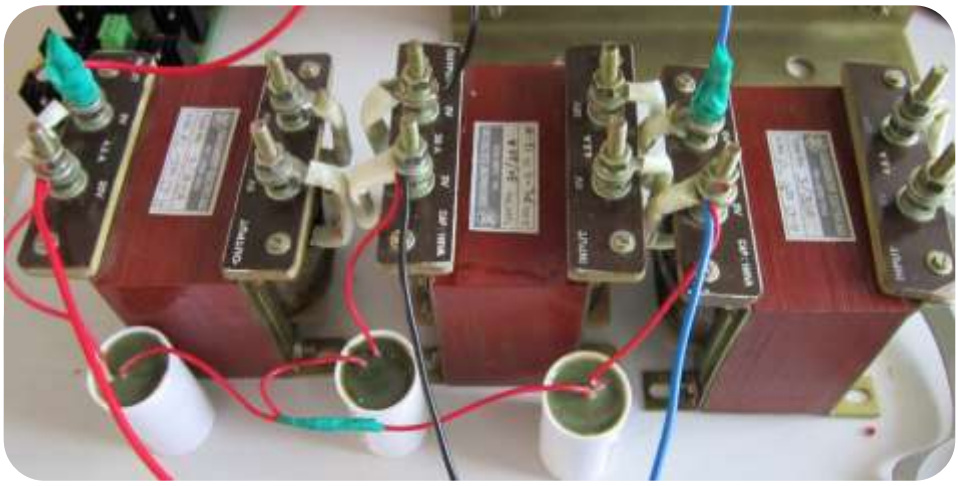


Figure 10.15 Input filter circuit

10.9 COMPARATOR CIRCUIT – GENERATING INTERNAL CURRENT REFERENCE

The reference current for the matrix converter to maintain unity power factor is generally the phase voltages itself. This requires three voltage transducers to sense the input phase voltage and three ADC channels to convert the information into a digital form.

A new technique was used to eliminate the sensors and ADC channels required, as described above. The comparators are used to generate two digital signals to detect the most positive voltage and the most negative voltage instances. The method to generate the reference current internally from the obtained digital signals is described in Chapter 8. Figure 10.16 shows the setup. .

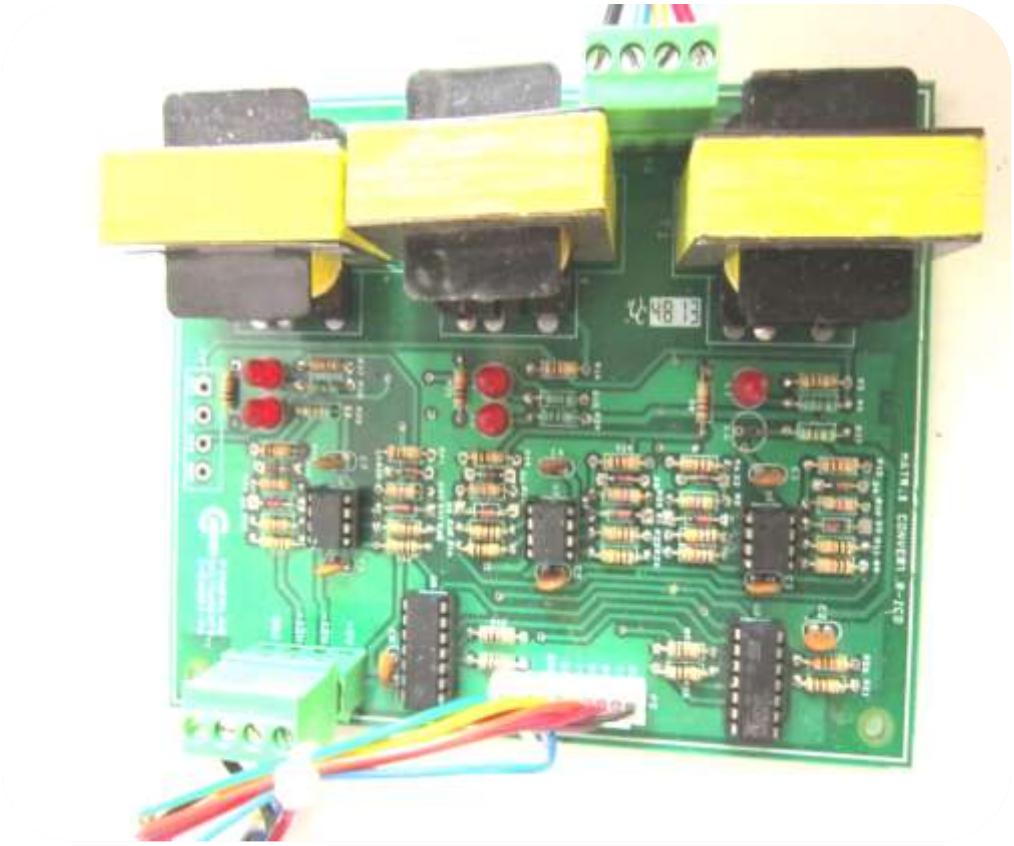


Figure 10.16 Comparator circuit for the generation of the current reference internally

Three 230 V / 9 V, 100 mA transformers are used to step down the phase voltages and applied as inputs to the IC 741 comparators. The outputs of the comparators are given to the FPGA through the buffer IC HCF4081BE.

10.10 FOUR-STEP COMMUTATION CIRCUIT-OUTPUT CURRENT DIRECTION SENSE CIRCUIT

The current direction sensing circuit consists of two anti-parallel diodes in series with the load. The voltage across the diodes is fed to a comparator operated as the zero-crossing detector. The output of the comparator gives the information about the direction of the current in each phase, which is the control signal for the four-step commutation sequencer. Figure 10.17 gives the direction of the current.

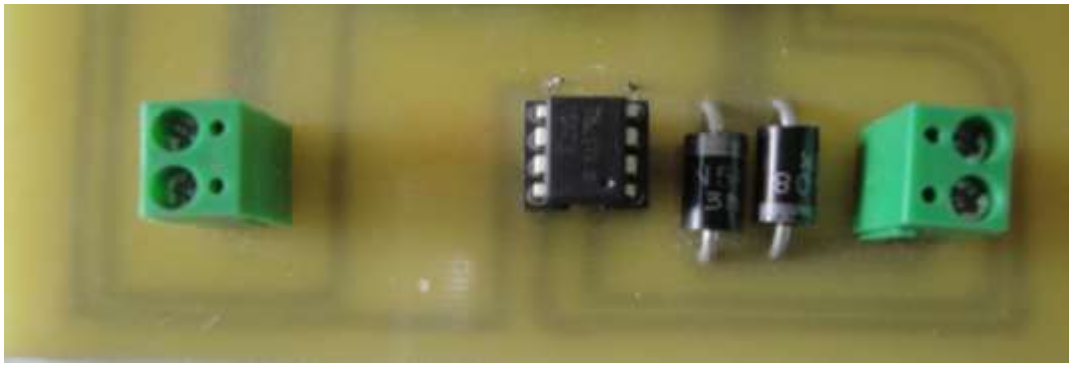


Figure 10.17 Current direction sense circuit

The flow of positive current at the output terminal leads to a voltage drop of +0.7 V across the anti-parallel diode setup and -0.7 V when the direction of output current is negative. The comparator's reference signal is taken as the ground so that the output is +15 V for a positive diode drop voltage and -15 V for a negative diode drop voltage. The output of the comparator is processed through a diode and a level converter so that the digital output is 3.3 V for positive current and 0 V for negative current. This digital information is used in the FPGA for performing the four-step commutation. Figures 10.18 and 10.19 shown the output of the four-step commutation when the current is positive and negative respectively.

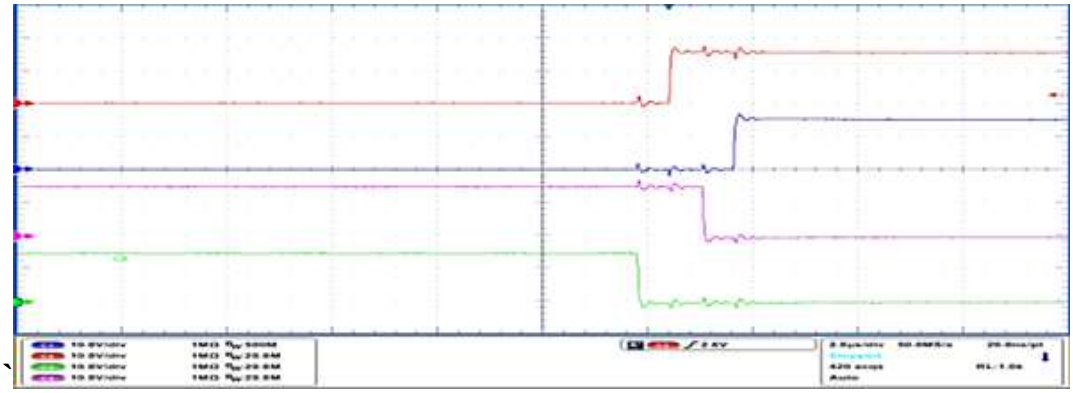


Figure 10.18 Commutation sequence when the current direction is positive

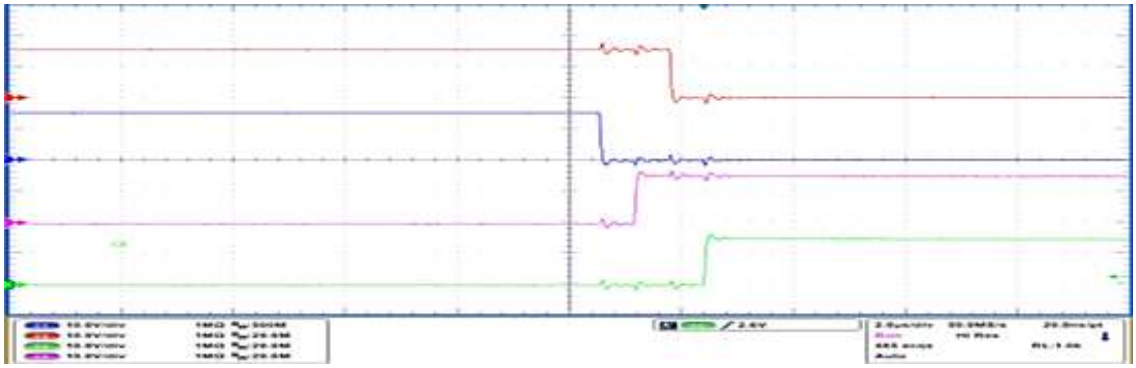


Figure 10.19 Commutation sequence when the current direction is negative

10.11 POWER SUPPLY UNIT (±15 V, 5 V)

The auxiliary regulated power supply of ±15 V is required to power the Concept SCALE driver and the comparators used in the circuits. A regulated power supply of 5 V is required to power the FPGA Board. Figure 10.20 shows the setup of the power supply.

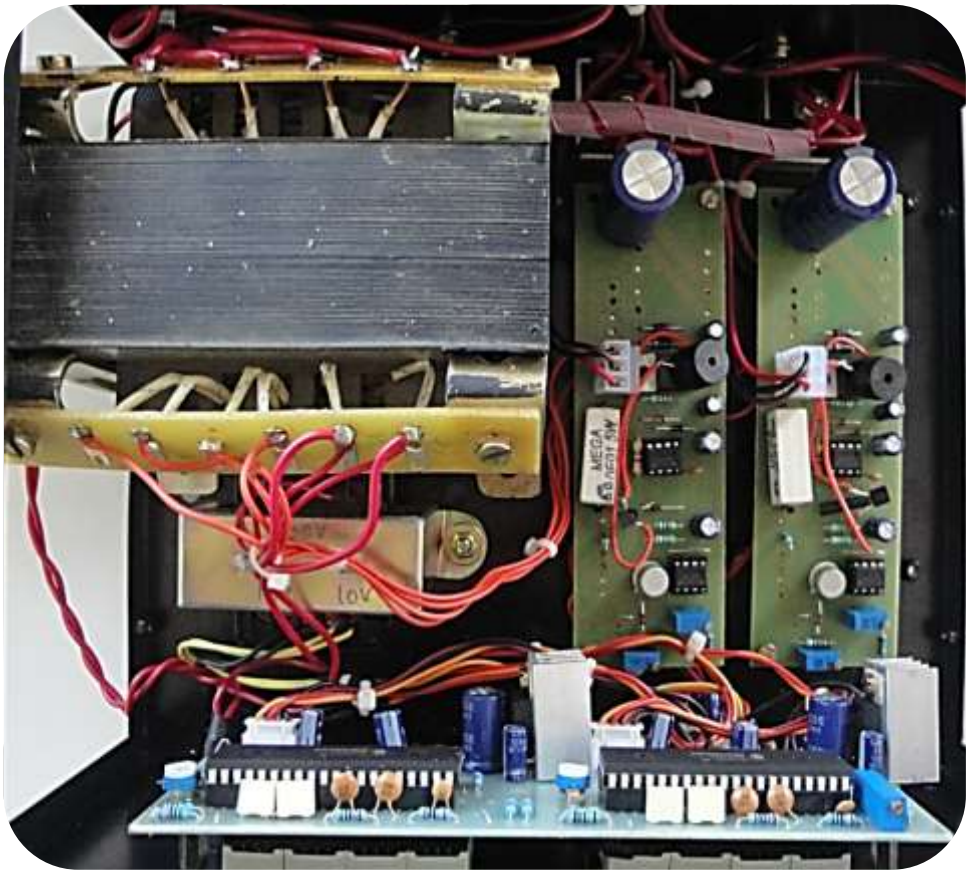


Figure 10.20 Regulated power supply unit

10.12 FPGA CONTROLLER UNIT-SPARTEN 3E (NEXYS 2)

The SPARTEN 3E FPGA is used as the digital controller in this work. Some of the features of this IC are that it contains 20 multiplier units that can perform parallel computations, 232 I/O ports for external data communication, and 500 K gates for implementing the control and modulation logic. The Nexys 2 Kit is designed to receive 16 analog inputs through the 4 PMOD ports available with the help of the Digilent PMOD AD1 Analog to Digital Converter (ADC). The firing pulses for the matrix converter are provided through the Hirose connector port of the Nexys 2 kit. The coding of the controller is performed using the VHDL Language. Due to the difficulty in writing a VHDL code for the matrix converter DSVM algorithm and the rotor side controller algorithm, the coding method adopted is the model-based design.

10.12.1 Model based design of the FPGA

Wherever the difficulty of coding exists, the model-based design is the suggested technique for coding. In this technique, a graphical interface is used for the design of the code and the software used to design the graphical interface is provided with a compiler to generate the appropriate code. In this work, to avoid the use of additional softwares, Matlab software is integrated with the Xilinx System Generator Toolbox to provide the graphical user interface in the Matlab environment. This technique for designing does not require the use of additional softwares.

10.12.2 Configuration of Inputs and Outputs for the Controller

The controller is designed to accept four Analog inputs (speed, voltage, active power and reactive power) through two PMOD AD1 modules. The three digital inputs determine the load current direction for providing four-step commutation. The two digital input of the controller are used for the reconstruction of the reference current signal for the matrix converter DSVM algorithm. The eighteen digital outputs trigger the matrix converter to control the stator power. Figure 10.21 presents the block diagram representation of the input and output signals to the FPGA. Figure 10.22 shows the controller along with the PMOD AD1 module.

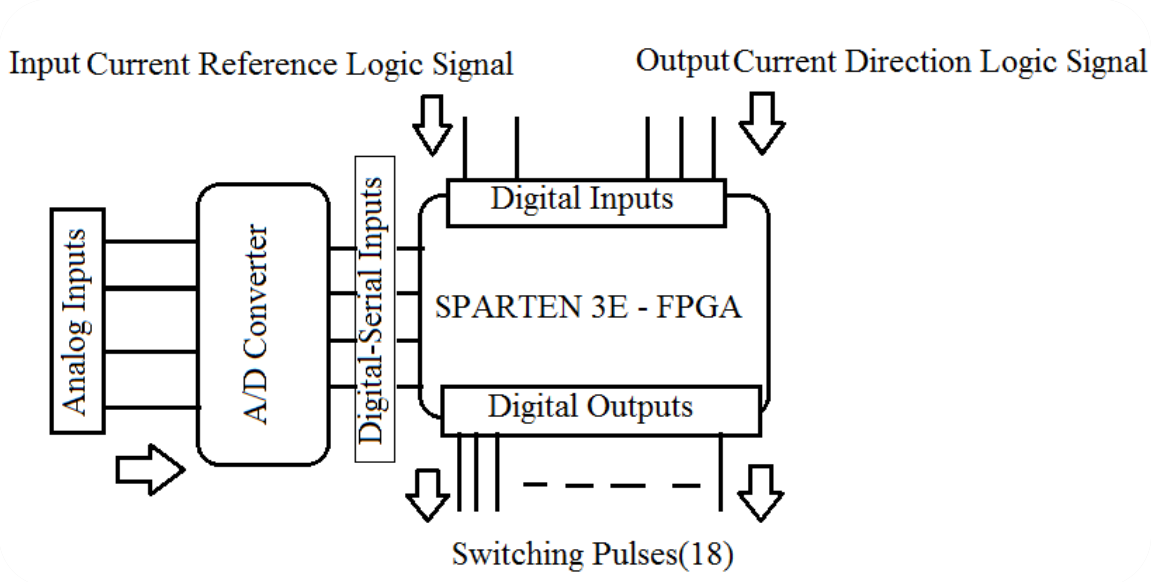


Figure 10.21 Block diagram of the input and output signals to FPGA

Figure 10.22 FPGA controller unit - Sparten 3E

Figure 10.23 shows the switching signals produced by the FPGA controller for switching the matrix converter. The pulses that are generated by the FPGA at the level of 3.3 V and converted to the 15 V level and passed to the driver stage (Concept 2SD) to improve the current capability of these signals before triggering the IGBTs of the matrix converter.

10.13 ANALOG TO DIGITAL CONVERTER – PMOD AD1

The ADC board (the AD1™) converts the signals at a maximum sampling rate of one million samples per second, fast enough for our applications.
The important features of PMOD AD1 include the following

1) Two AD7476A 12-bit A/D converter chips
2) 2-pole Sallen-Key anti-alias filters
3) Simultaneous A/D conversion channels at up to one MSa per channel

The AD1 converts an analog input signal ranging from 0-3.3 volts to a 12-bit digital value in the range 0 to 4095. The AD1 has two simultaneous A/D conversion channels, each with a 12-bit converter and filter. Each channel can sample a separate stream of analog signals. The AD1 can also convert a single stream of analog signals using only one channel. Each channel has two 2-pole Sallen-Key anti-alias filters with poles set to 500 KHz. The filters limit the analog signal bandwidth to a frequency range suitable for sampling rate of the converter. Figure 10.24 gives the AD1 module and its internal block diagram.

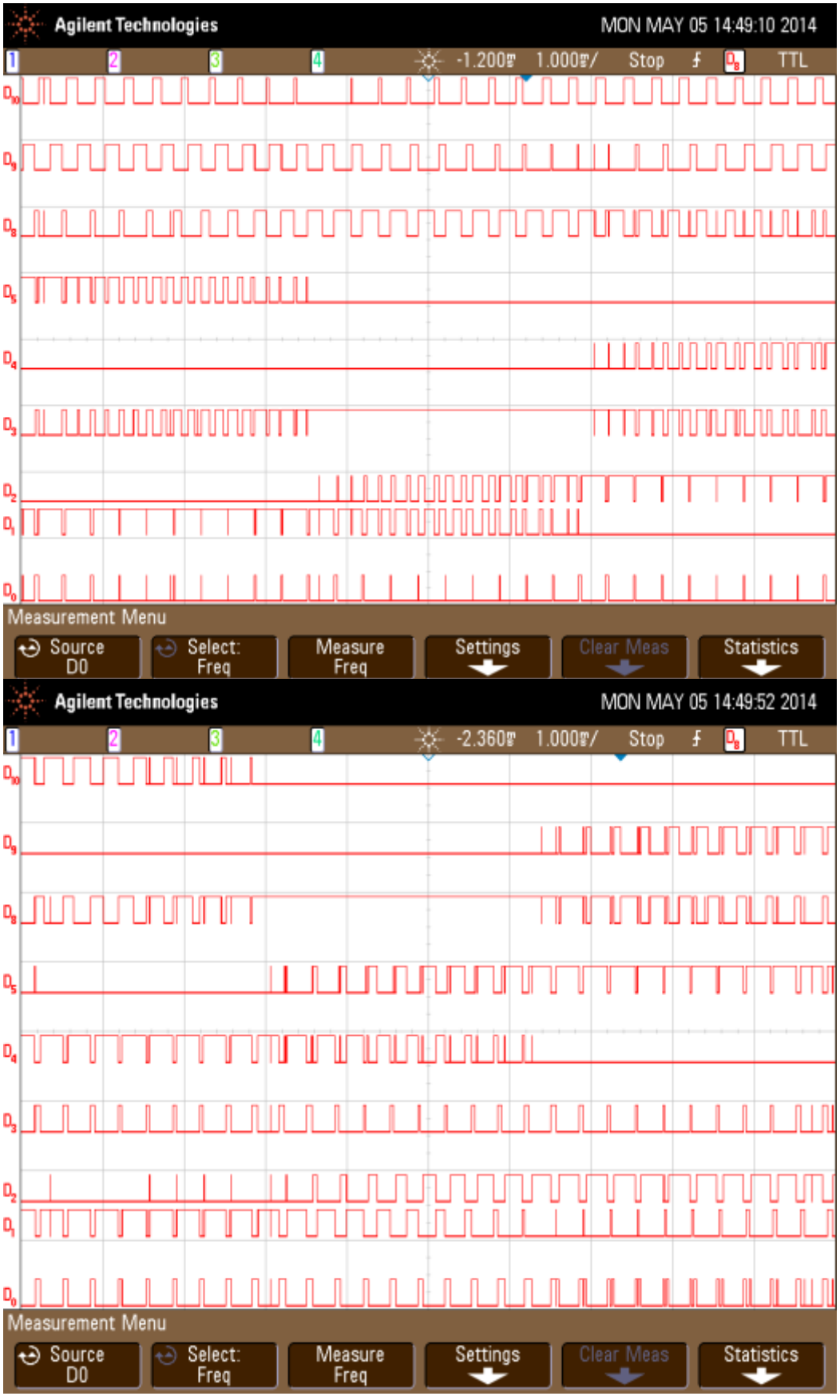


Figure 10.23 Eighteen switching pulses for the matrix converter generated from the FPGA

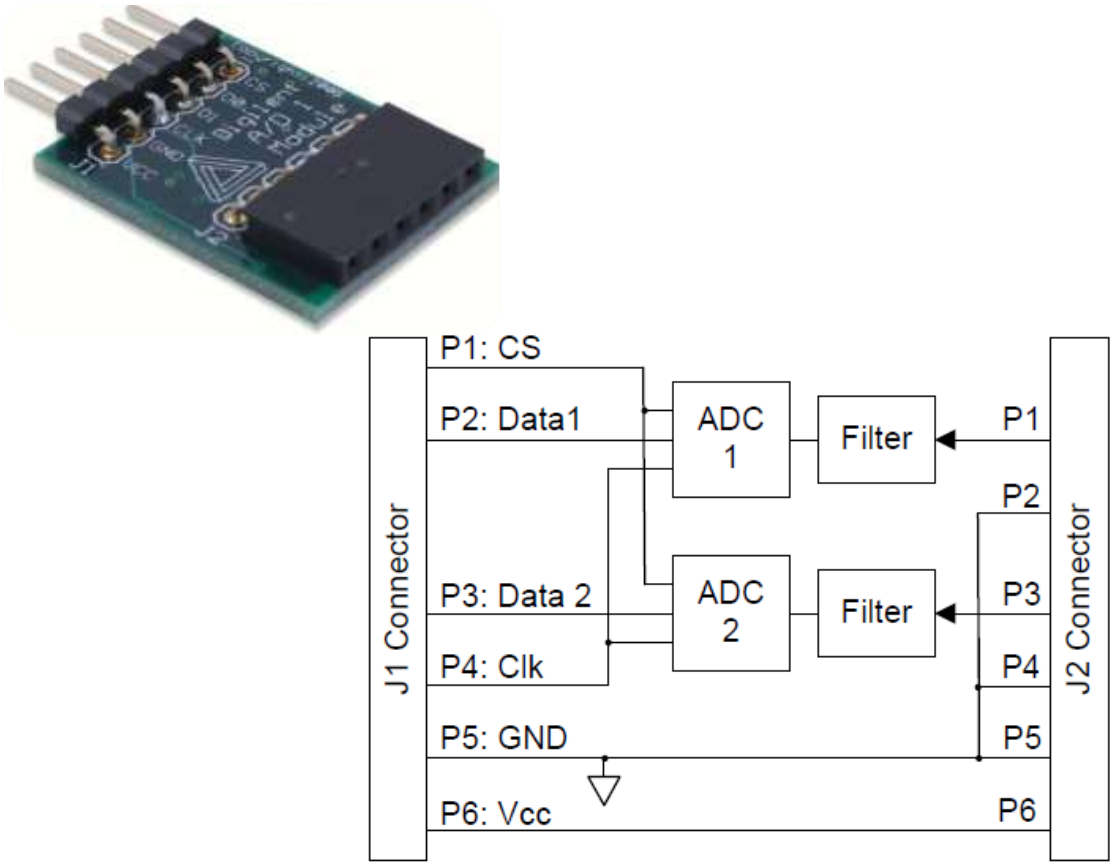


Figure 10.24 PMOD AD1 and the internal block diagram

10.14 POWER TRANSDUCERS AND VOLTAGE TRANSDUCER- MECO

The MECO Make active, reactive power and voltage transducers as shown in Figure 10.25 were used to measure the active power, reactive power and input voltage magnitude. The transducers are supplied with the auxiliary supply of (0-230 V) AC for the operation of the transducers. The signals received from the transducer ranging from (0-5) V level were converted to into 3.3V level to be processed by the ADC - PMOD AD1. These signals were used by the Rotor side converter algorithm to generate an appropriate reference to the DSVM algorithm of the matrix converter.

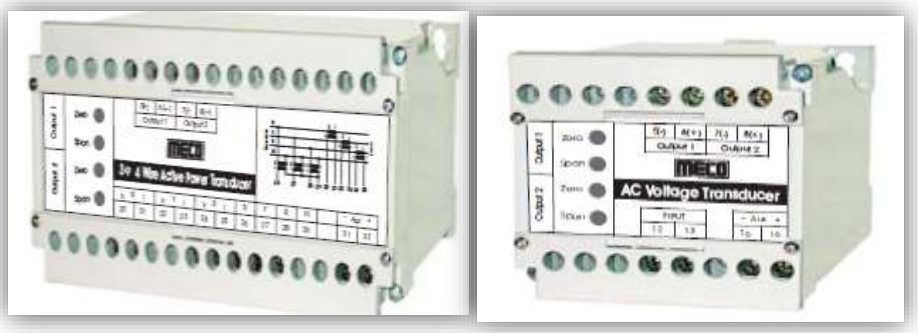


Figure 10.25 Meco power and voltage transducers

10.15 PROXIMITY SENSOR–SPEED SENSING

The proximity sensor is used to detect the speed of the rotor mounted close to the rotor. The sensor generates one pulse per revolution, corresponding to the speed of the rotor the time period between two pulse changes. These digital pulses from the sensor unit are processed by the FPGA using the algorithm explained in Chapter 9 to detect the speed of the rotor. Figure 10.26 shows the proximity sensor used in this work .

He 

Figure 10.26 Proximity sensor Mounted near the rotor

10.16 WORKING PRINCIPAL OF THE PROTOTYPE IMPLEMENTED

Section 10.3 to 10.16 describe the interconnections of the various units described in sections 10.3 to 10.16 are presented as a block diagram in Figure 10.27.

The action performed by the rotor controller.

The power output of the stator (active and reactive) is sensed using a power transducer and the analog information is converted into a digital output and processed in the FPGA. In a similar fashion, the voltage magnitude and the speed information are converted into a digital information and sent to the FPGA for processing. The FPGA with the information of speed determines the slip and with the magnitude of the stator voltage and the determined slip estimates the rotor voltage. The information of stator active power and the reactive power is used to determine the error in power from the predefined reference power value. This error is used by the two Digital PI controllers to determine the correction factor to be applied to the determined rotor voltage. The new reference rotor voltage signal to be injected into the rotor circuit for the control of stator power is passed to the DSVM algorithm of the matrix converter.

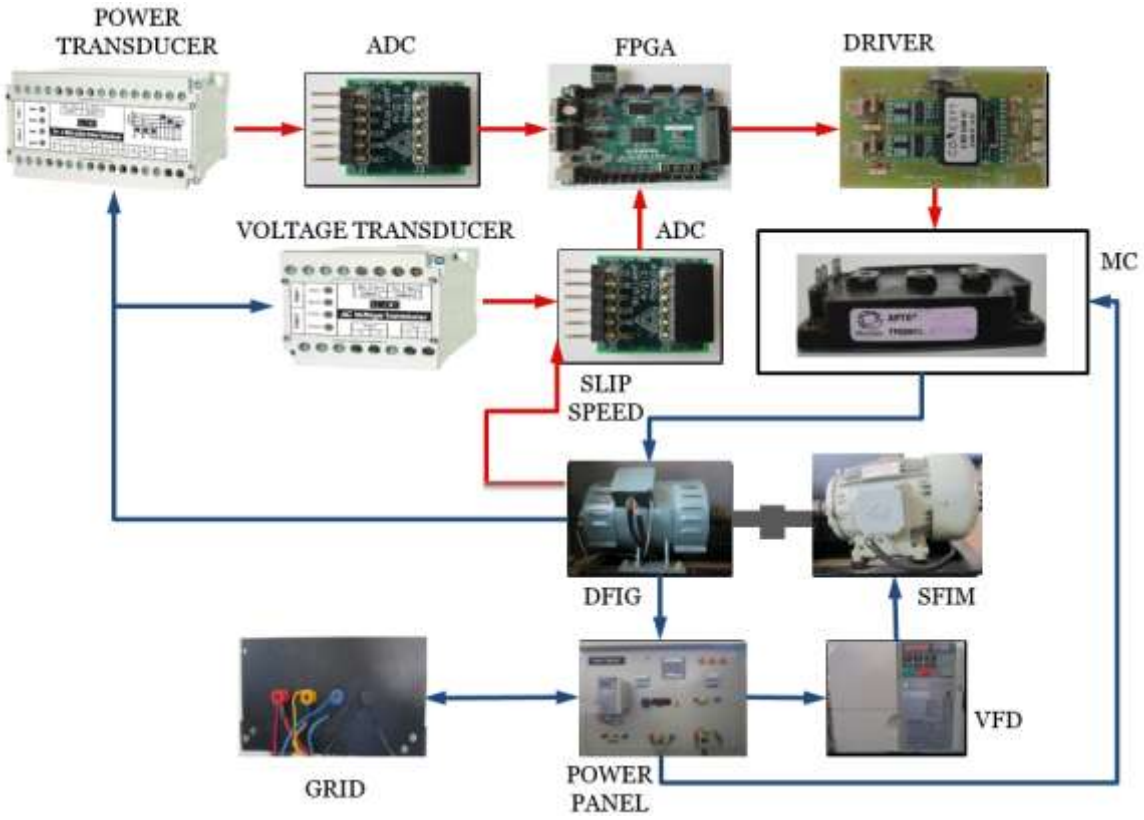


Figure 10.27 Block Diagram Representation of Interconnection of various units

The action performed by the DSVM algorithm is explained below in detail.

The reference rotor voltage signal generated by the rotor side controller is taken as the output voltage reference of the matrix converter. The input current reference generated from the digital signals of the comparator as explained in Chapter 8 is taken as the input current reference of the matrix converter. To both of these reference signals, the DSVM algorithm applies the ABC to α-β transformation and determines the angle and the sector in which the reference signals are currently present. Finally the DSVM algorithm determines three appropriate switching vector and their time period of application (duty cycle) for both the reference signals.

Finally the matrix converter is switched to generate the rotor voltage signal of required magnitude and frequency as demanded by the rotor controller algorithm. The DSVM algorithm generates the required output voltage and the required power factor at the input. The matrix converter setup is shown in Figure 10.28 and the complete prototype of the work is shown in Figure 10.29.

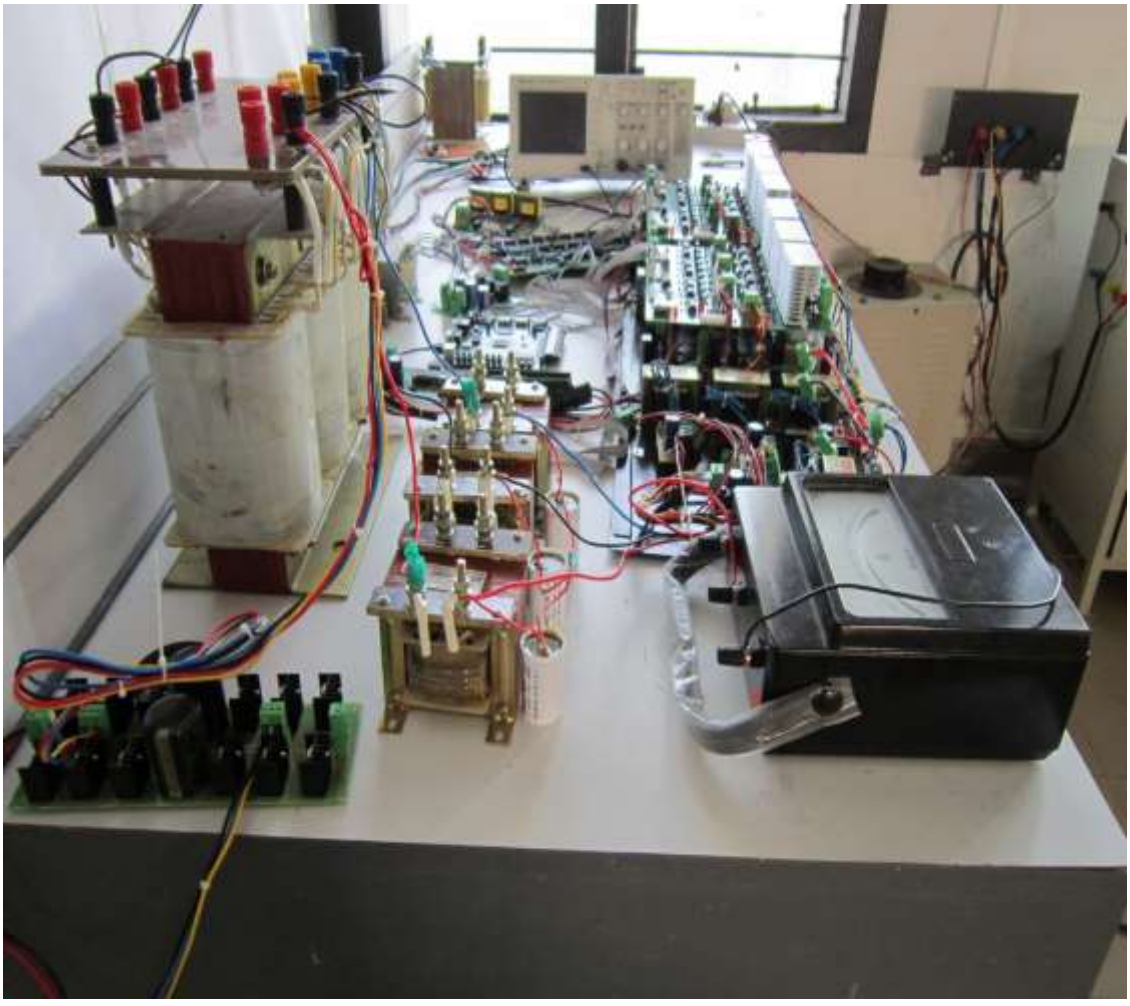


Figure 10.28 Matrix converter prototype setup

Figure 10.29 Complete prototype including Matrix converter and DFIG

10.17 DISCUSSION ON THE RESULTS

The output phase voltage of the matrix converter operated at a switching frequency of 3 kHz with a modulation index of 0.8 is shown in Figure 10.30. The output current and the input current of the matrix converter are shown in Figure 10.31 and 10.32 respectively. The input current which was expected to be sinusoidal as shown in the simulation results were found to be distorted to a greater extent because of the four-step commutation sequencer and the commutation law for the readjustment of duty cycle. In addition, due to the practical implementation of the matrix converter is not in part to the industrial standards. The output current is found to be more sinusoidal when compared to the input current of the matrix converter.

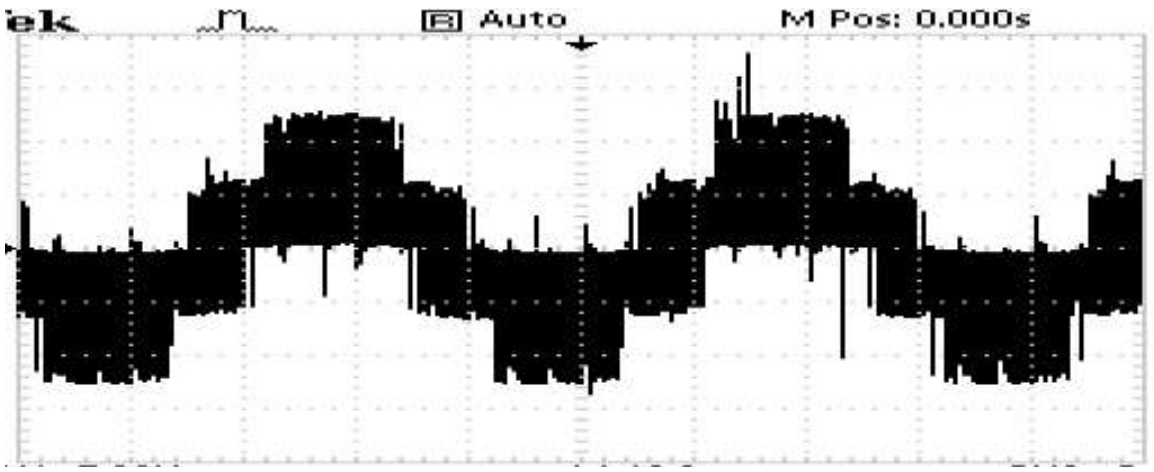


Figure 10.30 (a) Output Phase voltage of matrix converter with RL load
(SCALE –Y axis 50 /Division & X axis 0.01/ Division)

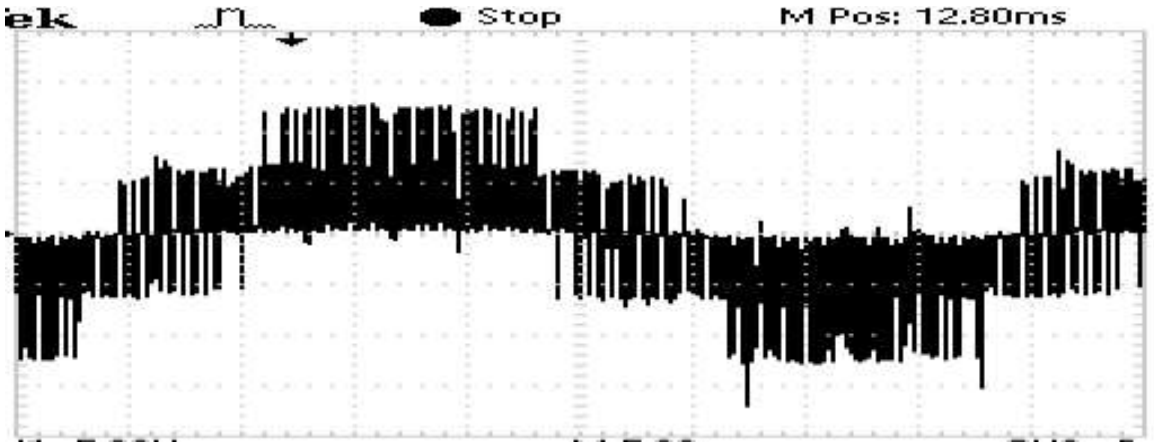


Figure 10.30 (b) Output phase voltage of matrix converter with RL load – Enlarged
(SCALE –Y axis 50 /Division & X axis 0.005/ Division)

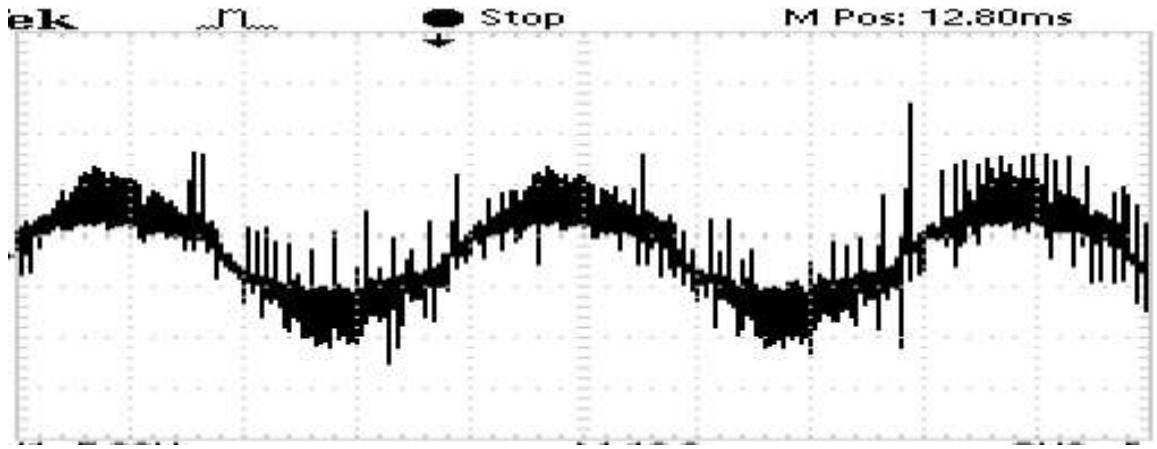


Figure 10.31 Input current of matrix converter with RL Load
(SCALE –Y axis 3 /Division & X axis 0.005/ Division)

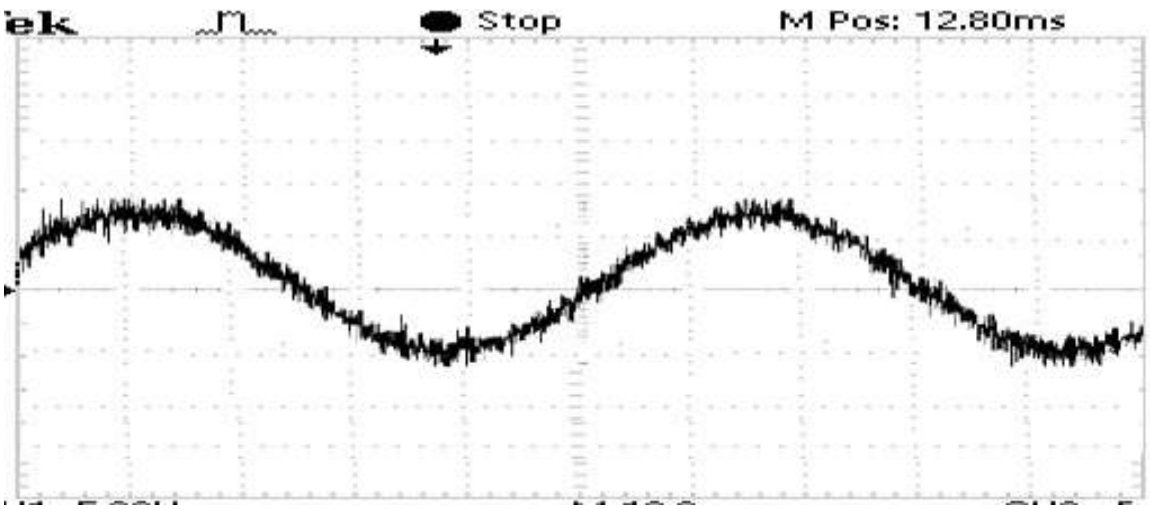


Figure 10.32 Output current of matrix converter with RL Load
(SCALE –Y axis 3 /Division & X axis 0.08/ Division)

The matrix converter output was connected to the rotor of the DFIG and the control of stator power was performed. The following results were obtained. The designed controller was able to perform stator power control more satisfactorily.

The matrix converter output line voltage that was applied to the rotor of the DFIG is shown in figure 10.33. The input currents and the output currents of the matrix converter when connected to the DFIG are shown in Figure 10.34 and 10.35 respectively.

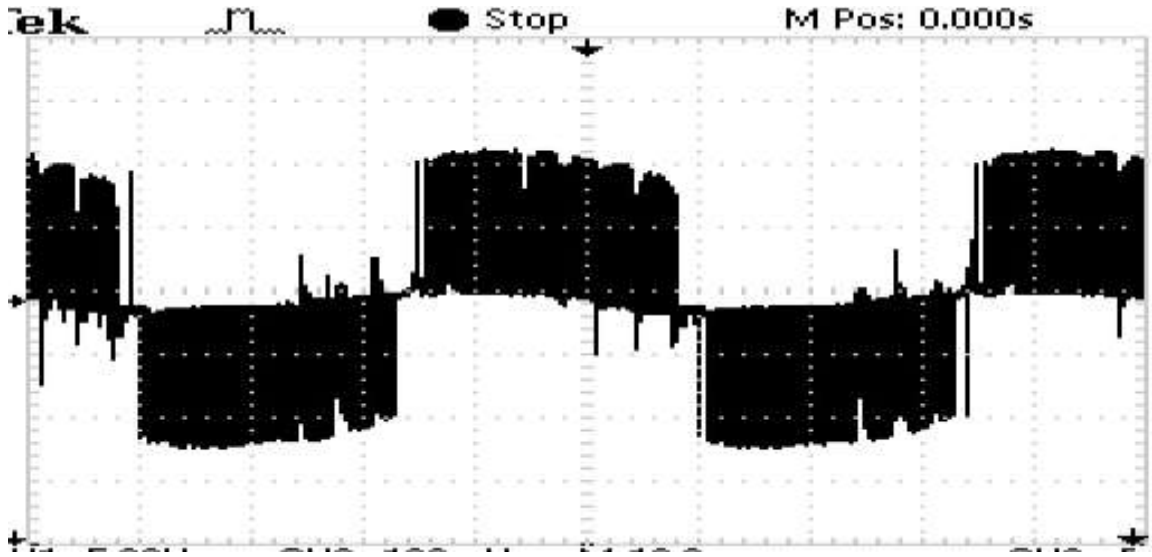


Figure 10.33 (a) Output Line Voltage of matrix converter applied to the rotor of the DFIG

(SCALE –Y axis 100/Division & X axis 0.1/ Division)

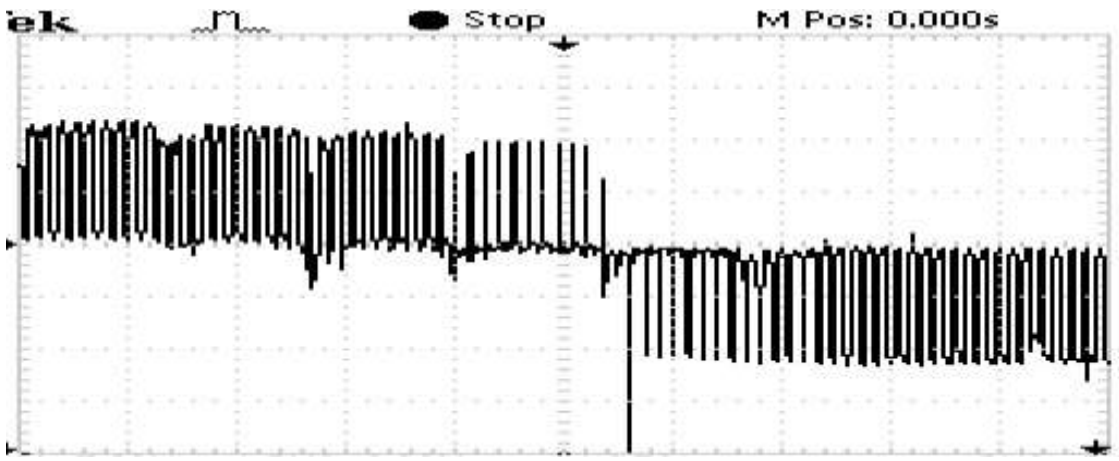


Figure 10.33 (b) Output Line Voltage of matrix converter applied to the rotor of the DFIG – Enlarged

(SCALE –Y axis 100/Division & X axis 0.05/ Division)

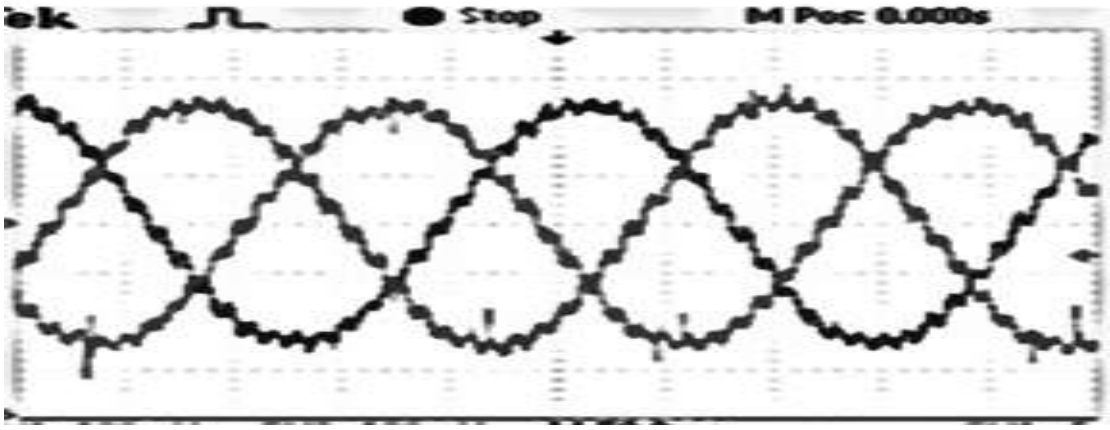


Figure 10.34 Output currents of matrix converter injected into the rotor of the DFIG

(SCALE –Y axis 0.4/Division & X axis 0.1/ Division)

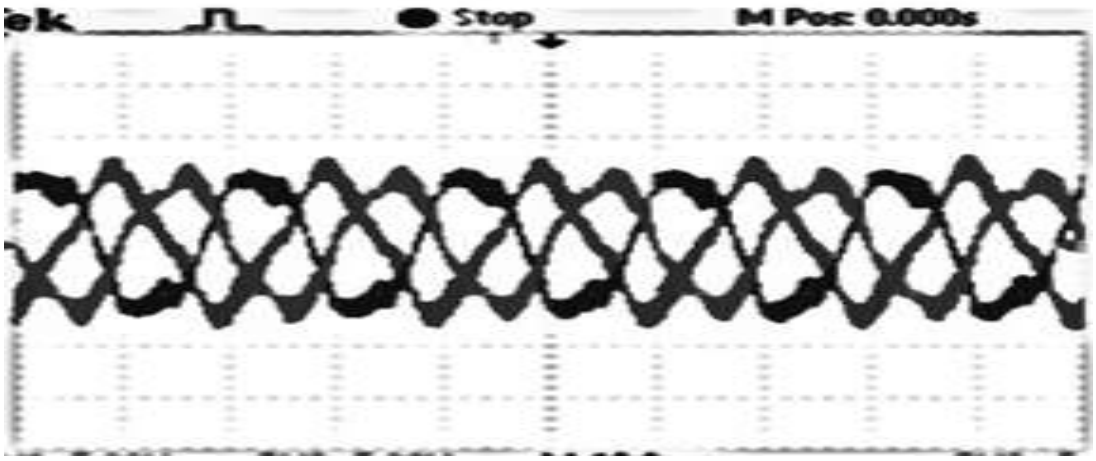


Figure 10.35 Input currents of matrix converter when connected to the rotor of the DFIG

(SCALE –Y axis 0.4/Division & X axis 0.01/ Division)

The reference active power and reactive power setting were kept at 1 KW and 0 KVAR respectively in the VHDL code of the FPGA controller. The FPGA controller used two digital PI controllers to minimize the error between the actual power and the reference power under all modes of operation. The prime mover was operated at 1560 rpm (super synchronous mode) and 1470 rpm (sub synchronous mode) using the YASKAWA VFD. Under both modes of operation the FPGA controller was found capable to control the power in the stator as requested. The active power transducer and reactive power transducer output at the stator for both super synchronous mode of operation and sub synchronous mode of operation is presented in Figure 10.36 and 10.37 respectively.

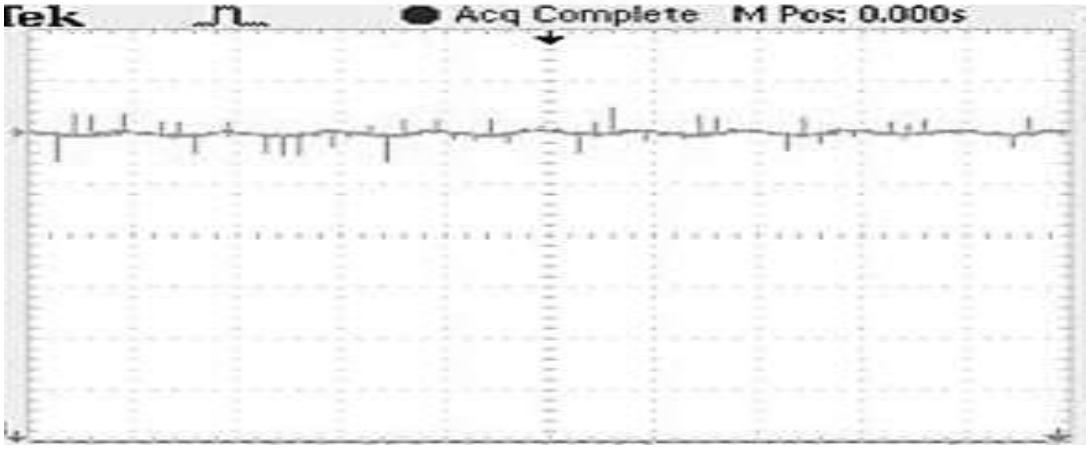


Figure 10.36 (a) Active power delivered in the super synchronous mode of operation
(SCALE –Y axis 0.5/Division & X axis 1/ Division)

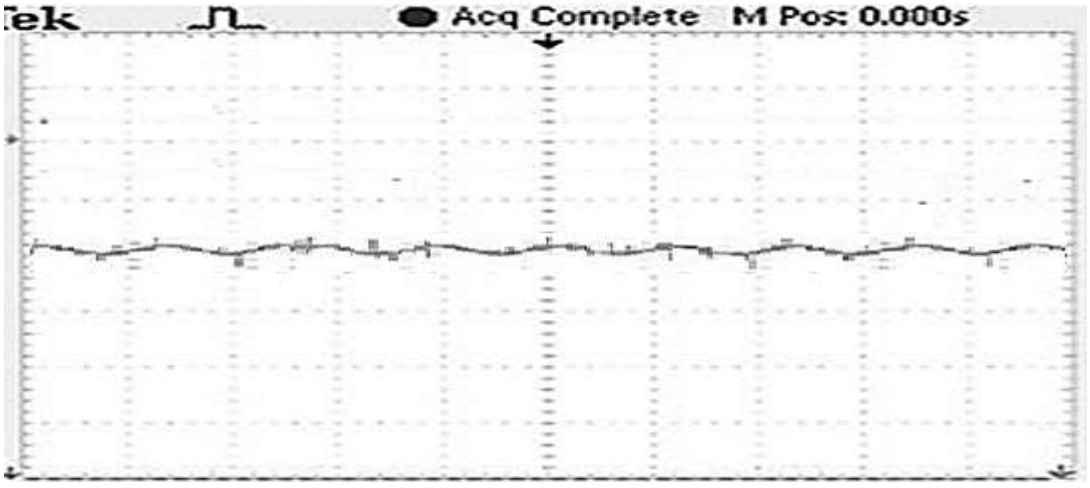


Figure 10.36 (b) Reactive power delivered in the super synchronous mode of operation
(SCALE –Y axis 0.5/Division & X axis 1/ Division)

The active power output under the sub synchronous mode of operation was found to be more oscillatory when compared to the super synchronous mode of operation as seen in Figure 10.37.

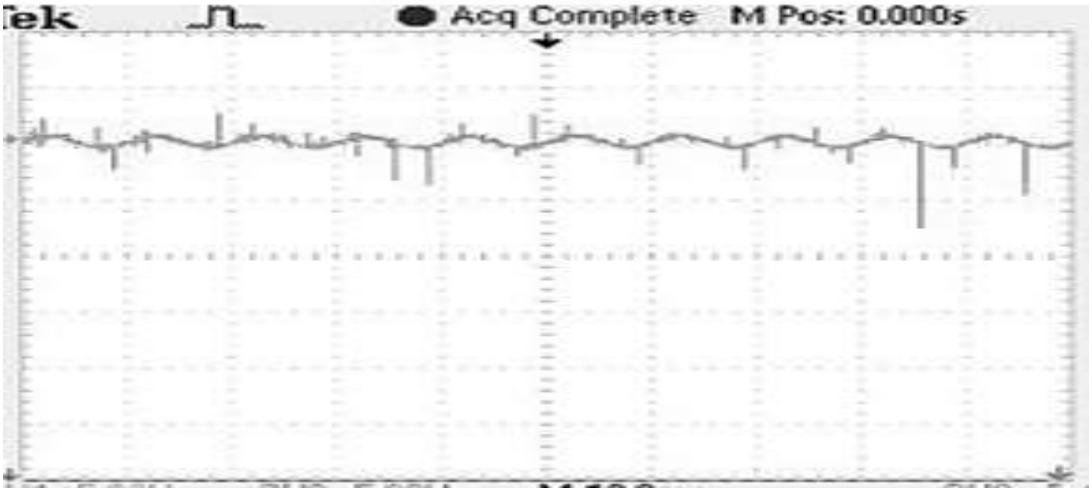


Figure 10.37 (a) Active power delivered in the Sub Synchronous mode of operation
(SCALE –Y axis 0.5/Division & X axis 1/ Division)

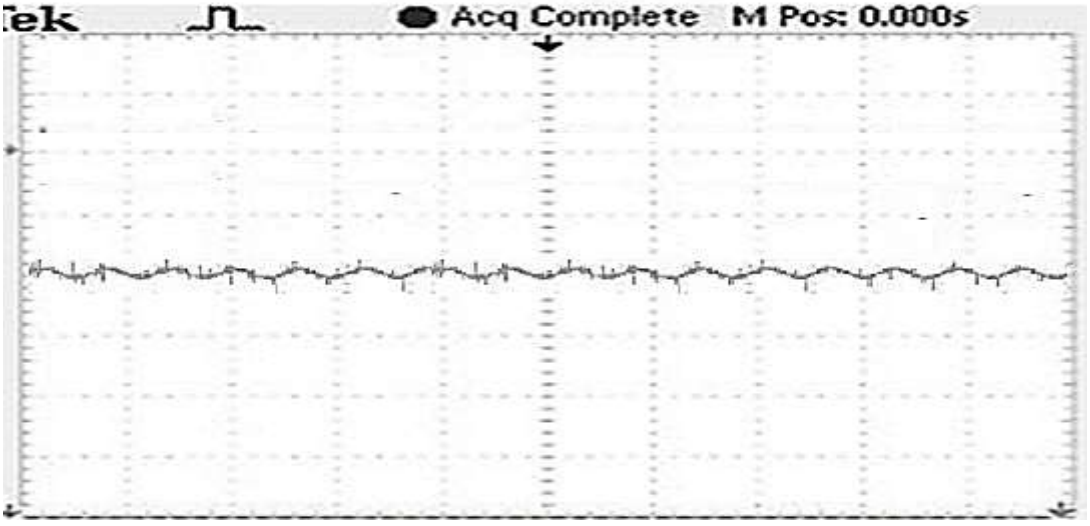


Figure 10.37 (b) Reactive power delivered in the Sub Synchronous mode of operation\
(SCALE –Y axis 0.5/Division & X axis 1/ Division)

Finally, it is concluded that the Matrix converter placed at the rotor side was able to control the active power flow and the reactive power flow in the stator. In both sub synchronous and super synchronous modes of operation the matrix converter was capable of delivering active power to the grid by absorbing or delivering power through the rotor terminals. This shows the variable speed operation of the wind turbines.

10.18 SCOPE OF THE WORK FOR FUTURE

The ride-through effects of matrix converter needs to be studied and improved which is one of the key factors that would decide the practical implementation of the matrix converter in the real time wind energy conversion systems.

The commutation problems of the matrix converter are addressed in various literature. The well-known four-step commutation technique is used in this work. It was experienced that the commutation failure often happens for unknown reasons in real time implementation. A complete investigation of these commutation issues needs to be carried out in the design of a stable and reliable matrix converter.

Common mode voltage issues in converters are generally addressed for reducing the early failure of the windings and bearing in machines fed by converters. Matrix converter also needs to be addressed with the issues of reduction or elimination of common mode voltage.

Further investigations are required to be carried out in evolving a simplified switching technique to avoid the complex computations during the process of generating the switching pulses.

Finally, the matrix converter needs to be rigorously analyzed for the effect of input filter on the stability of the system.

10.19 CONCUSION

After a detailed literature survey of matrix converter and the DFIG control structures it was found that the application of matrix converter in DFIG control would lead to a reduction in size of the converter, reduction in complexity of the control algorithm and elimination of bulky capacitor as compared to the conventional back to back converter. The conventional back-to-back converter uses a grid side converter and a rotor side converter along with a bulky DC bus. The matrix converter in the DFIG system uses a single converter on the rotor side, thereby eliminating the grid side converter. Owing to the large size of the bulky capacitor in the back-to-back converters the space occupied by the converter in more compared to the matrix converter and the failure of the DC

link capacitor leads to the replacement and maintenance problems. For the above said reason the matrix converter was selected as an alternative to the conventional back-to-back converter in this work. Various modulation techniques for the matrix converter were studied simulated in MATLAB-Simulink software and finally the direct space vector technique (DSVM) was selected since it leads to lower THD and higher modulation index (voltage transformation ratio). The various control techniques for the DFIG was studied and the simple control technique with PI controllers were selected and simulation was performed on the DFIG along with the matrix converter and the controller in MATLAB- Simulink software. Later the VHDL code development was performed using model base design in MATLAB- System generator interface for both the matrix converter switching technique and the rotor control of the DFIG using a matrix converter. These VHDL codes were optimized using Time division multiplexing technique (TDM) to implement the rotor side controller and DSVM algorithm within the available resources of the FPGA – SPARTEN 3E 500K IC. The data acquisition system to the FPGA for control action was developed using power transducers, speed sensors, comparators, output current direction sensing logic circuit, voltage transducers and analog to digital converters (ADC). The power circuit was developed using APTGT150DU120G bidirectional switch and CONCEPT SCALE driver IC. Finally the prototype was developed and was tested. The following results were inferred from the test. Matrix converters were capable of performing the power control in DFIG systems under sub synchronous and super synchronous modes of operation. As expected the control side algorithm was found to be less complex in matrix converters when compared to the conventional Back to back converters. Because in back to back converter the control algorithm involves two steps i) grid side control to maintain the DC bus constant and ii) rotor side control to provide the required rotor voltage. Whereas in matrix converter the grid side control is eliminated and the unified rotor side control is only required. However, the matrix converter switching algorithm was found to be extremely complex when compared to the back to back converter. The back to back converters are more stable compared to matrix converter since they don’t have a complex commutation strategy when compared to matrix converters.

Finally, from the work carried out it is reported that the use of matrix converter in DFIG system for control of power is one of the alternative solutions. However, it is suggested that before extending this work to the next level certain rigorous analysis are required. The matrix needs to be analyzed for its stability in terms of commutation issues and input filter resonance with the system. Moreover, a simplified switching algorithm, which can be a replacement to the existing technique, needs to be formulated. The analysis with respect to the ride through capability of the converter needs to be carried out and methods to improve the same needs to be formulated.

CHAPTER 11

PROBLEM FACED AND LESSONS LEARNT

The designed matrix converter was found to be stable when tested for speed control of the induction motor drive, where the matrix converter was feeding the stator of the singly fed induction motor (SFIM) with V/F control. When converter was connected to the power control of doubly fed induction generator (DFIG) on its rotor side, the control of power was achieved as desired.

Sudden misfiring of IGBT modules occurred, destroying the entire arm (Three IGBTS) of the converter when the experiment was conducted for a different set point (active power reference) due to unexpected interruption of supply.

As part of the project, the SSN has developed hardware & software for the control system & power circuit. However, the target specifications could not be met. As against the power rating of 5kW, the system could be tested only up to 1kW due to the failure of IGBTs during mains supply interruption.

11.1 PROBLEMS FACED

1. **Sudden misfiring of the IGBT modules, which destroyed the entire arm (three IGBTs) of the converter when the experiment was conducted for a different set-point (active power reference) due to unexpected interruption of supply.**

The possible reasons for failure could be the interruption of supply in the phases leading to a misfiring of the commutation algorithm, i.e. the zero crossing would have been detected wrongly during the power interruption. The misfiring of the IGBTs would have led to commutation problem destroying the IGBTs.

The other possible reason would be the failure of the driver circuit due to the wire bond lift-off and cracking of the solder layers in the driver circuit board resulting in an open circuit switch fault.

A proper hold up circuit is to be provided to the control the power supply, so that the control and protection features function properly, until the power circuit voltage decays to zero. The design of the holdup circuit, and the malfunctioning of the same may have caused the failure of IGBTs during mains interruption, which in turn could have triggered a malfunction in control & protection features.

Lesson Learnt

During such situations, a fault detection and diagnosis method that is both fast and reliable is required. This work did not include such methods of algorithms to reconfigure the switches accordingly. In future, such works would develop fault detection and diagnosis methods to overcome these problems.

2. Inadequate budget for the purchase of components that have failed

The project aimed at developing a power module (Matrix converter) completely at SSN College of Engineering. Hence, all the necessary components were purchased for developing the matrix converter. The proposal written for the development of the converter did not budget for multiple failure of devices. Hence, when the switches failed, new IGBT switches and other components could not be purchased. Considering that this is first external funded project, we did not anticipate such issues and including the same in the budget of the proposal.

Lesson Learnt

Standard industrial converter models need to be purchased and the experiments need to be conducted on such models when attempting a new method. In addition, there should be adequate provision in the budget for the purchase of devices and components when implementing a hardware project, which is still in the experimental research stage.

11.2 CONCLUSIONS

The converter designed in the work failed to be stable for reasons not fully known. However, we can gauge that fault detection and diagnosis methods with additional protection are essential for matrix converter when operated for power control techniques. As the converters, do not have inherent freewheeling paths to direct the inductive currents during impulse hard

switching, it is essential to analyze the converter for its stability in more detail before putting such converters into developing the prototype.

We have decided to conclude the work “matrix converter fed DFIG systems for power control” at this point due to budgetary and time constraints.

Based on our experience gained while implementing the project, we would carry out the complete analysis of the converter for fault detection and diagnosis. We plan to submit a new proposal shortly to funding agencies, with adequate budget and manpower’ for taking up this work forward.

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1. Senthil Kumaran, M., Siddharth, R. and Ranganath Muthu. "Matrix Converter Switching Strategy for Abnormal Voltage Conditions using Selective Harmonic Tracking Algorithm", International Journal of Modeling and Simulation, Vol. 32, No. 1, pp. 57 -64, 2012.

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MATRIX CONVERTER SWITCHING STRATEGY FOR ABNORMAL VOLTAGE CONDITIONS USING SELECTIVE HARMONIC TRACKING ALGORITHM

Senthilkumaran Mahadevan,* Siddharth Raju,* and Ranganath Muthu*

Abstract

A dynamic space vector modulation (SVM) approach for matrix converter operation in unbalanced and non-sinusoidal input voltage condition is presented. The concept of varying the modulation index based on the output of the selective harmonic tracking algorithm with reference to the fictitious DC bus is introduced. The complex relationship between output voltage and input voltage vectors of matrix converter for unbalanced and non-sinusoidal conditions is avoided using selective harmonic tracking algorithm. Using the oscillating fictitious DC bus vector, a simplified SVM approach is proposed to operate the matrix converter under extreme input voltage conditions. This approach is based on simple compensation of the output voltage modulation vector with respect to the oscillating fictitious DC bus vector. The unbalanced and non-sinusoidal input voltages are automatically compensated so that the output voltage is balanced and sinusoidal with minimum compromise in the sinusoidal nature of input current. The validity of the selective harmonic tracking algorithm approach is verified through simulation.

Key Words

Matrix converter, space vector, selective harmonic elimination, unbalanced condition

1. Introduction

The matrix converter (MC) is an array of 3×3 bidirectional switches functioning as a direct AC–AC converter. It directly interconnects two independent multiphase voltage systems at different frequencies. The MC achieves bidirectional power flow and independent control of the input displacement power factor without the use of bulky and limited lifetime reactive elements such as large electrolytic capacitors or AC inductors. Hence, it is called the all-silicon solution and is a good candidate for variable speed drives. The development of this converter started three decades back with the direct transfer function approach [1] where the output voltages were obtained by multiplication of modulation matrix with input voltages. Later the Optimum Alesina Venturini (OAV) method [2] was proposed, in which modulation index was extended from 0.5 to 0.866 by using the third harmonic injection technique. It was also proved that a modulation index of 0.866 is the physical limitation of the MC. Control technique using the "fictitious DC Link", a conceptually different idea [3], [4], decoupled the control into smaller independent units. This technique is now predominantly used by researchers of MC with space vector. Scalar control modulation algorithm using (MAX–MID–MIN) PWM technique [5] avoided the sector information required in the SVM method. Over-current and over-voltage spikes due to the difficulty in commutation of the controlled bidirectional switches was a major setback for this converter for years until advanced multi-step commutation strategies appeared that allowed for safe operation of switches [6]. Another important limitation of MC was the requirement of large number of power semiconductor switches for implementation. This problem has now been overcome with power modules complete with power circuit in a single chip [7] (EUPEC – FM35R12KE3, SEMIKRON SK60GM123). Today, research activity is in studying advanced technological and applications issues such as reliable implementation of commutation strategies, over voltage protection [8], operation under abnormal conditions [9], and reduction of common mode voltage and switching losses [10]. However, not much work has been done for abnormal input and load conditions for MC without complex calculations. In this paper unbalanced and harmonic study of MC is attempted. The selective harmonic tracking algorithm (SHTA), which calculates the oscillating fictitious DC bus vector (OFDCV) and modifies the modulation index for preserving the sinusoidal nature of input and output signals, is proposed.

A brief overview of SVM for MC is discussed in Section 2. In Section 3 dynamic model is presented for analytical study of unbalanced conditions in the MC. Equations

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Recommended by Prof. T. Wei
(DOI: 10.2316/Journal.205.2012.1.205-5627)

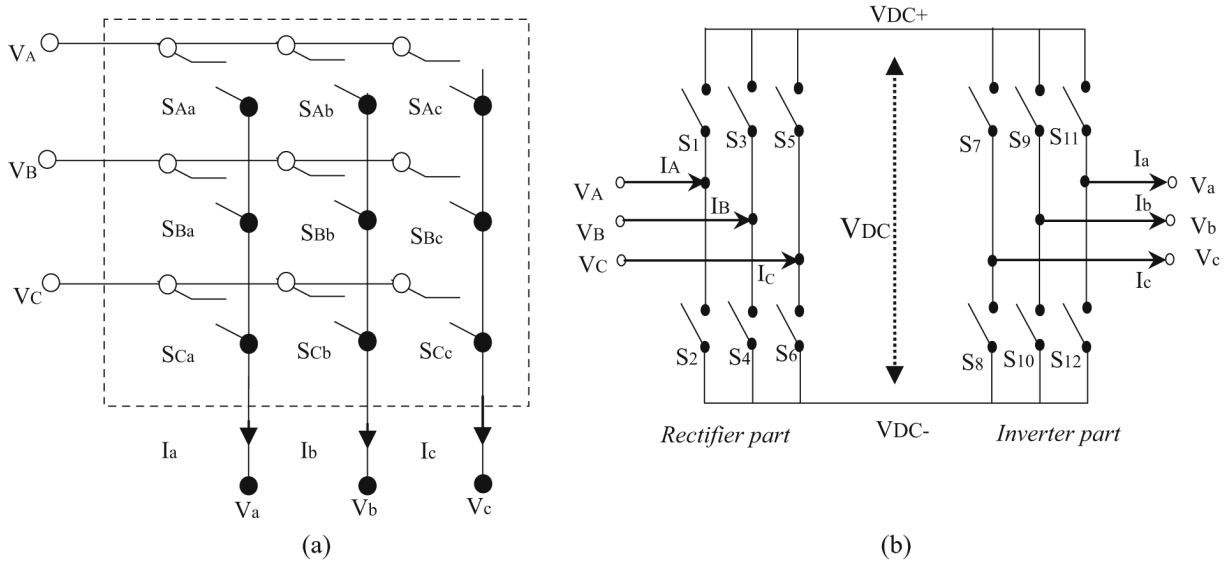

Figure 1. (a) Conventional MC and (b) MC as two stage converter.

for operation of MC under abnormal input conditions have been derived and simple modifications on SVM have been proposed for mitigating the effect of unbalance in Section 4 and in Section 5 the simulation results have been presented.

2. SVM for Matrix Converter

Output voltages and the input currents of the MC [11], as shown in Fig. 1(a), are represented by the switching function T, as given in (1) and (2):

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \times \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \times \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2}$$

Switching function T is represented as the product of a rectifier switching function and an inverter switching function as given in (3). The most commonly used modulation strategy for MC is the indirect modulation method, which decouples the control of the input current and the output voltage. MC can be visualized as a two-stage converter, as shown in Fig. 1(b).

$$\begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} = \begin{bmatrix} S_7 & S_8 \\ S_9 & S_{10} \\ S_{11} & S_{12} \end{bmatrix} \times \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix} \tag{3}$$

It is assumed that the power conversion happens through the fictitious DC-link. The inputs I_{IN}, V_{IN} and the outputs V_{OUT}, I_{OUT} are expressed as space vectors as given in (4) and (5):

$$\begin{aligned} V_{OUT} &= \frac{2}{3}\left(V_a + V_b \cdot \mathrm{e}^{j\frac{2\pi}{3}} + V_c \cdot \mathrm{e}^{j\frac{4\pi}{3}}\right), \\ I_{OUT} &= \frac{2}{3}\left(I_a + I_b \cdot \mathrm{e}^{j\frac{2\pi}{3}} + I_c \cdot \mathrm{e}^{j\frac{4\pi}{3}}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} V_{IN} &= \frac{2}{3}\left(V_A + V_B \cdot \mathrm{e}^{j\frac{2\pi}{3}} + V_C \cdot \mathrm{e}^{j\frac{4\pi}{3}}\right), \\ I_{IN} &= \frac{2}{3}\left(I_A + I_B \cdot \mathrm{e}^{j\frac{2\pi}{3}} + I_C \cdot \mathrm{e}^{j\frac{4\pi}{3}}\right) \end{aligned} \tag{5}$$

where V_A, V_B, V_C and V_a, V_b, V_c are input and output phase voltages, respectively, and I_A, I_B, I_C and I_a, I_b, I_c are input and output currents, respectively. An arbitrary voltage V_{OUT} in Fig. 2(a) can be synthesized as a vector sum of any two adjacent active vectors (V_1 to V_6) and zero vectors (V_0, V_7). Similarly, the input current I_{IN} in Fig. 2(b), can be synthesized as a vector sum of any two adjacent active vectors (I_1 to I_6) and one of the zero vectors (I_{0a}, I_{0b}, I_{0c}).

The output voltage and input current SVM duty cycles for the MC can be obtained from (6) to (10) which are derived from the product of inverter duty cycles and rectifier duty cycles [10]:

$$\begin{aligned} d_{v\alpha\, I\alpha} &= d_{v\alpha} * d_{I\alpha} = m_v * \sin\left(\frac{\pi}{3} - \theta_v\right) * m_c \sin\left(\frac{\pi}{3} - \theta_c\right) \\ &= \frac{T_{v\alpha\, I\alpha}}{T_S} \end{aligned} \tag{6}$$

$$d_{v\alpha\, I\beta} = d_{v\alpha} * d_{I\beta} = m_v * \sin\left(\frac{\pi}{3} - \theta_v\right) * m_c \sin(\theta_c) = \frac{T_{v\alpha\, I\beta}}{T_S} \tag{7}$$

$$d_{v\beta\, I\alpha} = d_{v\beta} * d_{I\alpha} = m_v * \sin(\theta_v) * m_c \sin\left(\frac{\pi}{3} - \theta_c\right) = \frac{T_{v\beta\, I\alpha}}{T_S} \tag{8}$$

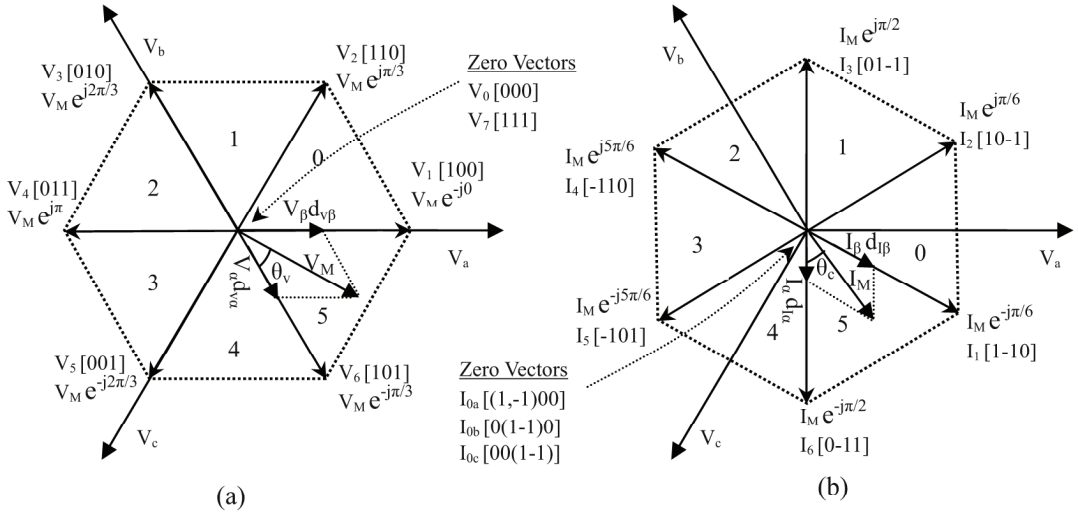

Figure 2. (a) Inverter voltage hexagon and (b) rectifier current hexagon.

$$d_{v\beta\, I\beta} = d_{v\beta} * d_{I\beta} = m_v * \sin(\theta_v) * m_c \sin(\theta_c) = \frac{T_{v\beta\, I\beta}}{T_S} \quad (9)$$

$$d_0 = 1 - d_{v\alpha I\alpha} - d_{v\alpha I\alpha} - d_{v\beta I\alpha} - d_{v\beta I\alpha} - d_{v\beta I\beta} = \frac{T_0}{T_S} \quad (10)$$

3. Dynamic Model of Matrix Converter as a Two Stage Converter

In this section, a dynamic model for a MC is developed that is valid for both steady-state and transient analyses. This model is validated with the direct switching model of MC. For observing the dynamics under unbalanced conditions, the direct transformation matrix D [12] is decomposed into two matrixes $D_I(\omega_0)$ and $D_R(\omega_i)$ as given in (11) and the fictitious DC bus voltage V_{DC} is as given in (12):

$$D = m_c m_v \begin{bmatrix} \sin(\omega_0 t + \varphi_0) \\ \sin\left(\omega_0 t + \varphi_0 - \frac{2\pi}{3}\right) \\ \sin\left(\omega_0 t + \varphi_0 + \frac{2\pi}{3}\right) \end{bmatrix} \times \begin{bmatrix} \sin(\omega_i t - \varphi_i) \\ \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ \sin\left(\omega_i t - \varphi_i + \frac{2\pi}{3}\right) \end{bmatrix}^T \quad (11)$$

$$V_{DC} = m_c \begin{bmatrix} \sin(\omega_i t - \varphi_i) \\ \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ \sin\left(\omega_i t - \varphi_i + \frac{2\pi}{3}\right) \end{bmatrix}^T \times \begin{bmatrix} V_{am} \sin(\omega_i t) \\ V_{bm} \sin\left(\omega_i t - \frac{2\pi}{3}\right) \\ V_{cm} \sin\left(\omega_i t + \frac{2\pi}{3}\right) \end{bmatrix} \quad (12)$$

where m_c and m_v are, respectively, the rectifier and inverter modulation indices, ω_i and ω_0 are, respectively, the input and output angular velocities. Under balanced condition, substituting V_{am}, V_{bm}, $V_{cm} = V_m$ and $m_c = 1$ in (12), (13) is obtained:

$$V_{DC} = 1.5 \times V_m \times \sin(\varphi_i) \quad (13)$$

4. Effect of Input Disturbances on the Fictitious DC Bus

Disturbances at the input introduce oscillations on the fictitious DC Bus. For any ith harmonic at the input, these oscillations can be decomposed into two components, namely $(i-1)\omega_e t$ and $(i+1)\omega_e t$. Considering a 3-phase system with m harmonics that is unbalanced, the Fourier series for phase voltages can be expressed as in (14):

$$V_a = \sum_{i=1}^{m} V_{a,i} \ \sin(i\omega_e t + \varphi_i) \quad (14)$$

Resolving the A phase input voltage into its symmetrical sequence components, we get (15):

$$V_a = \sum_{i=1}^{m} [V_{pi} \sin(i\omega_e t + \varphi_i + \varphi_{pi}) + V_{ni} \sin(i\omega_e t + \varphi_i + \varphi_{ni}) + V_{0i} \sin(i\omega_e t + \varphi_i + \varphi_{0i})] \quad (15)$$

The current lags the voltage by ρ for all phases. For the ith harmonic with positive sequence $V_{pi} < (\varphi_i + \varphi_{pi})$ and negative sequence $V_{ni} < (\varphi_i + \varphi_{ni})$, the current space vector for positive sequence of ith harmonic is given by (16)–(18):

$$f_{ai}^{+} = V_{pi} \sin(\theta - \rho) \sin(i\omega_e t + \varphi_i + \varphi_{ni}) \quad (16)$$

$$f_{bi}^{+} = V_{pi} \sin(\theta - \rho - 120^\circ) \sin(i\omega_e t + \varphi_i + \varphi_{ni} - 120^\circ) \quad (17)$$

$$f_{ci}^{+} = V_{pi} \sin(\theta - \rho + 120^\circ) \sin(i\omega_e t + \varphi_i + \varphi_{ni} + 120^\circ) \quad (18)$$

The d–q frame rotates in synchronism with the fundamental supply frequency, therefore $\theta = \omega_e t$ and (16)–(18) can be reduced to (19):

$$f_i^{+} = f_{ai}^{+} + f_{bi}^{+} + f_{ci}^{+} = \frac{3}{2} V_{pi} (\cos((i-1)\omega_e t + \varphi_{pi} + \varphi_i + \rho)) \quad (19)$$

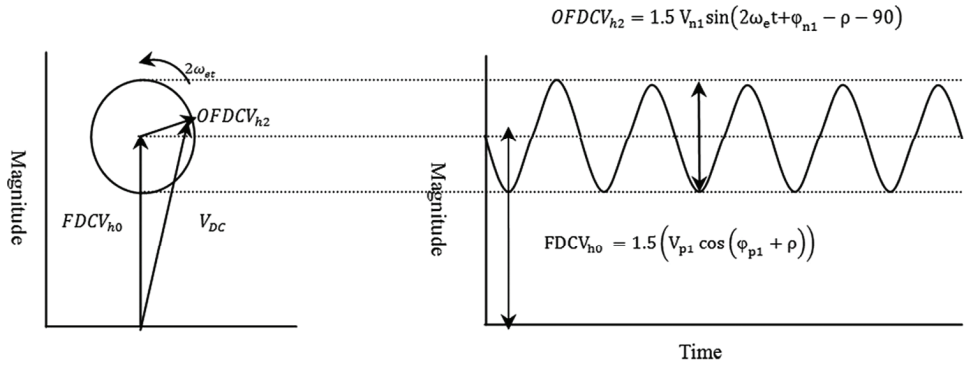

Figure 3. (a) Phasor representation and (b) time representation.

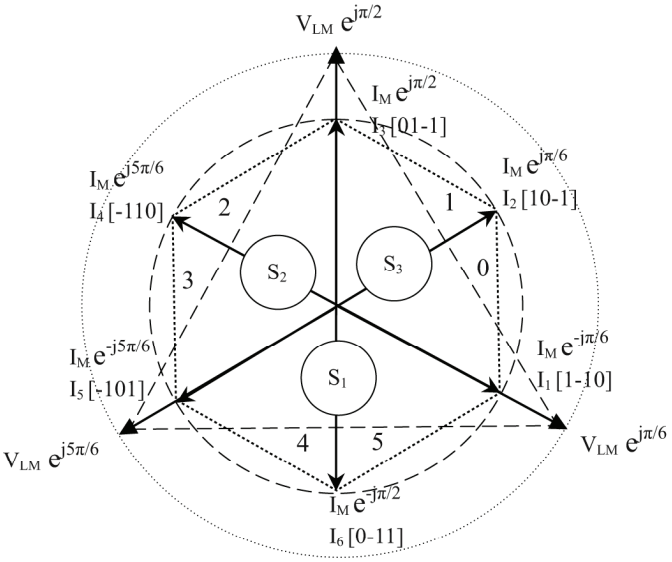

Figure 4. FDCV space vector with rectifier current space vector.

Similarly, the current space vector for negative sequence of ith harmonic is given by (20):

$$f_i^- = f_{ai}^- + f_{bi}^- + f_{ci}^- = -\frac{3}{2} V_{ni} (\cos((i+1)\omega_e t + \varphi_{ni} + \varphi_i - \rho)) \tag{20}$$

Under any switching, zero sequence component in the DC bus voltage is not present. Hence $f_i^0 = 0$ and the total current space vector f_i is given in Eqn. 21:

$$f_i = f_i^+ + f_i^- \tag{21}$$

The calculated fictitious DC bus voltage is given by (22):

$$V_{DC\_Calc} = \sum_{i=1}^{m} f_i \tag{22}$$

In unbalanced case with no harmonic content, (22) reduces to (23) as shown in Fig. 3(a) and (b):

$$V_{DC\_Calc} = \frac{3}{2}(V_{p1} \cos(\varphi_{p1} + \rho) + V_{n1} \sin(2\omega_e t + \varphi_{n1} - \rho - 90^\circ)) \tag{23}$$

Table 1
Voltage and Current Sector Selection

No.	Voltage Sector	Current Sectors
1	$S1$	0, 3
2	$S2$	1, 4
3	$S3$	5, 2

Table 2
Simulation Parameters

Quantity	Value
R–L Load	$R = 5\ \Omega$, $L = 0.3$ mH
Input phase voltage	220 V
Input voltage frequency	50 Hz
Input filter	$L = 100$ mH, $C = 35$ mF
Output voltage frequency	50 Hz
Switching frequency	10 KHz
Unbalance and harmonic content	$V_a = 100\%$ $V_b = 90\%$ $V_c = 100\%$ $V_{a2} = 4\%$ $V_{b2} = 10\%$ $V_{c2} = 10\%$ $V_{a3} = 3\%$ $V_{b3} = 25\%$ $V_{c3} = 12\%$

It can be seen in Fig. 3(b) that the second harmonic component is introduced in the fictitious DC bus voltage. If the inverter stage switching calculation is carried out without compensating for the 2nd harmonic voltage, the output voltage will be unbalanced and the space vector shall trace an ellipse. To compensate for harmonics and unbalance, output total harmonic elimination (OTHE) technique and input selective harmonic elimination (ISHE) technique have been proposed.

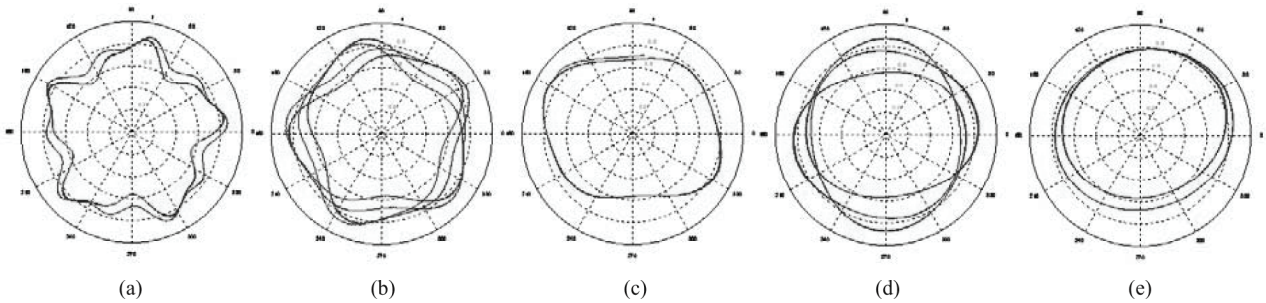

Figure 5. Polar plot of modified $m_{v,comp}$ for (a) $f = 20\,\text{Hz}$, (b) $f = 40\,\text{Hz}$, (c) $f = 50\,\text{Hz}$, (d) $f = 75\,\text{Hz}$, and (e) $f = 100\,\text{Hz}$.

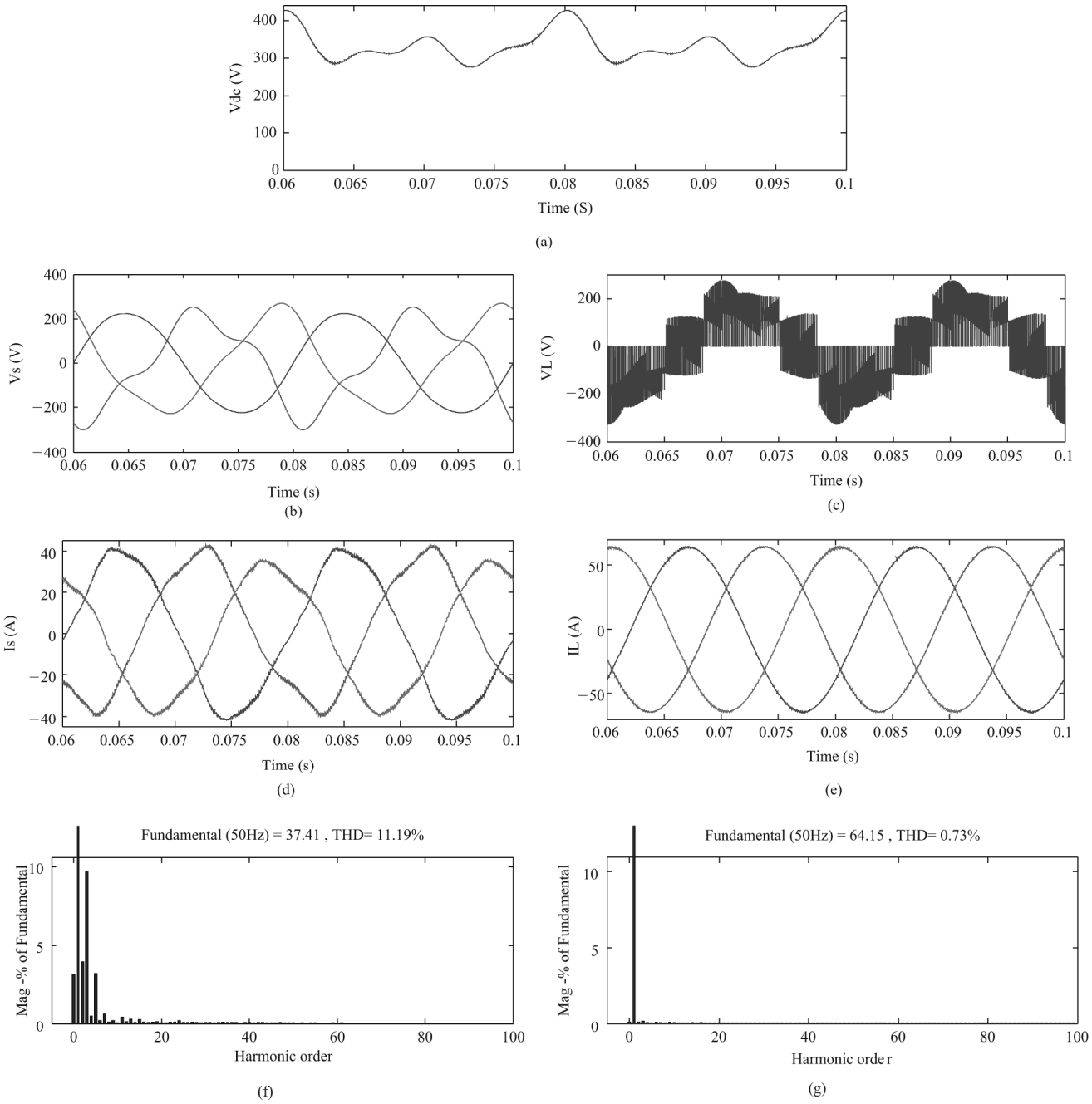

Figure 6. (a) FDC bus voltage, (b) input phase voltage, (c) output phase voltage, (d) input phase current, (e) output phase current, (f) harmonic characteristics of input current, and (g) harmonic characteristics of output current.

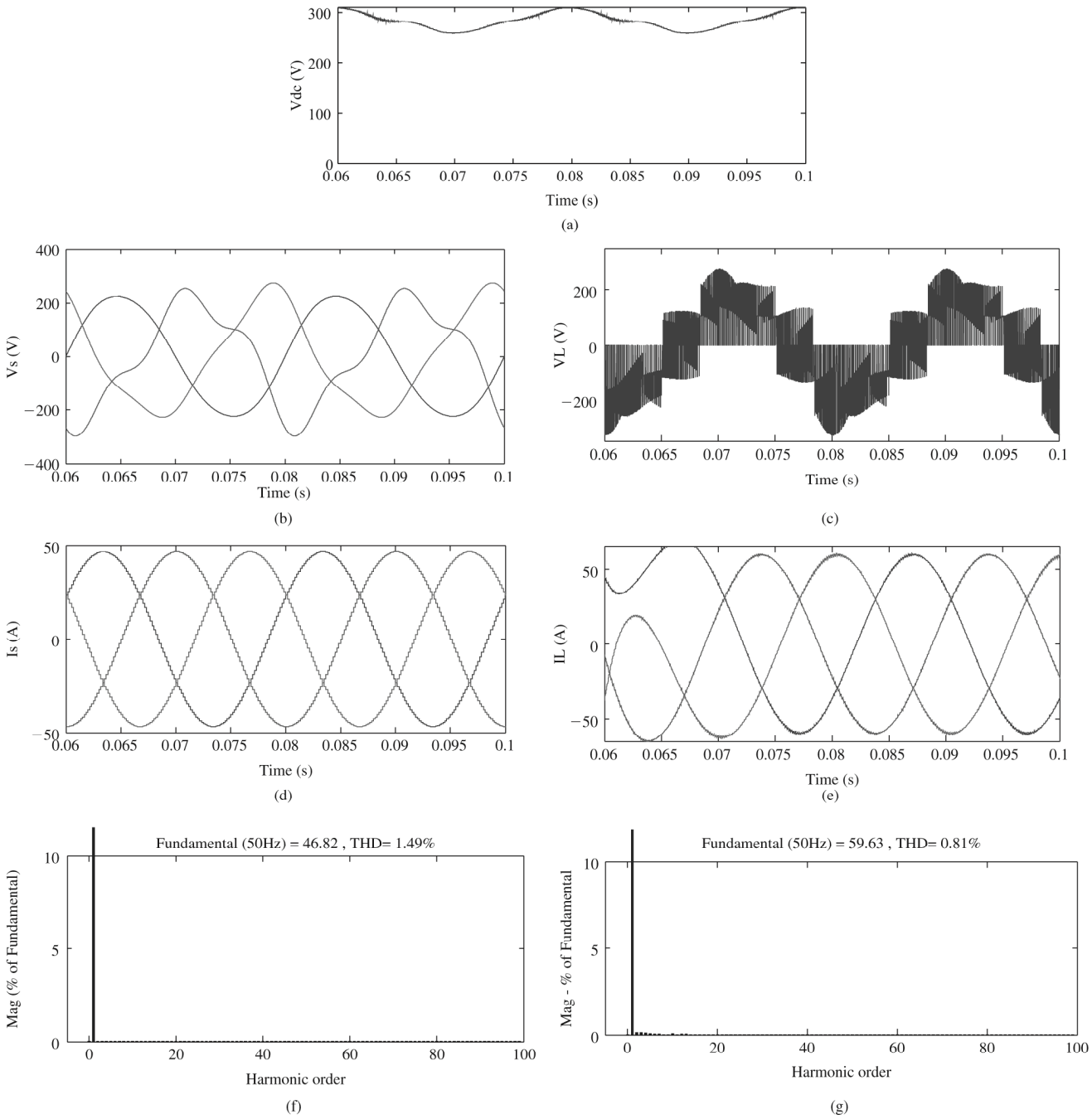

Figure 7. (a) FDC bus voltage, (b) input phase voltage, (c) output phase voltage, (e) input phase current, (e) output phase current, (f) harmonic characteristics of input current, and (g) harmonic characteristics of output current.

4.1 Output Total Harmonic Elimination (OTHE) Technique

The fictitious DC voltage (FDCV) space vector and the rectifier current space vector are shown in Fig. 4. The DC bus voltage can be synthesized as in (24):

$$V_{DC\_STHA} = d_{I\alpha} \times |V_1| + d_{I\beta} \times |V_2| \qquad (24)$$

The sector correspondence between the input current and FDCV space vector for unity displacement factor (UDF) is given in Table 1.

V_1, V_2 are the line voltages of the corresponding sector and $d_{I\alpha}$, $d_{I\beta}$ are the duty cycle ratio of the input current space vector with $m_c = 1$. The output modulation index is modified dynamically based on the computed DC link voltage. $V_{dc,min}$ is chosen as the maximum length of output voltage vectors. For an increase in the DC link voltage above this limit, the modulation index of the voltage source converter is reduced correspondingly to keep the output vector at the constant value as in (25). The output voltage vector traces a circle and hence a balanced output voltage is obtained for the 3 phases. A simple memory technique is used digitally to find V_{dc,min_SHTA} over every cycle from V_{dc_SHTA} and is used in the subsequent cycles. As a

result, the harmonic characteristic of the output current is improved while the input current harmonics are left uncompensated:

$$m_{v,comp} = m_v \times V_{dc,min\_SHTA}/V_{dc\_SHTA} \quad (25)$$

where $m_{v,comp}$ is the compensated inverter side modulation index.

4.2 Input Selective Harmonic Elimination (ISHE) Technique

For reduced harmonic content in input current and sinusoidal output voltage, correction must be applied to the rectifier and inverter side of the indirect modulation method. The input is analyzed for its selective harmonic content and the phase sequence voltages and FDCV is computed as in (23). The modulation index of the current source converter is computed as in (26):

$$m_{c,comp} = V_{dc,min}/V_{dc\_Calc} \quad (26)$$

where $m_{c,comp}$ is the compensated rectifier side modulation index. This can eliminate selective harmonic content in addition to the unbalance on the input current. But FDCV still oscillates because of the remaining uncompensated harmonics. For improving the quality of the output current SHTA must be applied on the inverter side as in (25).

5. Simulation Results

To evaluate the performance of proposed techniques, simulation with $R-L$ load was performed. The simulation parameters are shown in Table 2.

Using SHTA, a SVPWM switching sequence for balanced output was synthesized under abnormal input voltage conditions. An analysis between the uncompensated system and the compensated system has been carried out and the results are presented.

5.1 Output Voltage Synthesis using OTHE Technique

Oscillations in the FDC bus reflect harmonics and unbalance in the input. By modifying the modulation index dynamically as shown in Fig. 5, it is found that the output current spectrum contains no harmonic content and is balanced with a total harmonic distortion (THD) = 0.73%. The input current spectrum shows harmonic contents with THD = 11.19% as shown in Fig. 6.

5.2 Output Voltage Synthesis using ISHE

Oscillations in the FDC bus reflect the uncompensated harmonics in the input. Input compensation was done for the third harmonic and unbalance; the second harmonic was allowed to appear on the FDC bus. Modifying the modulation index dynamically at input and output, it is found that the digitally filtered input current spectrum shows harmonic contents with THD = 1.49% and the output current spectrum contains no harmonic content and is balanced with a THD = 0.81% as shown in Fig. 7. It is found that this technique performs selective compensation at the input and complete compensation at the output.

6. Conclusion

The available scheme in literature [13] aims only at eliminating the effects of unbalance whereas the proposed method provides a comprehensive scheme for elimination of the effects of both unbalance and harmonics. In the proposed method only the modulation index has been determined dynamically whereas the other method uses new space vector solution which makes the system complex and requires many memory tables for calculating the duty cycles that increases the memory requirement in the DSP or FPGA used.

A simple SHTA method for MC using the virtual DC-link concept for abnormal input voltage conditions has been presented. Proposed techniques take advantages of the decoupling algorithm used in indirect space vector PWM to synthesize quality voltage with a minimum de-rating of the load. In addition, new switching sequences that can improve the output voltage and current quality have been proposed. As a result, the harmonic characteristic of the output current of the MC was improved at the cost of minimum de-rating of the load. Under OTHE technique the input current spectrum was uncompensated but under ISHE technique harmonic contents was minimized at the input with total compensation on the output. The proposed techniques can be used for grid fault ride – through in DFIG connected to wind turbine. These techniques are compatible with indirect space vector PWM method and can easily be implemented for selective harmonic elimination at the input and total harmonic elimination at the output.

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International Review of Electrical Engineering (IREE)

PART A

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(continued)

Praise Worthy Prize

International Review of Electrical Engineering (I.R.E.E.), Vol. 7, N. 4
ISSN 1827- 6660 July - August 2012

Minimum Error Switching Strategy for Matrix Converter with Input Current Control

M. Senthil Kumaran, R. Siddharth, Ranganath Muthu

Abstract – *This paper introduces a new switching strategy for Matrix Converter (MC), the Minimum Error Switching Strategy (MESS) that implements a modified hysteresis based control technique. The technique limits the switching time to produce switching pulses of constant width. The decoupled indirect-space vectors of the MC are used for input current control and output voltage control. Switching vectors are selected based on the minimum computed voltage error and minimum computed current error over every sampling period. Important features of the technique are the constant pulse width switching leading to simplified modulation, uniformly distributed switching stresses over an output cycle and inherent mitigating effects of unbalance at the input. The technique proves to be more efficient in offering superior input and output current spectrums for higher switching frequency. In this paper, under distorted input voltage conditions, behavior of the MC controlled by MESS is analyzed. The proposed PWM algorithm is verified by MATLAB simulation and hardware experimentation on a laboratory prototype and results obtained are satisfactory.*

Keywords: *Matrix Converter, Unbalanced Input, Over-Modulation Index, Error Compensation*

Nomenclature

V_i	3 phase input voltages
V_o	3 phase output voltages
I_i	3 phase input currents
I_o	3 phase output currents
S	Matrix converter switching matrix
S_I	Fictitious inverter switching matrix
S_C	Fictitious converter switching matrix
V_{cm}	Common mode voltage
Ve_{mj}	Calculated output voltage error
Ve_{pj}	Previous state output voltage error
Ie_{mj}	Calculated input current error
Ie_{pj}	Previous state input current error
S_{Ion}	Fictitious inverter switching matrix used for the current state
S_{Con}	Fictitious converter switching matrix used for the current state
V_{DC}	Fictitious DC bus voltage
I_{DC}	Fictitious DC bus current
m_v	Modulation index of the fictitious inverter
m_c	Modulation index of the fictitious converter
T_s	Sampling Time
d	Duty cycle

I. Introduction

The matrix converter (MC) is a compact array of 3 × 3 bidirectional switches functioning as a direct AC-AC converter.

In many AC drive application it is desired to use compact voltage source converters instead of conventional AC-DC-AC converters that have bulky DC capacitors. With proper switching, MC can be treated as a universal AC transformer with the ability to change amplitude, frequency and phase angle, which are the three important quantities that characterize an AC variable. The development of this converter started three decades back with the direct transfer function approach [1], wherein the output voltages were obtained by multiplication of the modulation matrix with input voltages. Later the Optimum Alesina Venturini (OAV) method [2] was proposed, in which the modulation index was extended from 0.5 to 0.866 by using the third harmonic injection technique. It was also proved that a modulation index of 0.866 is the physical limitation of the MC modulated by direct space vector technique. Control technique using the 'fictitious DC Link', a conceptually different idea [3] - [4], decoupled the control into smaller independent units. This technique is now predominantly used by researchers of MC with space vector. Scalar control modulation algorithm using (MAX - MID - MIN) PWM technique [5] avoided the sector information required in the space vector modulation (SVM) method. A new simple technique for modeling and analysis of matrix converter using Singular Value Decomposition (SVD) [6] was proposed from which all other technique could be developed. For many years, the difficulty in commutation of controlled bidirectional switches was a major setback for this converter until advanced multi-step commutation strategies appeared that allowed for safe operation of

Manuscript received and revised July 2012, accepted August 2012

switches [7]. In recent years MC has become more attractive because of the availability of high speed DSP processors in implementing multi step commutation techniques. Another important limitation of MC was the requirement of large number of power semiconductor switches. The development of intelligent power modules (EUPEC- IPM) [8] has increased the reliability and efficiency of the converter. Recently, MCs have also found applications in induction motor drives for direct torque control [9].

This paper proposes a simple Minimum Error Switching Strategy (MESS), with constant pulse-width, for all switching devices of the converter. This distributes the switching stresses of each switch uniformly within an output cycle of the converter. In addition, it has an inherent capability of mitigating the effects of unbalance at the input. A brief overview and modeling of MC with decoupled space vector technique is introduced in Section II. The MESS for voltage control in inverter and in MC is developed in Section III. The modified MESS for improved current spectrum is explained in Section IV. The inherent mitigating effect of MESS for MC under distorted input conditions are discussed in Section V. In Section VI, the proposed MESS method is compared with SVM technique. In Section VII, simulation and hardware results are presented.

II. Decoupled Space Vectors for Matrix Converter

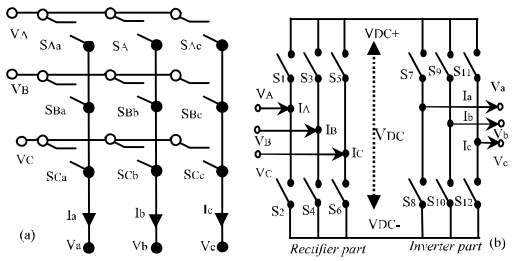
A 3-phase to 3-phase CMC topology is shown in Fig. 1(a). CMC connects any input phase to any output phase, with 512 switching patterns, of which only 27 are valid. The output voltages and currents of the matrix converter, shown in Figs. 1, are given by Eqns. (1) to (3):

$$V_i = \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}, \quad V_o = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \quad I_i = \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \;\&\; I_o = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (1)$$

$$S = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \;\&\; V_{cm} = \frac{1}{3}\begin{bmatrix} V_a + V_b + V_c \\ V_a + V_b + V_c \\ V_a + V_b + V_c \end{bmatrix} \quad (2)$$

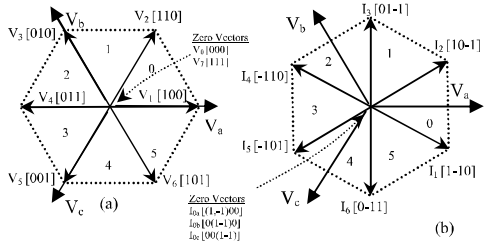
$$V_o = S \times V_i - V_{cm} \;\&\; I_i = S^T \times I_o \quad (3)$$

where V_i and I_i are respectively the 3-phase input voltages and currents, V_0 and I_0 are respectively the 3-phase output voltages and currents, S denotes the switching function and V_{cm} represents the common mode voltage. Valid switching patterns of S are further divided into three groups; rotating vectors (6), stationary vectors (18) and zero vectors (3). Rotating vectors reduce the voltage transfer ratio of the converter for sinusoidal outputs [10] and hence are not used. The remaining 21 vectors are used in the space vector technique. The SVM technique for CMC with decoupled space vectors is presented. The CMC is decoupled into a fictitious current source converter (FCSC) and a fictitious voltage source inverter (FVSI), connected back to back with a fictitious DC bus (FDCB) as shown in Fig. 1(b). The objective of the Indirect Space Vector Modulation (ISVM) technique is to synthesize output voltages from input voltages and input currents form output currents.



Figs. 1. (a) Conventional Matrix Converter, (b) Back to Back Converter

The voltage and current space vectors of the decoupled FVSI and FCSC are shown in Figs. 2.



Figs. 2. (a) Inverter Voltage Hexagon, and (b) Rectifier Current Hexagon

Switching function S is represented as the product of rectifier switching function and inverter switching function, as given in Eqns. (4) & (5), where, S_C and S_I are respectively the inverter and converter switching matrixes required to synthesize voltage vectors V_o & current vectors I_i:

$$\begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} = \begin{bmatrix} S_7 & S_8 \\ S_9 & S_{10} \\ S_{11} & S_{12} \end{bmatrix} \times \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix} \quad (4)$$

$$S = S_I \times S_C \quad (5)$$

For the FVSI, an arbitrary output voltage V_{OUT} can be synthesized as a vector sum of any two adjacent active vectors (V_1 to V_6) and zero vectors (V_0, V_7). Similarly, for the FCSC, the input current I_{IN} can be synthesized as a vector sum of any two adjacent active vectors (I_1 to I_6) and one of the zero vectors (I_{0a}, I_{0b}, I_{0c}). The SVM duty cycle for the CMC can be obtained from Eqns. (6) to (10), which are derived from the product of inverter duty cycle and rectifier duty cycle [11], were θ_v is the reference voltage space vector angle in a sector and θ_c is the reference current space vector in a sector:

$$d_{v\alpha\, I\alpha} = d_{v\alpha} * d_{I\alpha} = \\ = m_v * sin\left(\frac{\pi}{3} - \theta_v\right) * m_c\, sin\left(\frac{\pi}{3} - \theta_c\right) = \\ = \frac{T_{v\alpha\, I\alpha}}{T_s} \quad (6)$$

$$d_{v\alpha\, I\beta} = d_{v\alpha} * d_{I\beta} = \\ = m_v * sin\left(\frac{\pi}{3} - \theta_v\right) * m_c\, sin(\theta_c) = \\ = \frac{T_{v\alpha\, I\beta}}{T_s} \quad (7)$$

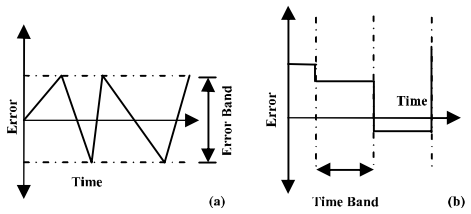
$$d_{v\beta\, I\alpha} = d_{v\beta} * d_{I\alpha} = \\ = m_v * sin(\theta_v) * m_c\, sin\left(\frac{\pi}{3} - \theta_c\right) = \\ = \frac{T_{v\beta\, I\alpha}}{T_s} \quad (8)$$

$$d_{v\beta\, I\beta} = d_{v\beta} * d_{I\beta} = \\ = m_v * sin(\theta_v) * m_c\, sin(\theta_c) = \\ = \frac{T_{v\beta\, I\beta}}{T_s} \quad (9)$$

$$d_0 = 1 - d_{v\alpha\, I\alpha} - d_{v\alpha\, I\alpha} - d_{v\beta\, I\alpha} + \\ - d_{v\beta\, I\beta} = \frac{T_{v\beta\, I\beta}}{T_s} \quad (10)$$

III. Minimum Error Switching Strategy (MESS)

This section introduces a new switching strategy for the CMC. Hysteresis PWM current control technique for power converters [12] under closed loop is the widely used due to its simplicity. Such hysteresis techniques are not available for voltage control as they provide only a six pulse output instead of a PWM output. Hence, it is necessary to modify the hysteresis method for voltage control, which is here termed as the (MESS) technique. The basic idea of the modulation technique is to have a constant time band instead of a constant error band, as in hysteresis technique, as shown in Figs. 3.



Figs. 3. (a) Hysteresis controller (b) MESS controller

The method minimizes the error between the actual output and the expected output in a switching period. In the next switching instant the previously calculated minimum error is added to the present error, which is the input to controller. The proposed switching strategy decouples the CMC into a FVSI and FCSC, as explained in section 2. It selects appropriate switching that minimizes the output voltage error for FVSI and input current error for the FCSC.

It is assumed that constant DC voltage and constant DC current are available at the FDCB. During every switching period, the error quantities Ve_{mj} for FVSI and Ie_{mj} for FCSC are calculated using Eqns. (11) to (14) and Tables I & II. Since the input current magnitude is dependent only on the load, the modulation index m_c of the FCSC is always operated at unity. Hence, the I_{DC} of the FDCB link is assumed to be constant with magnitude of one and used for current error calculations of FCSC. V_{DC} is determined using the selected switching pattern of FCSC and the measured input voltage as given by Eqn. (19), for voltage error calculations of FVSI. The switching states S_{Ion} , S_{Con} as given in Eqns. (15) and (16), are selected that corresponds to the smallest of the sum of the absolute value of the three phase errors and the propagated error. Finally, both FVSI and FCSC switching signals are processed through a digital logic circuit [13] for generating CMC switching signal:

$$V_{mj}(t) = S_{Im} \times V_{DC\,i}(t)\,, \\ m \in \{1 \to 8\}, i \in \{+,-\}\ \&\ j \in \{a,b,c\} \quad (11)$$

$$Ve_{mj}(t) = \left(V_{rj}(t) - V_{mj}(t)\right) + Ve_{pj}(t) \quad (12)$$

$$I_{mj}(t) = {S_{Cm}}^T \times I_{DC\,i}(t)\,, \\ m \in \{1 \to 9\}, i \in \{+,-\}\ \&\ j \in \{A,B,C\} \quad (13)$$

$$Ie_{mj}(t) = \left(I_{rj}(t) - I_{mj}(t)\right) + Ie_{pj}(t) \quad (14)$$

$$S_{Ion}(t) = S_{Im} \in \min_{m \to 1 \ldots 8} \sum_{i=a,b,c} |Ve_{mj}(t)|^2 \quad (15)$$

$$S_{Con}(t) = S_{Cm} \in \min_{m \to 1 \ldots 9} \sum_{i=A,B,C} |Ie_{mj}(t)|^2 \quad (16)$$

$$Ve_{pj}(t) = Ve_{mj}\,(t-1) \in S_{Ion}(t-1) \quad (17)$$

$$Ie_{pj}(t) = Ie_{mj}\,(t-1) \in S_{Con}(t-1) \quad (18)$$

$$\begin{bmatrix} V_{DC+} \\ V_{DC-} \end{bmatrix} = \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix} \times \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (19)$$

where, V_{mj} and I_{mj} are respectively the output voltage and input current corresponding to switching matrixes S_{Im} and S_{Cm}, V_{rj} and I_{rj} denote respectively the reference output voltage and input current, Ve_{mj} and Ie_{mj} are respectively the output voltage error and input current error corresponding to switching states S_{Im} and S_{Cm}, Ve_{pj} and Ie_{pj} are respectively the output voltage error and input current error due to the previous switching state and S_{Ion} and S_{Con} are respectively the switching matrix used for the present switching state for FVSI and FCSC.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGE FOR THE FVSI

m	S_{Im}	V_a	V_b	V_c
1	[100]	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$
2	[110]	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$
3	[010]	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$
4	[011]	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$
5	[001]	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$
6	[010]	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$
7	[000]	0	0	0
8	[111]	0	0	0

TABLE II
SWITCHING STATES AND INPUT CURRENTS FOR THE CSC

m	S_{Cm}	I_A	I_B	I_C
1	[1 -1 0]	I_{DC}	- I_{DC}	0
2	[1 0 -1]	I_{DC}	0	- I_{DC}
3	[0 1 -1]	0	I_{DC}	- I_{DC}
4	[-1 1 0]	- I_{DC}	I_{DC}	0
5	[-1 0 1]	- I_{DC}	0	I_{DC}
6	[0 -1 1]	0	- I_{DC}	I_{DC}
7	[(1, -1) 0 0]	0	0	0
8	[0 (1, -1) 0]	0	0	0
9	[0 0(1, -1)]	0	0	0

This technique has superior performance under high switching frequencies, because of its constant pulse width nature and simplicity in implementation. The uneven and multiple switchings within a sampling period in SVM makes real-time implementation complex. Near the boundries of a sector where the switching time is reduced to very small intervals that are less than one-tenth of the sampling period, the power devices fail to respond effectively and undergo additional stresses and losses. The proposed technique has the inherent ability of mitigating the effects of unbalance and harmonics at the output.

IV. Improved Current Control of MESS

Considerably high harmonics content of the input current of the CMC is experienced by the MESS technique of section 3 for lower modulation indexes. Hence, a modified MESS technique is proposed, in this section, to improve the performance for low modulation indexes. It is observed that zero vectors of CSC do not influence the input current spectrum but zero vectors of VSI influence the input current spectrum by a considerable factor. Hence, the error of the CSC is recalculated as explained below.

The first step in the MESS technique is to calculate the CSC switching pattern as explained earlier in section 3. Next, the V_{DC} of the FDCB is computed on the assumption that a constant I_{DC} flows in the FDCB, as given in Eqn. (20). For active and zero vectors applied on the CSC, Eqn.(20) calculates the accurate value of V_{DC}. The third step is to calculate the VSI switching pattern with the computed V_{DC}:

$$V_{DC} = \begin{bmatrix} S_1 & S_3 & S_5 \\ -S_2 & -S_4 & -S_6 \end{bmatrix} \times \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (20)$$

However in computing the switching pattern for VSI, the assumption that a constant I_{DC} flows in the FDCB hold good only for selection of active vectors. However, for selection of zero vectors of VSI, the above said assumption do not hold good. This is because, with the application of zero vectors, the I_{DC} becomes zero due to the isolation of the source from the load. There is a need to recalculate the current error, which could be used for calculation in the next sampling time. Hence, it is proposed in the improved MESS technique to ignore the calculated current error, $Ie_{mj}\,(t-1)$ and use $Ie_{mj}\,(t-2)$, when a zero vector is applied on the VSI, as given by Eqn.(21):

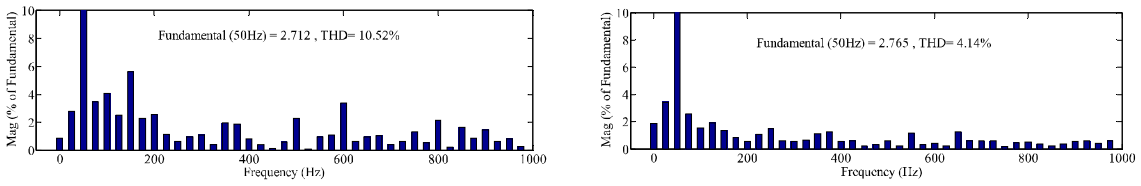
$$\begin{aligned} Ie_{pj}(t) &= Ie_{mj}\,(t-1)\epsilon\ S_{Con}(t-1) \\ &\text{when the VSI uses a active vector} \\ Ie_{pj}(t) &= Ie_{mj}\,(t-2)\epsilon\ S_{Con}(t-2) \\ &\text{when the VSI uses a zero vector} \end{aligned} \quad (21)$$

It is found that for lower modulation index, as seen in Figs. 4, that in the improved MESS technique, the input current total harmonic distortion (THD) is reduced by 59% when compared to method proposed in section 3. The block diagram representation of the improved MESS technique is shown in Fig. 5.

V. Unbalanced and Harmonic Effects on MESS

The proposed technique has the inherent ability of mitigating the effects of unbalance and harmonics present at the input. Since the method works on the error propagation and compensation scheme, the effects of unbalance and harmonics are completely eliminated or reduced depending on the magnitudes of unbalance, harmonics and present modulation index (MI).

The MESS technique, when operated at lower MI, minimizes the effects of unbalance without the need for additional calculations, as in SVM [14] technique, as shown in Fig. 10. However, when operating with higher MI the effect of unbalance can be eliminated only by reducing the MI. The factor by which the modulation index is reduced is determined by the amount of unbalance at the input.



Figs. 4. Current harmonics (a) MESS technique and (b) Modified MESS technique

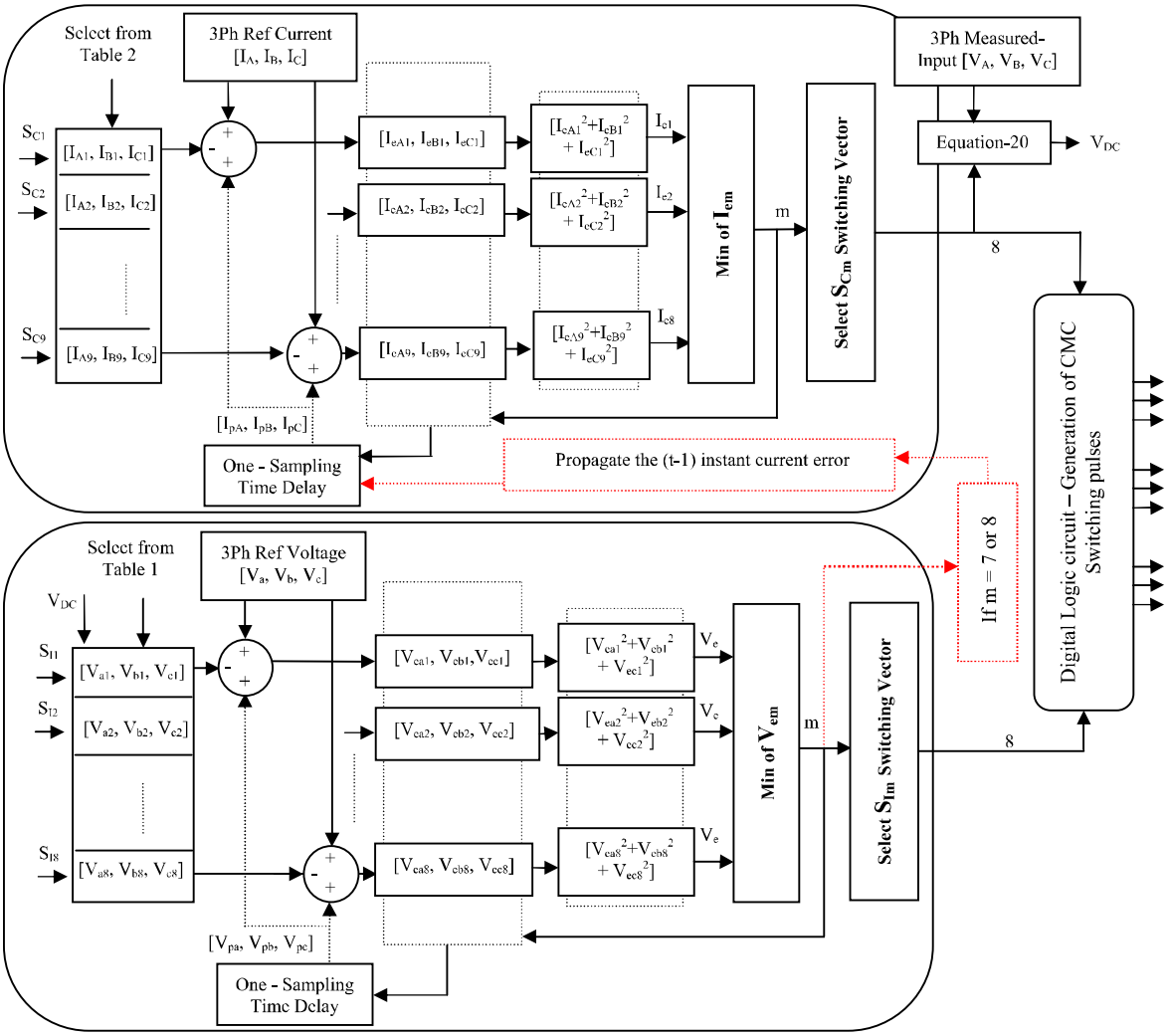


Fig. 5. Parallel Execution Sequence of MESS Algorithm

VI. Common Mode Voltage Reduction Scheme in MESS

The MESS technique also implements methods to reduce the peak magnitude of the common mode voltage (CMV) [15]. This method reduces the CMV by connecting the FSCS leg with minimum input voltage to the FDCB during the zero vector switching period of FCSC and zero vector switching period of FVSI. The algorithm to implement the CMV reduction is given in Fig. 6. The reduction of peak magnitude of the common mode voltage is shown in Figs. 7.

VII. Simulation and Hardware Results

To evaluate the performance of proposed techniques,

simulation with R–L load was performed using MATLAB/ Simulink. The simulation parameters are shown in Table III.

TABLE III
SIMULATION PARAMETERS

Quantity	Value
R-L Load	R = 5Ω , L = 23.7 mH
Input phase voltage	230 V
Input voltage frequency	50 Hz
Input filter	L = 1 mH, C = 10 μF
Output Voltage frequency	25 Hz
Switching frequency	10 kHz
Modulation Index	0.78

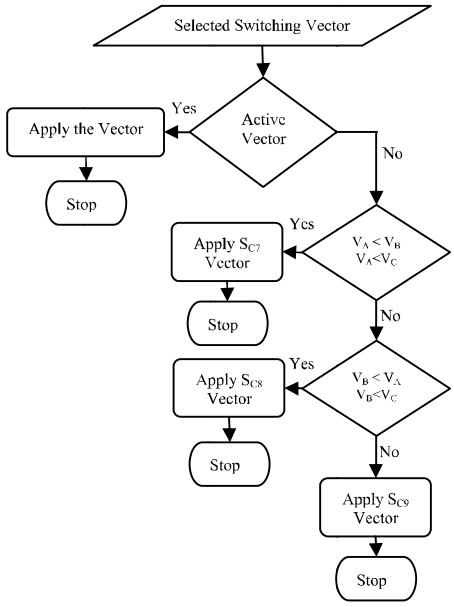
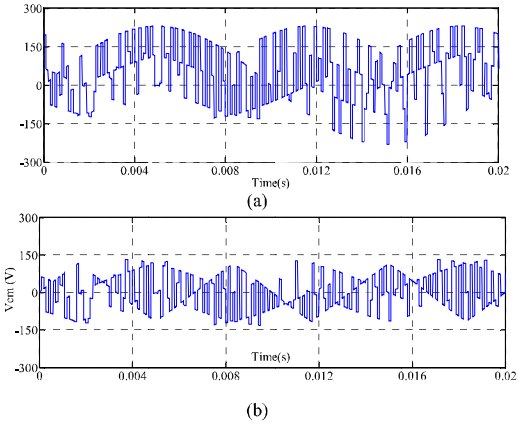


Fig. 6. Algorithm for common mode voltage reduction

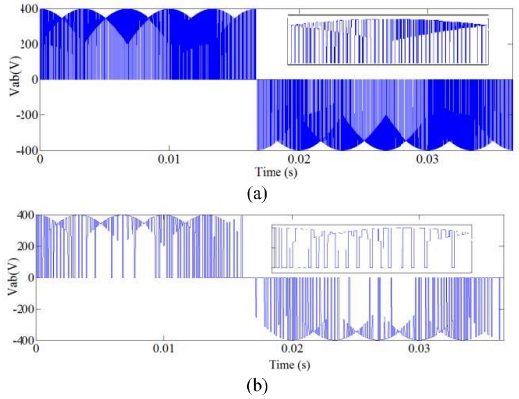
The MESS algorithm was simulated and the simulation results are presented in Fig. 10. An unbalance of 80% in phase B was introduced at 0.06s and the converter operates at a modulation index of 0.75. The MESS technique mitigates the unbalance automatically without any additional computation at the output, as seen in Fig. 9(d). It can also be seen that the peak of common mode voltage is reduced by 60%, as seen in Figs. 7, by implementing the algorithm.

The MESS switching states are compared with SVM switching states and are shown in Figs. 8. It is observed that the multiple switching that occur in SVM method within the sampling frequency, when compared to the constant switching in MESS technique, results in an increased switching loss [16], for the same switching frequency, as given in Fig. 9.

The current harmonics of the MESS is comparatively high when compared to SVM technique. At higher switching frequencies, the MESS technique has superior performance as compared to SVM, because the SVM introduces multiple pulses within the switching interval, which increases the actual switching frequency of the device due to which the device may fail to respond. These introduce more harmonics at the output current.



Figs. 7. Simulation Results (a) Without common mode voltage reduction and (b) With common mode voltage reduction



Figs. 8. Simulation Results (a) SVM output (b) MESS output

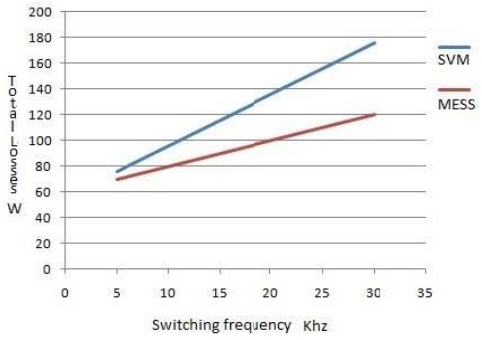


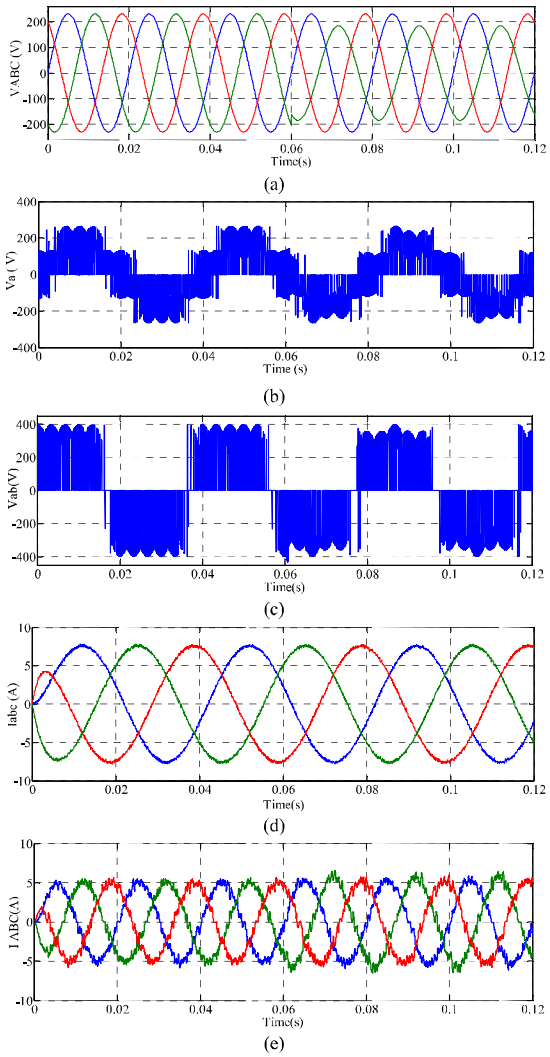
Fig. 9. Total losses in CMC with SVM and MESS techniques

To validate the proposed control algorithm, a laboratory prototype was developed, as shown in Fig. 11. The hardware consists of a power module designed with eighteen discrete IRFP460 MOSFET switches, a driver

module designed with Scale technology based Concept Driver 6SDEI06 ICs, a measurement module designed with LV 25p voltage sensors and LA 55p current sensors and a controller module designed with FPGA – Spartan-3 DSP. The input filter capacitance and inductance for the hardware is designed to be 10μF and 1 mH. The damping resistor of 50Ω [17]-[18] is used for reducing the harmonics content near the resonant frequency.

The experiment was conducted with a balanced input voltage and the switching frequency was selected to be 7 kHz.

The matrix converter was used for converting 50 Hz input frequency to 25 Hz output frequency using the MESS technique, as shown in Figs. 12. The hardware results verify the effectiveness of the proposed MESS method for CMC.



Figs. 10. Simulation Results (a) input phase voltage (b) output phase voltage, (c) output line voltage, (d) output current, (e) input current

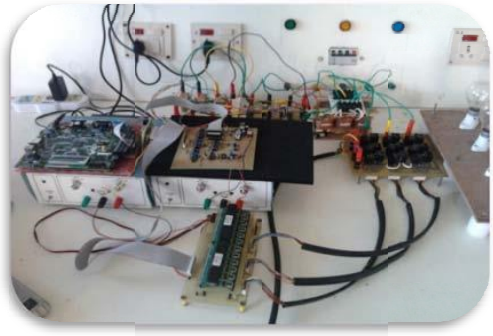
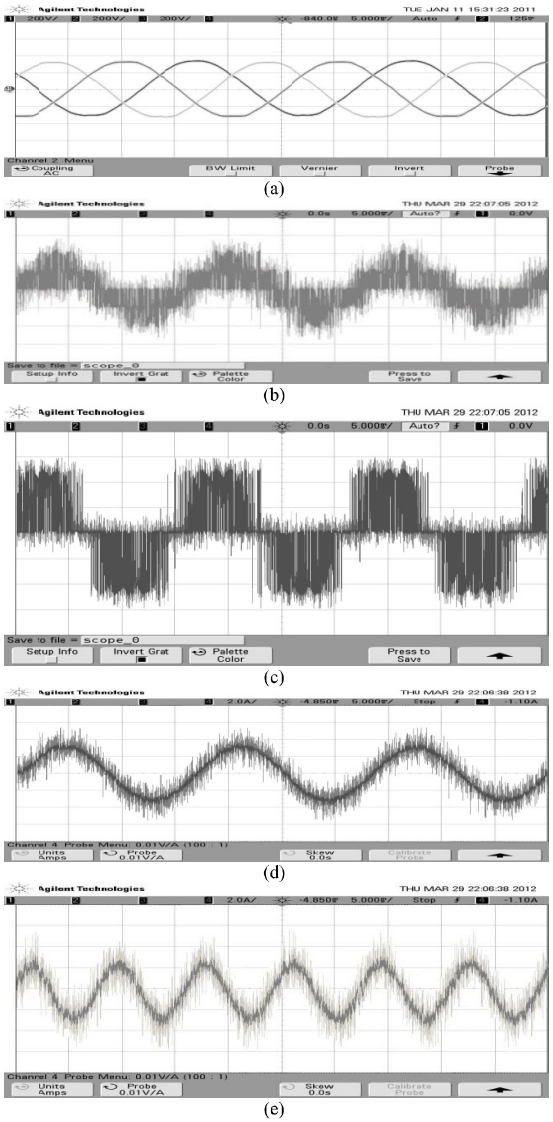


Fig. 11. Matrix Converter Hardware Prototype



Figs. 12. Simulation Results (a) input phase voltage (b) output phase voltage, (c) output line voltage, (d) output current, (e) input current

VIII. Conclusion

In this paper, the proposed MESS strategy for matrix converter was compared with SVM technique for matrix converter. The switching losses were found to be higher in the SVM technique because of uneven and multiple pulse width switching, during every sampling period. This method is simple and effective for real-time implementation and controller design. It has been found that MESS technique mitigates the effects of unbalance at the input. This avoids the modification of the modulation index as is required in SVM technique. It is found that due to constant pulse width, the method has lower switching stresses on the power devices and allows the power devices to respond effectively.

The input current ripples in MESS technique are found to be relatively higher than SVM because of the error propagated over the constant sampling period. This method also requires more computational time compared to SVM. But this can be overcome by the use of parallel processing units. Simulation and hardware results validate the effectiveness of the proposed modulation strategy.

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Elimination of common mode voltage using phase shifted dual source matrix converter with improved modulation index

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Abstract

Purpose – The high-frequency common-mode voltage introduced by power converters, using conventional modulation techniques, results in common-mode current that has the potential to cause physical damage to the shaft and bearings of electric drives as well as unwanted tripping of ground fault relays in motor drives and electrical networks. The paper aims to provide a complete elimination of common mode voltage using a matrix converter (MC) with a new modulation strategy that reduces the size of the power converter system considerably. Further, a new MC topology is proposed to eliminate the common mode voltage with improved voltage transfer ratio (VTR).

Design/methodology/approach – The direct MC topology is selected, as it is the only converter topology that has the potential to eliminate common mode voltage in direct AC to AC systems. Using the rotating space vector technique, common mode voltage is eliminated but this reduces the VTR of the converter. To improve the VTR, a modified MC topology with a modified rotating space vector strategy is proposed. In addition, for improving the power factor at the input, the input current control strategy is developed.

Findings – The use of rotating space vector technique eliminates the common mode voltage even under all input abnormalities like unbalance and harmonics. By applying positive and negative rotating space vectors, input power factor control can be achieved. However, the control range is limited from unity power factor to the output power factor. It is observed that in the current controlled technique the modulation index reduces further. It is also found that there is a reduction in switching stresses of individual switches in proposed topology compared to direct MC topology.

Originality/value – In this paper, a modified rotating space vector technique is applied to the proposed converter topology for elimination of common mode voltage with an increased VTR. The topology can be used for common mode voltage elimination in existing electric drives without the need for modifying the drive system.

Keywords Matrix converter, Space vector modulation, Common mode voltage, Common mode current, Rotating space vector, Vectors, Voltage

Paper type Technical paper

COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering
Vol. 32 No. 6, 2013
pp. 2006-2026

0332-1649
DOI 10.1108/COMPEL-04-2012-0063

I. Introduction

The matrix converter (MC) is an array of 3×3 bidirectional switches functioning as a direct AC to AC converter. It directly interconnects two independent three-phase voltage systems at different frequencies. Alesina and Venturini (1989) introduced the mathematical formulation of modulation techniques for MC through direct transfer function approach (Venturini and Alesina, 1980), where output voltages were obtained by multiplication of modulation matrix with input voltages. Later, the optimum Alesina Venturini (OAV) method (Venturini and Alesina, 1989) was proposed, in which the voltage transfer ratio (VTR) was increased from 0.5 to 0.866 by using the third harmonic injection technique. Control technique using the "fictitious DC link", a conceptually different idea (Huber and Borojevic, 1995; Nielsen *et al.*, 1996), decoupled the control into smaller independent units. Scalar control modulation algorithm using MAX-MID-MIN PWM technique (Luca, 2007) avoided the sector information as required in the SVM technique. Today, MC research activity is in advanced topologies and applications issues such as reliable implementation of commutation strategies, over-voltage protection (Wheeler *et al.*, 2002), operation under abnormal conditions (Hotate and Masuse, 2004), reduction of common mode voltage and reduction of switching losses. Common-mode current has the potential to cause physical damage and unwanted tripping of ground fault relays in motor drives and electrical networks. Also, research has identified damages such as frosting; spark tracks in surface of balls, races and pitting of electric machines caused by bearing currents that flow due to common mode voltage (Adabi *et al.*, 2007). These currents are created by the common mode voltage applied to the machine by the inverter. In typical three-phase MC drives, there exists substantial common-mode voltage between the load neutral and the earth ground. As the modulation frequency increases and zero-sequence impedance of the machine decreases, the common mode voltage causes higher common-mode currents, worsening electromagnetic interference (EMI) problems and potentially damaging the network or the machine (Chen *et al.*, 1996). Different common mode voltage mitigating techniques such as PWM based (Cha and Prasad, 2003; Videt *et al.*, 2007; Lai, 1999; Nguyen and Lee, 2012), active and passive filter-based current injection for cancellation of common mode (Choochuan, 2005) have been proposed. The elimination of common mode voltage (Kanchan *et al.*, 2006) has been proposed for open ended winding-based induction drives fed by a three-level inverter. The same idea has been extended to direct and indirect MC fed three-phase open-ended winding AC machines (Gupta *et al.*, 2010; Tewari *et al.*, 2011). A high-frequency common-mode EMI model has also been proposed for direct MCs (Jordi *et al.*, 2011). In this paper, RSVM technique is used to eliminate the CMV with a VTR of 0.5 for direct AC to AC converter-fed induction machines. In addition, the phase-shifted dual source matrix converter topology (PDMC) is introduced that improves the VTR to 0.866. The performance of RSVM for CMC and PDMC under unbalanced and non-sinusoidal input conditions are analysed.

This paper discusses CMV elimination in MC with modified topology and its space vector modulation technique. In Section II, the rotating space vector modulation technique is developed for the CMC for elimination of CMV with a VTR of 0.5. Section III explains the method of input current control in RSVM. Section IV introduces a PDMC and its RSVM technique that improves the VTR to 0.866. In Section V, mathematical models of the PDMC and CMC are described and the simulation results of RSVM technique applied to CMC and PDMC using MATLAB/Simulink are presented.

II. Rotating space vector PWM for CMC

The CMC topology, shown in Figure 1(a), has been chosen in this work, as it is the only possible converter topology where the common mode voltage can be eliminated completely. Two constraints imposed on this converter are:

(1) input terminals should never be short-circuited; and

(2) output terminals should never be left open.

At any given instant, due to the first constraint, only two of the converter phases can conduct in an indirect matrix converter (AC-DC-AC back to back converter), as shown in Figure 1(b). This introduces common mode voltage since the circuit configuration allows only two input phases to connect to the three output phases; hence the neutral voltage V_n can never be equal to zero. Hence, the CMC topology is selected. The voltage across the star point of the load with respect to source neutral is given by equation (1) where, V_a, V_b, and V_c are the phase voltages of the load:

$$V_n = \frac{(V_a + V_b + V_c)}{3} \tag{1}$$

For any three-phase three-wire balanced system $V_N = 0$:

$$V_N = \frac{(V_A + V_B + V_C)}{3} \tag{2}$$

where V_A, V_B and V_C are the three-phase balanced input phase voltages. From equations (1) and (2), the sum of load voltages V_a, V_b and V_c should be equal to the sum of input phase voltages V_A, V_B and V_C for the load neutral voltage V_n to be equal to 0. Hence, elimination of common mode voltage introduces a third additional constraint in the CMC, namely at any given instant all the three input phases must be connected to the load. The above three conditions can be combined to a single constraint namely, at any given instant, all the three phases of the source must be connected to different phases of the load. This additional constraint, used for elimination of common mode voltage, allows the use of only six switching vectors from the valid 27 vectors of the

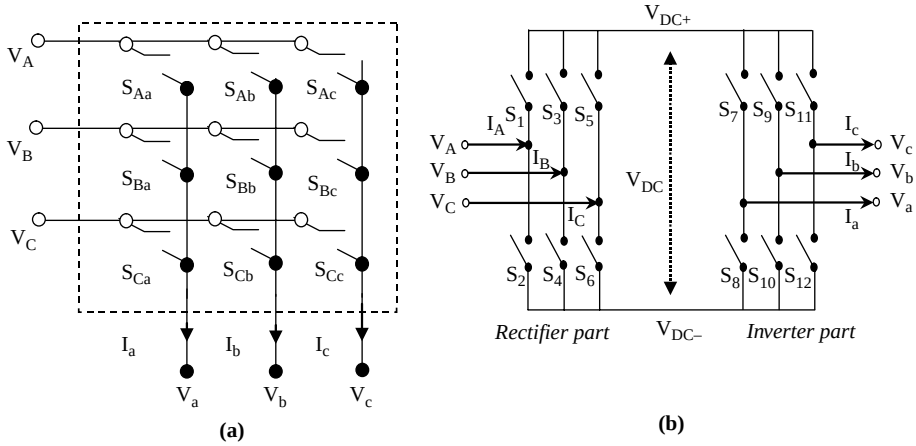


Figure 1.
(a) Conventional MC and (b) indirect MC

MC that connect all the input phases to the output phases, as shown in Figure 2. The remaining valid vectors that are not used are the 18 stationary vectors and the three zero vectors. The six vectors that are used are termed as rotating space vectors since their position in space is not fixed. Out of these six rotating space vectors, three space vectors rotate in the direction of the output frame and the remaining three rotate in the direction opposite to the rotating output reference frame. Switching patterns for the counter-clockwise rotating vectors are given in equation (3):

$$\begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \text{ or } \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \text{ or } \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \quad (3)$$

The output space vector is shown in Figure 3(a), when any of the three possible switching patterns given in equation (3) are employed.

Switching space vectors rotate at input frequency ω_s rad/s while the output reference space vector rotates at ω_o rad/s. Determination of duty cycles for switching

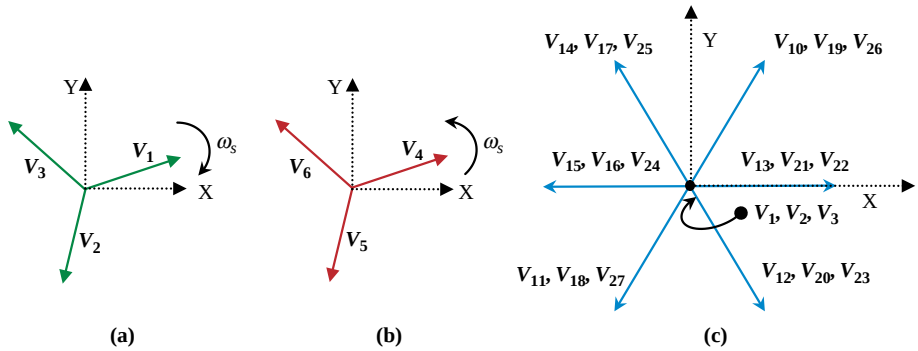


Figure 2.
(a) Clockwise rotating vectors, (b) counter-clockwise rotating vectors and (c) stationary vectors

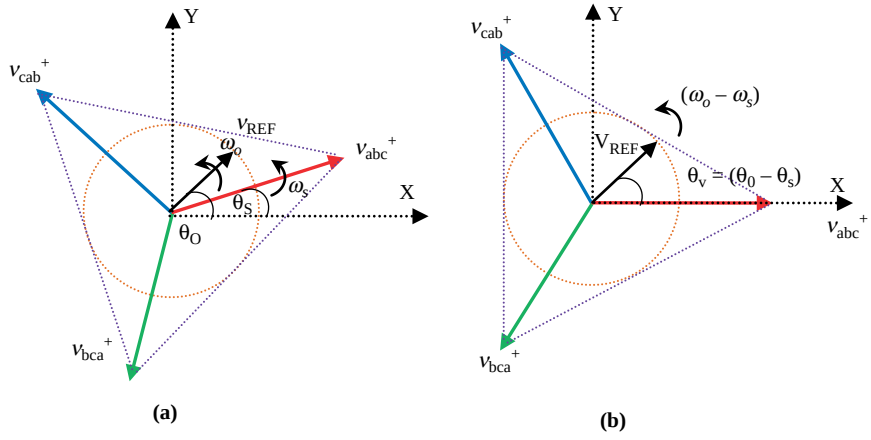


Figure 3.
Dynamic space vector PWM

Notes: (a) Positive sequence rotating reference frame; (b) fixed reference

space vectors that rotates is tedious. Hence, the switching vectors rotating at ω_s is taken as the reference and the relative angle θ_v between the output reference voltage vector angle θ_o and the actual switching voltage space vector angle θ_s, as shown in Figure 3(a), is computed and used in duty cycle calculation, as shown in Figure 3(b). The positions of active switching voltage vectors and reference output voltage vector in space are given by equations (4) and (5):

$$v^{+}_{abc} = \frac{3}{2}V_i{*}e^{j\omega_s t}, \quad v^{+}_{cab} = \frac{3}{2}V_i{*}e^{j(\omega_s t+(2\pi/3))}, \quad v^{+}_{bca} = \frac{3}{2}V_i{*}e^{j(\omega_s t-(2\pi/3))} \tag{4}$$

$$v_o = \frac{3}{2}V_o{*}e^{j\omega_0 t} \tag{5}$$

where, $v^{+}_{abc}, v^{+}_{cab}, v^{+}_{bca}$ are active vectors with magnitudes V_i and v_o is the output vector with magnitude V_o. Using sine law of triangles, as shown in Figure 4, the duty cycles of active vectors and zero vectors are computed, as given by equations (6)-(9). As shown in Figure 3(b), the angle between two active vectors is 120° with relative angle $\theta_v = \theta_o - \theta_s$:

$$\frac{d_\alpha v_\alpha}{\sin(120^\circ - \theta_v)} = \frac{d_\beta v_\beta}{\sin(\theta_v)} = \frac{V_{o(REF)}}{\sin(60^\circ)} \tag{6}$$

$$d_\alpha = m_v \sin(120^o - \theta_v) \tag{7}$$

$$d_\beta = m_v \sin(\theta_v) \tag{8}$$

$$d_0 = 1 - d_\alpha - d_\beta \tag{9}$$

where, $m_v = (2V_o/\sqrt{3}V_i)$ and v_α, v_β are arbitrary vectors of a given sector. Conventional SVM technique utilizes zero vectors for sinusoidal output but in the proposed RSVM technique, the use of zero vectors introduces common mode voltage. From equation (4) it can be shown that $d_m v^{+}_{abc} + d_m v^{+}_{cab} + d_m v^{+}_{bca} = 0$, where d_m is some arbitrary duty cycle. This idea is used to achieve sinusoidal output and eliminate common mode voltage. During the zero vector switching time, RSVM technique uses all three active vectors with equal duty ratio. The modified duty ratios for the RSVM technique are given by equations (10)-(12):

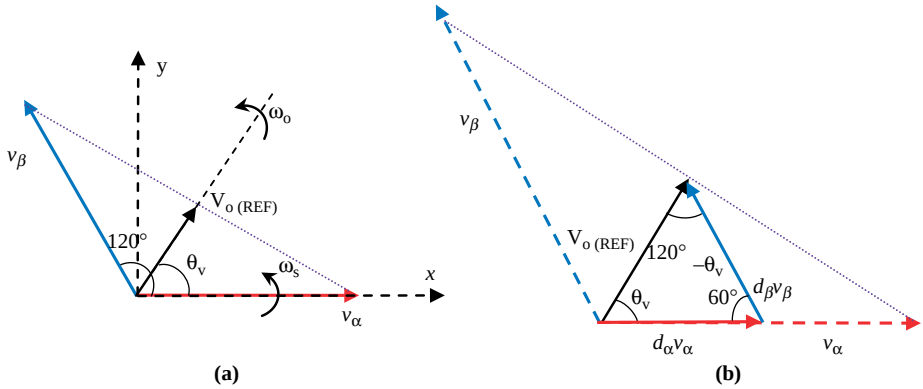


Figure 4.
Duty cycle calculation

Notes: (a) Sector 1; (b) weighted combination of active vectors

$$d_1^+ = d'_\alpha = m_v \sin(120^o - \theta_v) + \frac{d_0}{3} \tag{10}$$

$$d_2^+ = d'_\beta = m_v \sin(\theta_v) + \frac{d_0}{3} \tag{11}$$

$$d_3^+ = d'_0 = \frac{d_0}{3} \tag{12}$$

Hence, within any given sector, the required output can be synthesized over a sampling period by applying the respective active rotating vector, as given in Table I. The output voltage is related to active vectors, the duty cycles of which are given in equation (13), which satisfies equation (14) at all times:

$$v_o = d_1^+ v_1 + d_2^+ v_2 + d_3^+ v_3 \tag{13}$$

$$d_1^+ + d_2^+ + d_3^+ = 1 \tag{14}$$

where, d_1^+, d_2^+, d_3^+ and v_1, v_2, and v_3 are, respectively, the duty cycles and the active positive rotating vectors. The duty cycle of each switch is directly obtained in equations (15)-(17) by substituting equations (4) and (5) in equations (13) and (14). The modulation index m_v of this method is limited to 0.5:

$$D_{Aa} = D_{Bb} = D_{Cc} = \frac{1}{3} + \frac{2m_v}{3} \cos(\omega_o t - \omega_s t) \tag{15}$$

$$D_{Ba} = D_{Cb} = D_{Ac} = \frac{1}{3} + \frac{2m_v}{3} \cos\left((\omega_o t - \omega_s t) + \frac{2\pi}{3}\right) \tag{16}$$

$$D_{Ca} = D_{Ab} = D_{Bc} = \frac{1}{3} + \frac{2m_v}{3} \cos\left((\omega_o t - \omega_s t) - \frac{2\pi}{3}\right) \tag{17}$$

With a similar procedure, the same output voltage can be synthesized using the three negative rotating active space vectors, duty ratios of which are given by equations (10)-(13). Within any given sector, the required output can be synthesized by applying the respective active rotating vector, as given in Table II, for the computed duty cycle period, given in equation (13).

III. Input power factor control in RSVM

Input power factor control in direct AC to AC converters (Milanovic and Dobaj, 2000) is carried out using the principle of space vector technique applied to input current but the RSVM technique uses the shared duty ratio control technique for achieving the same. At any instant, based on the applied active voltage space vector at the output, any of the

S. no.	θ_v	Sector no.	Active vectors v_1	v_2	v_3
1	$0° < \theta_v \leq 120°$	1	v^+_{abc}	v^+_{cab}	v^+_{bca}
2	$120° < \theta_v \leq 240°$	2	v^+_{cab}	v^+_{bcc}	v^+_{abc}
3	$240° < \theta_v \leq 360°$	3	v^+_{bca}	v^+_{abc}	v^+_{cab}

Table I. Positive rotating switching vectors and sector no. for CMC

input phase currents (say $i_a(t)$) should be equal to any one of the output phase currents ($i_A(t)$, $i_B(t)$ or $i_C(t)$). The positions of active output current vectors, when using the corresponding positive directional rotating voltage vectors and the input current vector in space are given by equations (18) and (19):

$$i^{+}_{abc} = \frac{3}{2} I_o * e^{j(\omega_0 t - \rho)}, \quad i^{+}_{cab} = \frac{3}{2} I_o * e^{j(\omega_o t - \rho + (2\pi/3))}, \quad i^{+}_{bca} = \frac{3}{2} I_o * e^{j(\omega_o t - \rho - (2\pi/3))} \tag{18}$$

$$i_s = \frac{3}{2} I_o * e^{j(\omega_s t - \rho)} \tag{19}$$

The positions of active output current vector, when using the corresponding negative directional rotating voltage vectors and the input current vector in space, are given by equations (20) and (21):

$$i^{-}_{acb} = \frac{3}{2} I_o * e^{-j(\omega_0 t - \rho)}, \quad i^{-}_{bac} = \frac{3}{2} I_o * e^{-j(\omega_o t - \rho + (2\pi/3))}, \quad i^{-}_{cba} = \frac{3}{2} I_o * e^{-j(\omega_o t - \rho - (2\pi/3))} \tag{20}$$

$$i_s = \frac{3}{2} I_o * e^{j(\omega_s t + \rho)} \tag{21}$$

It can be seen from equations (19) and (21) that the input current lags or leads the input voltage by ρ degrees when positive or negative directional voltage vectors are, respectively, applied, where cos ρ lagging is the output load power factor, as shown in Figure 5(a). Since the output power factor depends upon the load, it is not possible to control the output power factor. Hence, the only way to control the input power factor, cos ϕ, is to apply both + ve and − ve rotating voltage space vectors at the output terminals, as shown in Figure 5(b)-(d). The proportion in which the + ve and − ve rotating voltage space vectors are applied decides the input power factor, as given in equation (22). However, the input power factor can be controlled in a limited range between output power factor and unity, i.e. $\cos\rho < \cos\phi < 1$. The duty cycle of each switch is given by equations (23)-(31):

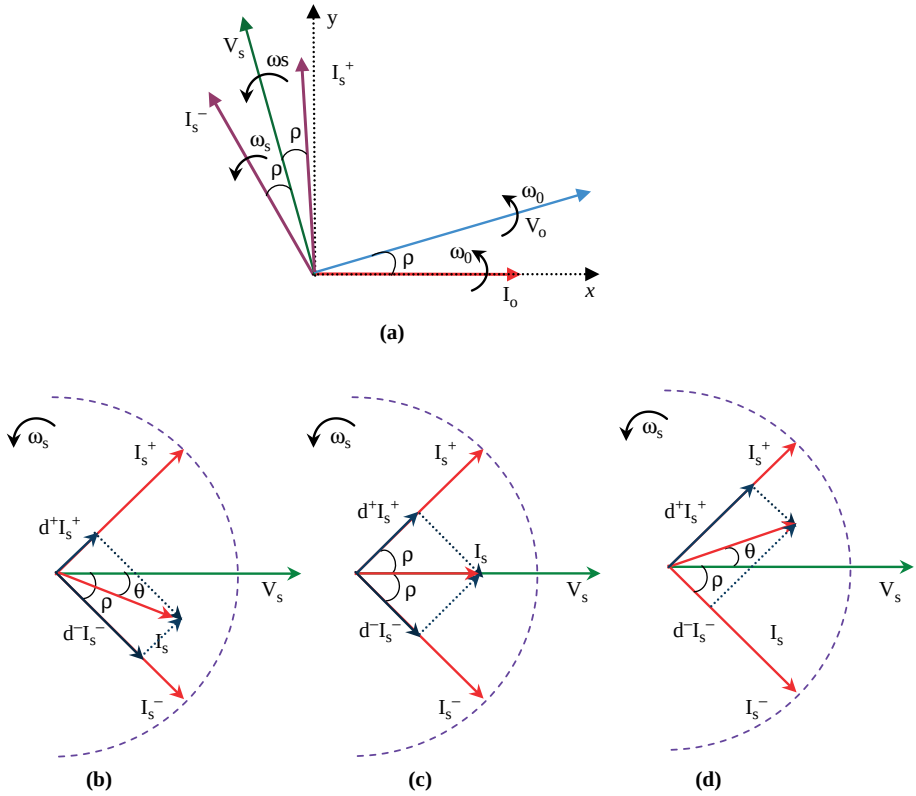
$$\theta = \tan^{-1}\{(1 - 2d^{+})\tan\rho\} \tag{22}$$

$$D_{Aa} = \frac{1}{3} + \frac{2r\, m_v}{3} \cos(\omega_o t - \omega_s t) + \frac{2(1 - r)\, m_v}{3} \cos(\omega_o t + \omega_s t) \tag{23}$$

$$D_{Ba} = \frac{1}{3} + \frac{2r m_v}{3} \cos\left((\omega_o t - \omega_s t) + \frac{2\pi}{3}\right) + \frac{2(1 - r)\, m_v}{3} \cos\left((\omega_o t + \omega_s t) - \frac{2\pi}{3}\right) \tag{24}$$

Table II. Negative rotating switching vectors and sector no. for CMC

S. no.	θ_v	Sector no.	Active vectors v_1	v_2	v_3
1	$0° < \theta_v \leq 120°$	1	v^{-}_{acb}	v^{-}_{bac}	v^{-}_{cba}
2	$120° < \theta_v \leq 240°$	2	v^{-}_{bac}	v^{-}_{cba}	v^{-}_{acb}
3	$240° < \theta_v \leq 360°$	3	v^{-}_{cba}	v^{-}_{acb}	v^{-}_{bac}



Notes: (a) Input current positions; (b) lagging power factor ($d^+ < d^-$); (c) unity power factor ($d^+ = d^-$); (d) leading power factor ($d^- d^+$)

Figure 5.
Input power factor control

$$D_{Ca} = \frac{1}{3} + \frac{2r\,m_v}{3}\cos\left((\omega_o t - \omega_s t) - \frac{2\pi}{3}\right) + \frac{2(1-r)\,m_v}{3}\cos\left((\omega_o t + \omega_s t) + \frac{2\pi}{3}\right) \tag{25}$$

$$D_{Bb} = \frac{1}{3} + \frac{2r\,m_v}{3}\cos(\omega_o t - \omega_s t) + \frac{2(1-r)\,m_v}{3}\cos\left((\omega_o t + \omega_s t) + \frac{2\pi}{3}\right) \tag{26}$$

$$D_{Cb} = \frac{1}{3} + \frac{2rm_v}{3}\cos\left((\omega_o t - \omega_s t) + \frac{2\pi}{3}\right) + \frac{2(1-r)\,m_v}{3}\cos(\omega_o t + \omega_s t) \tag{27}$$

$$D_{Ab} = \frac{1}{3} + \frac{2rm_v}{3}\cos\left((\omega_o t - \omega_s t) - \frac{2\pi}{3}\right) + \frac{2(1-r)\,m_v}{3}\cos\left((\omega_o t + \omega_s t) - \frac{2\pi}{3}\right) \tag{28}$$

$$D_{Cc} = \frac{1}{3} + \frac{2rm_v}{3}\cos(\omega_o t - \omega_s t) + \frac{2(1-r)\,m_v}{3}\cos\left((\omega_o t + \omega_s t) - \frac{2\pi}{3}\right) \tag{29}$$

$$D_{Ac} = \frac{1}{3} + \frac{2rm_v}{3}\cos\left((\omega_o t - \omega_s t) + \frac{2\pi}{3}\right) + \frac{2(1-r)\,m_v}{3}\cos\left((\omega_o t + \omega_s t) + \frac{2\pi}{3}\right) \quad (30)$$

$$D_{Bc} = \frac{1}{3} + \frac{2rm_v}{3}\cos\left((\omega_o t - \omega_s t) - \frac{2\pi}{3}\right) + \frac{2(1-r)\,m_v}{3}\cos(\omega_o t + \omega_s t) \quad (31)$$

Let T^+ be the time for which the positive rotating space vectors are applied and T^- be the time for which the negative rotating space vectors are applied within a given sampling time T_s. The respective duty ratios are d^+ and d^-, which satisfy the relation $d^+ + d^- = 1$ at all times. The input power angle θ is given by equation (22).

IV. Rotating space vector PWM (RSVM) for PDMC

The RSVM for CMC uses only three vectors with the modulation index limited to 0.5, which is the major limitation of RSVM. The short coming of this strategy is overcome by using a 6×3 MC composed of two 3×3 MCs [MC_x, MC_y] fed by a three-phase center-tapped transformer. The transformer produces 180° shifted space vector pattern by generating a six phase supply as shown in Figure 6. In the proposed topology, the modulation index is increased to 0.866 with the help of the newly available three space vectors as shown in Figure 7. The six switching patterns for the counter-clockwise rotating space vectors are given by equations (32) and (33), where, all the elements of S_{MC_x} are equal to 0 if any one switching sequence of S_{MC_y} is applied. Similarly, all the elements of S_{MC_y} are equal to 0 if any one switching sequence of S_{MC_x} is applied:

$$S_{MC\_x} = \begin{bmatrix} S_{Aax} & S_{Abx} & S_{Acx} \\ S_{Bax} & S_{Bbx} & S_{Bcx} \\ S_{Cax} & S_{Cbx} & S_{Ccx} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \text{or} \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \text{or} \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad (32)$$

$$S_{MC\_y} = \begin{bmatrix} S_{Aay} & S_{Aby} & S_{Acy} \\ S_{Bay} & S_{Bby} & S_{Bcy} \\ S_{Cay} & S_{Cby} & S_{Ccy} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \text{or} \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \text{or} \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad (33)$$

The positions of active switching voltage space vectors and the reference output voltage space vector are given by equations (34) and (35):

$$\begin{aligned} v_{abc_x^+} &= \frac{3}{2}V_i * e^{j\omega_s t}, \quad v_{cab_x^+} = \frac{3}{2}V_i * e^{j(\omega_s t + (2\pi/3))}, \quad v_{bca_x^+} = \frac{3}{2}V_i * e^{j(\omega_s t - (2\pi/3))} \\ v_{abc_y^+} &= \frac{3}{2}V_i * e^{j(\omega_s t + \pi)}, \quad v_{cab_y^+} = \frac{3}{2}V_i * e^{j(\omega_s t + (\pi/3))}, \quad v_{bca_y^+} = \frac{3}{2}V_i * e^{j(\omega_s t + (\pi/3))} \end{aligned} \quad (34)$$

$$v_o = \frac{3}{2}V_o * e^{j\omega_0 t} \quad (35)$$

where $v_{abc_x^+}, v_{cab_x^+}, v_{bca_z^+}$ and $v_{abc_y^+}, v_{cab_y^+}, v_{bca_y^+}$ are, respectively, the active positive rotating switching vectors corresponding to S_{MC_x} and S_{MC_y}. V_i&V_o. are the magnitudes of input and output space vectors, respectively. The duty cycles of active vectors and zero vector are computed using sine law of triangles, as explained in

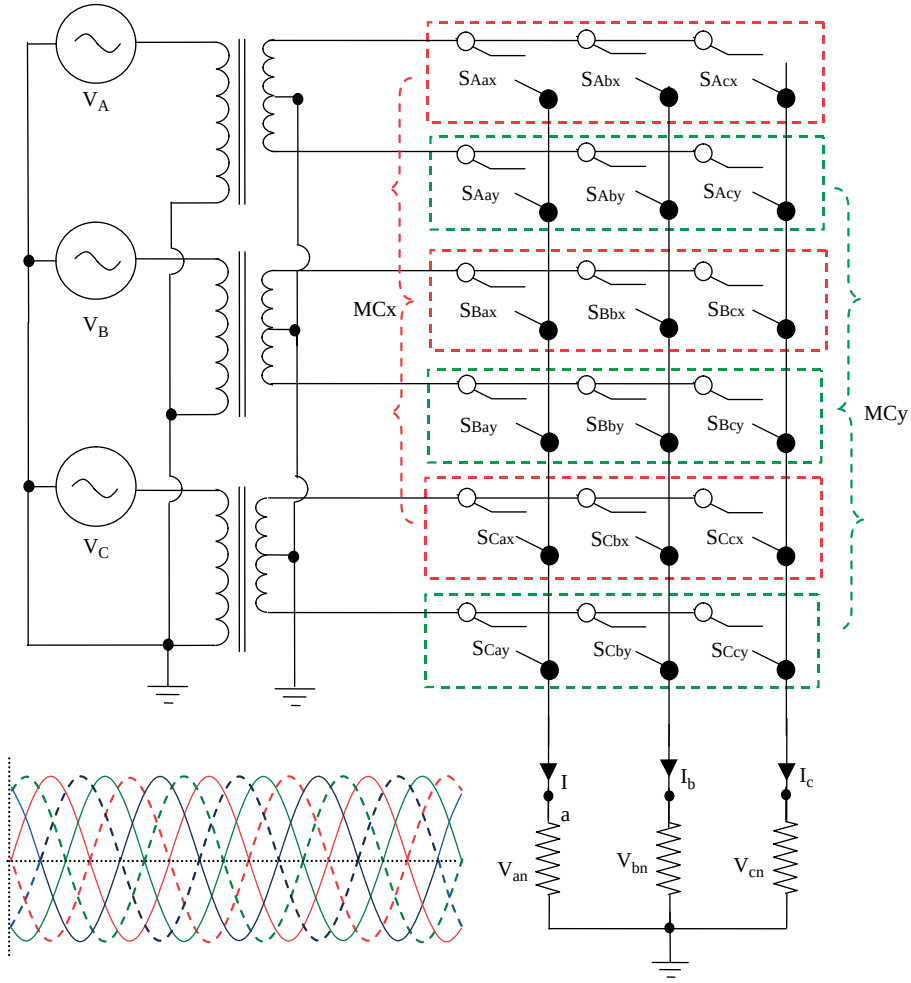


Figure 6.
Phase shifted dual source matrix converter

Section II, and given by equation (36), with the angle between the two active vectors being 60° and the relative angle $\theta_v = \theta_o - \theta_s$.

$$d_\alpha = m_v \sin(60^o - \theta_v), \quad d_\beta = m_v \sin(\theta_v), \quad d_0 = 1 - d_\alpha - d_\beta \tag{36}$$

where, $m_v = (2V_o/\sqrt{3}V_i)$ and v_α, v_β are arbitrary vectors in a given sector. As explained in Section II, this technique does not utilize zero vectors. From equations (34) and (35), it can be shown that $d_m\, v_{abc_x^+} + d_m\, v_{abc_y^+} = 0$, where d_m is some arbitrary duty cycle. To achieve sinusoidal output and eliminate common mode voltage, RSVM technique utilizes two opposite active vectors in equal ratio within the zero switching time that modifies the duty ratios as given by equation (37):

$$d_1^+ = d_\alpha, \quad d_2^+ = d_\beta + \frac{d_0}{2}, \quad d_3^+ = \frac{d_0}{2} \tag{37}$$

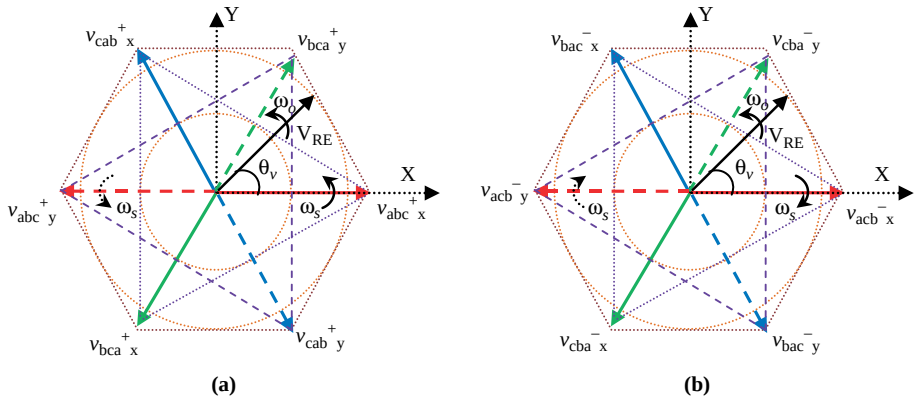


Figure 7.
Space vector distribution of PDMC

Notes: (a) + ve sequence vectors; (b) – ve sequence vectors

Hence, within any given sector, the required output can be synthesized by applying the respective active rotating vectors, as given in Table III, for the computed duty cycle given in equation (38):

$$v_o = d_1^+ v_1 + d_2^+ v_2 + d_3^+ v_3 \tag{38}$$

where, d_1^+, d_2^+, d_3^+ and v_1, v_2, v_3 are, respectively, the duty cycles and the active voltage vectors. As described in Section II, the same output voltage can be obtained using the negative rotating space vectors, as shown in Figure 7(b). Within any given sector, the required output can be synthesized by applying the respective active rotating vectors, as given in Table IV, for the computed duty cycle given in equation (37).

In a similar manner, as described in Section II, the ratio in which the + ve and − ve rotating voltage space vectors are applied decides the input power factor at the primary of the center tapped transformer, as given by equation (22).

It is also observed that the input power factor control reduces the magnitude of the input current, as shown in Figure 8, by a factor given in equation (39):

$$\frac{|I_{s\_c}|}{|I_s^+|} = \frac{\cos\rho}{\cos\left(\tan^{-1}\{(1-2d^+)\tan\rho\}\right)} \tag{39}$$

where, $|I_{s\_c}\|$, $|I_s^+|$ are, respectively, the peak magnitude of the controlled input current and the peak magnitude of the uncontrolled input current of the MC.

Table III.
Positive rotating switching vectors and sector no. for PDMC

S. no.	θ_v	Sector no.	Active vectors v_1	v_2	v_3
1	$0° < \theta_v \leq 60°$	1	$v_{abc_x^+}$	$v_{bca_y^+}$	$v_{bca_x^+}$
2	$60° < \theta_v \leq 120°$	2	$v_{bca_y^+}$	$v_{cab_x^+}$	$v_{cab_y^+}$
3	$120° < \theta_v \leq 180°$	3	$v_{cab_x^+}$	$v_{abc_y^+}$	$v_{abc_x^+}$
4	$180° < \theta_v \leq 240°$	4	$v_{abc_y^+}$	$v_{bca_x^+}$	$v_{bca_y^+}$
5	$240° < \theta_v \leq 300°$	5	$v_{bca_x^+}$	$v_{cab_y^+}$	$v_{cab_x^+}$
6	$300° < \theta_v \leq 360°$	6	$v_{cab_y^+}$	$v_{abc_x^+}$	$v_{abc_y^+}$

From equation (39) it is observed that the modulation index at the output of the MC reduces by the same factor as described in equation (40):

$$m_{v\_c} = \frac{\cos\rho}{\cos\left(\tan^{-1}\{(1-2d^{+})\tan\rho\}\right)} m_v \quad (40)$$

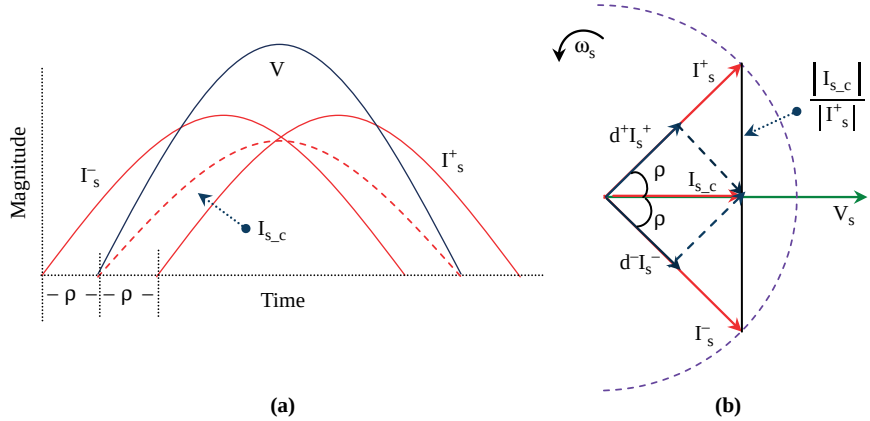
V. Simulation results

Simulation of CMC and the proposed PDMC was carried out using mathematical models, as shown in Figures 9 and 10, and also verified using ideal switches. The system parameters used in the simulation were: supply – 220 V, 50 Hz, Load – $R = 5\,\Omega$, $L = 20.73$ mH, cos $\rho = 0.8$ at 25 Hz output frequency and switching frequency of 10 kHz. The input filter capacitance and inductance is designed to be $C_f = 10\,\mu F$ and $L_f = 1$ mH with a damping resistor $r_d = 50\,\Omega$ (She *et al.*, 2009; Imayavaramban, 2008) for filtering the higher order frequencies very near the switching frequency. The absence of passive freewheeling paths for the load makes the PDMC hard to handle the commutation behaviour; hence the four-step commutation method (Muroya and Shinohara, 2001) is used in the RSVM technique.

The mathematical model of PDMC can be implemented using two three-phase AC voltage regulators connected to a single MC, as shown in Figure 10. Although this

S. no.	θ_v	Sector no.	Active vectors v_1	v_2	v_3
1	$0° < \theta_v \leq 60°$	1	$v_{acb_x}^-$	$v_{cba_y}^-$	$v_{cab_x}^-$
2	$60° < \theta_v \leq 120°$	2	$v_{cba_y}^-$	$v_{bac_x}^-$	$v_{bca_y}^-$
3	$120° < \theta_v \leq 180°$	3	$v_{bac_x}^-$	$v_{acb_y}^-$	$v_{acb_x}^-$
4	$180° < \theta_v \leq 240°$	4	$v_{acb_y}^-$	$v_{cba_x}^-$	$v_{cba_y}^-$
5	$240° < \theta_v \leq 300°$	5	$v_{cba_x}^-$	$v_{bac_y}^-$	$v_{bac_x}^-$
6	$300° < \theta_v \leq 360°$	6	$v_{bac_y}^-$	$v_{acb_x}^-$	$v_{acb_y}^-$

Table IV.
Negative rotating switching vectors and sector no. for PDMC



(a) (b)

Figure 8.
Input current magnitude for unity power factor

Notes: (a) Instantaneous; (b) vector

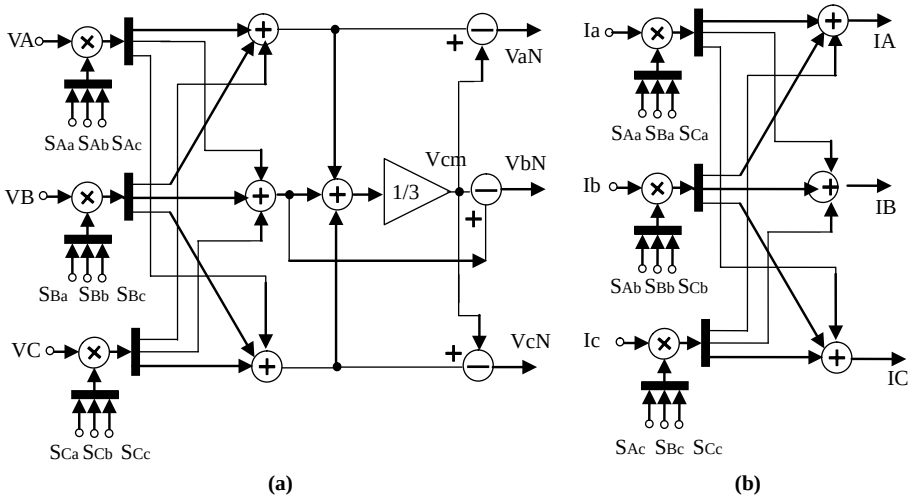


Figure 9.
Mathematical model of CMC

Notes: (a) Voltage model; (b) current model

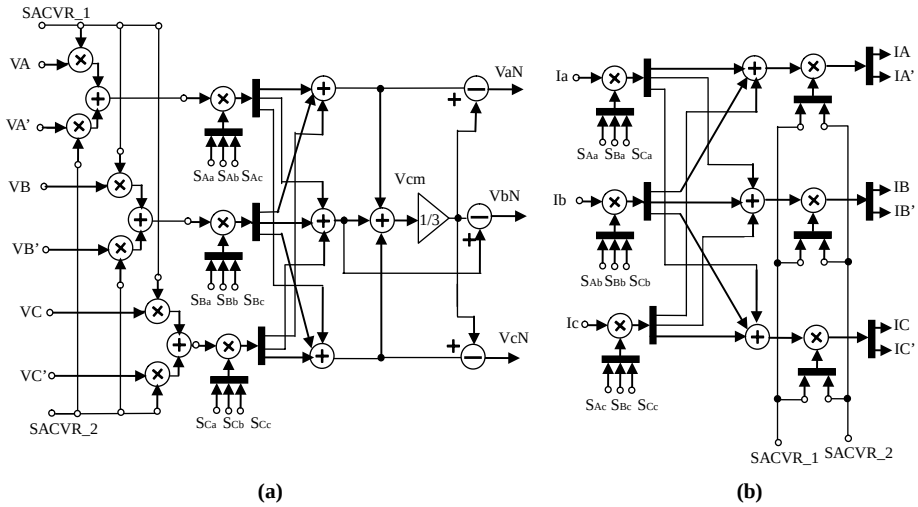


Figure 10.
Mathematical model of PDMC

Notes: (a) Voltage model; (b) current model

topology reduces the switch count by three, it operates with three additional devices during conduction, which increases the switching losses by 100 per cent. Hence, the proposed topology with a 6×3 MC appears superior. The block diagram representation of the rotating space vector modulation technique for PDMC is shown in Figure 11.

Figure 12(a)-(f) shows the simulation results of the CMC modulated using RSVM for modulation index of 0.5 and Figure 12(g)-(l) show the simulation results of the CMC modulated using RSVM with current control for modulation index of 0.5.

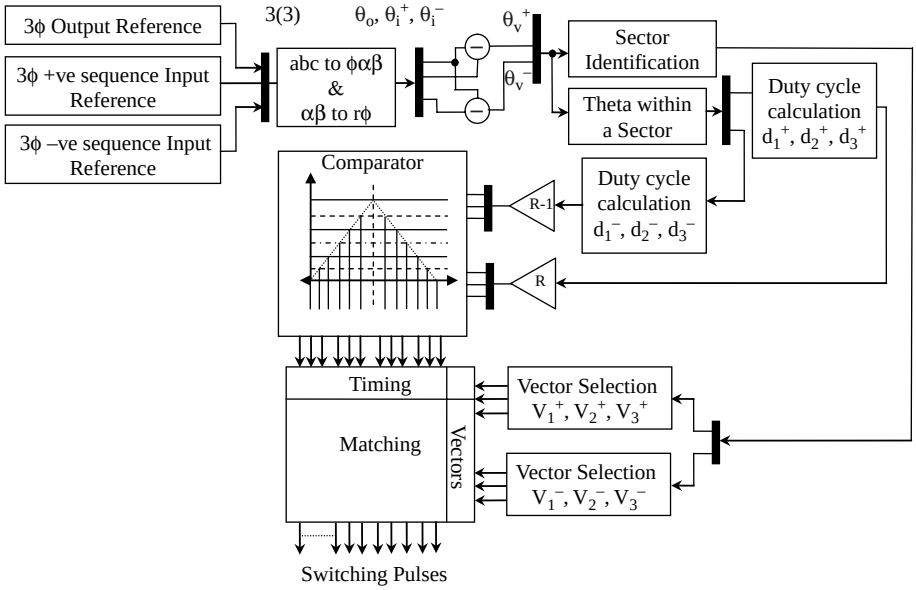


Figure 11.
Block diagram of the proposed current controlled RSVM strategy

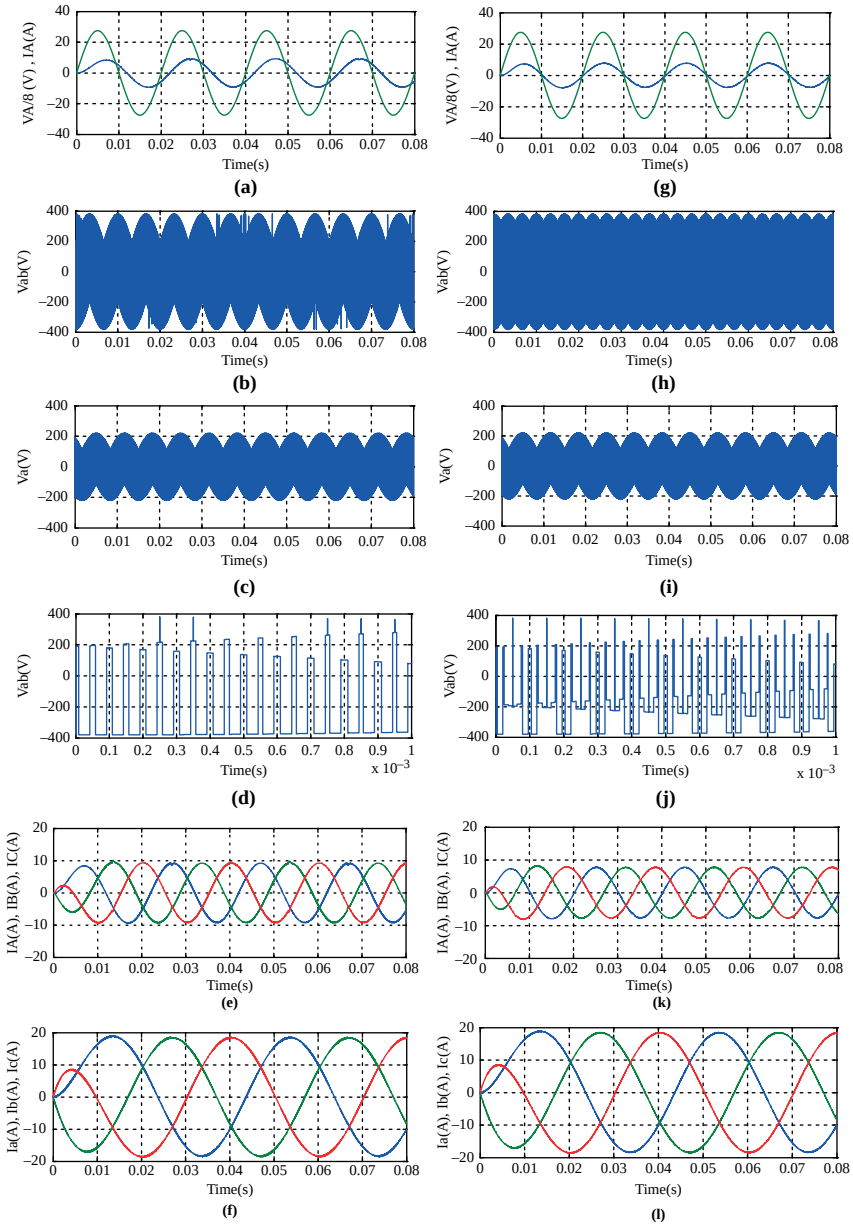
Figure 13(a)-(f) represent the simulation results of the PDMC modulated without current control and Figure 13(g)-(l) show the simulation results of the PDMC modulated with current control. The modulation index of the PDMC modulated with RSVM increases by 73.2 per cent as compared to modulation index of the CMC modulated by RSVM, as shown in Figures 3 and 7. The improved performance in load current can be observed in the peak magnitude that increases by approximately 73 per cent, as shown in Figures 12(l) and 13(l).

It can be seen from Figures 12(d), (j), and 13(d), (j) that the output voltage consists of three levels when positive rotating vectors are applied and consists of six levels when both positive and negative vectors are applied. This indicates that the number of switching states increases using current control technique for unity power factor, as required, in most of the cases. It can be seen from Figures 12(a), and (g), 13(a), (g) that the input peak current reduces approximately by a factor given in equation (30), for PDMC modulated by RSVM with current control.

From Figures 12(h) and 13(h), it can be observed that the voltage stresses on the devices are more in CMC topology than in the RSVM technique as the voltage has to change its state between + ve line voltage and − ve line voltage at all times whereas in the PDMC topology this does not take always place.

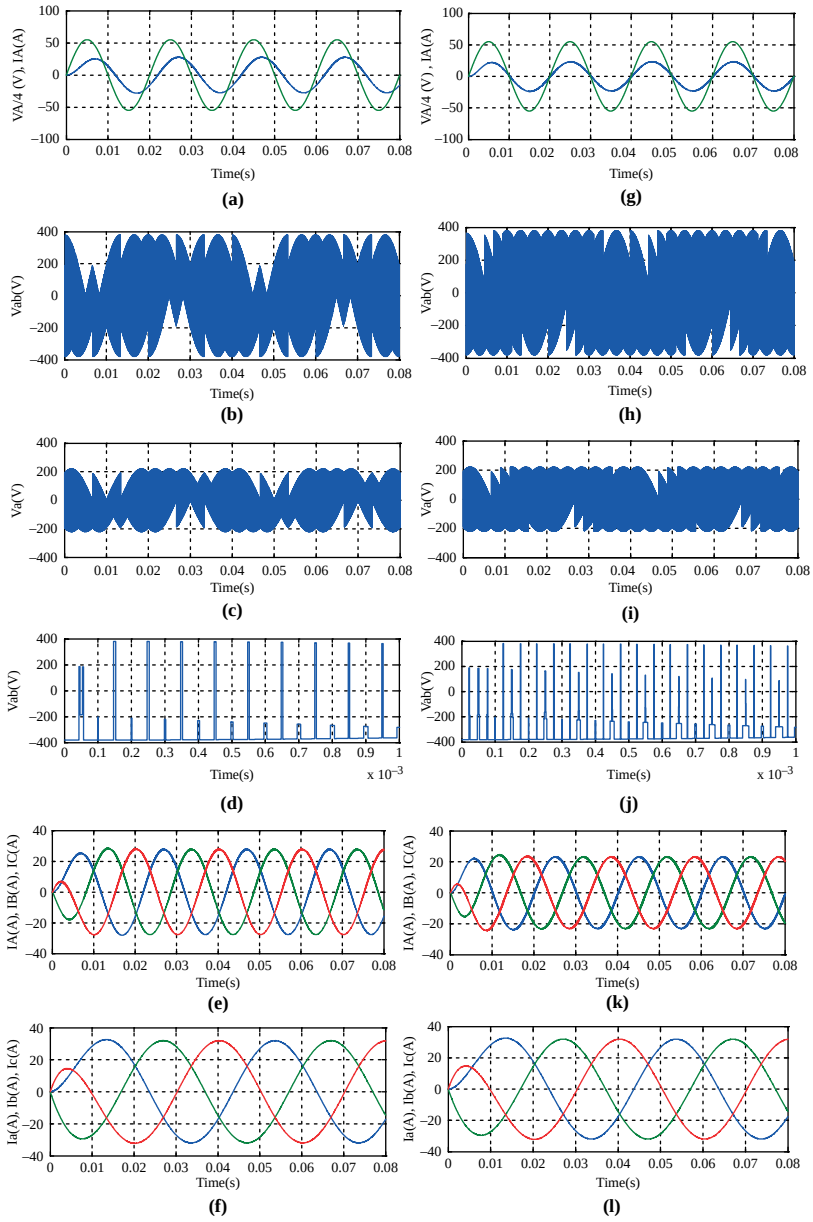
Figure 14(a) shows the common mode voltage induced due to space vector PWM in CMC and Figure 14(b) shows the common mode voltage induced in the RSVM technique for both CMC and PMDC. The peak of the common mode voltage can be as high as the magnitude of input phase voltage in space vector technique. This has been completely eliminated in the proposed switching strategy with input current control.

Figure 15 shows the simulation results of the PDMC connected to a three-phase, 400 V, 50 Hz, 1,430 rpm, 4 KW induction motor (IM). The reference speed of the IM is increased from zero to its rated value and is operated under no-load till 0.6 s. From 0.6 to 1 s, the IM is operated under load of 7 N-m. The reference speed is set to 54 per cent of its rated speed



Notes: (a)-(f) Without current control and (g)-(l) with current control; (a) and (g) input current and voltage, respectively; (b) and (h) output line voltage; (c) and (i) output phase voltage; (d) and (j) output line voltage magnified; (e) and (k) input currents; (f) and (l) output currents

Figure 12.
RSVM for CMC



Notes: (a)-(f) Without current control and (g)-(l) with current control; (a) and (g) input current and voltage, respectively; (b) and (h) output line voltage; (c) and (i) output phase voltage; (d) and (j) output line voltage magnified; (e) and (k) input currents; (f) and (l) output currents

Figure 13.
RSVM for PDMC

at 1 s, as shown in Figure 15(a). Figure 15(b) shows the variation of current in the IM. It can be seen from Figure 15(c) that the input power factor is controlled under all dynamic and steady state conditions for the RSVM-based vector control technique. Figure 15(d) shows the elimination of common mode voltage for load disturbances and set point variations.

An unbalance of 4.3 per cent in the B phase of the input voltage is applied to the CMC and the PDMC, as shown in Figure 16(a). Figure 16(b) shows that a low magnitude, low frequency CMV, proportional to the magnitude of the unbalance, is present in the CMC. However, In PDMC, the space vectors of the phase shifted MC introduce a low magnitude, high-frequency CMV, as shown in Figure 16(c).

A third harmonic (homopolar) component is injected in the input from 0.04 to 0.08 s and a second harmonic (non-homopolar) component is injected from 0.08 to 0.12 s as shown in Figure 17(a). Figure 17(b) and (c) shows the elimination of CMV for non-homopolar harmonics while homopolar harmonics introduce zero sequence voltages, which contribute to CMV.

As the number of branches increases, as in the case of PDMC, the current and voltage stresses are shared among the branches equally hence reducing the stresses on each device and extending the life of the device. If one of the arms fails to conduct, PDMC can be made to operate as CMC with reduced common mode voltage by optimal vector selection in SVM method. Considering the economic aspect, the solution for common mode voltage elimination seems to be costly. However, with the advances in power semiconductor devices technology, the cost of the devices is expected to reduce. Although the design looks expensive, the advantages of the design compensates for the cost.

VI. Conclusion

PDMC topology has twice the number of switches as compared to the CMC topology. However, it is the only possible configuration, in direct AC to AC converters, to eliminate common mode voltage with an increased modulation index of 0.866. It is found that in the RSVM technique, current control can be carried out using both positive and negative rotating vectors. RSVM also eliminates the CMV for inputs having non-homopolar harmonics. However, it does not eliminate the CMV for unbalanced inputs or inputs with homopolar harmonics.

The PDMC topology can also be constructed using two AC voltage regulators and one MC which reduces the switch count by one-sixth of the proposed topology. However, the proposed topology exhibits superior performance because of the decreased conduction losses of 50 per cent. However, the control range of PDMC and

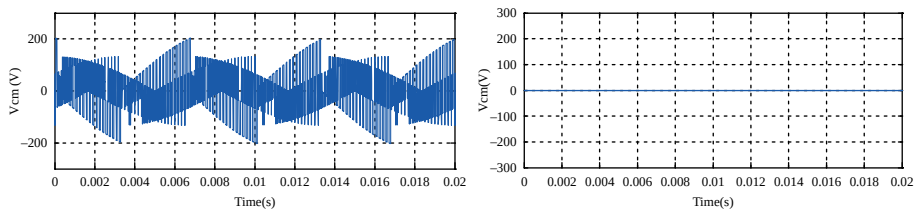


Figure 14.
Common mode voltage

Notes: (a) SVM modulated CMC; (b) RSVM modulated CMC (or) PDMC

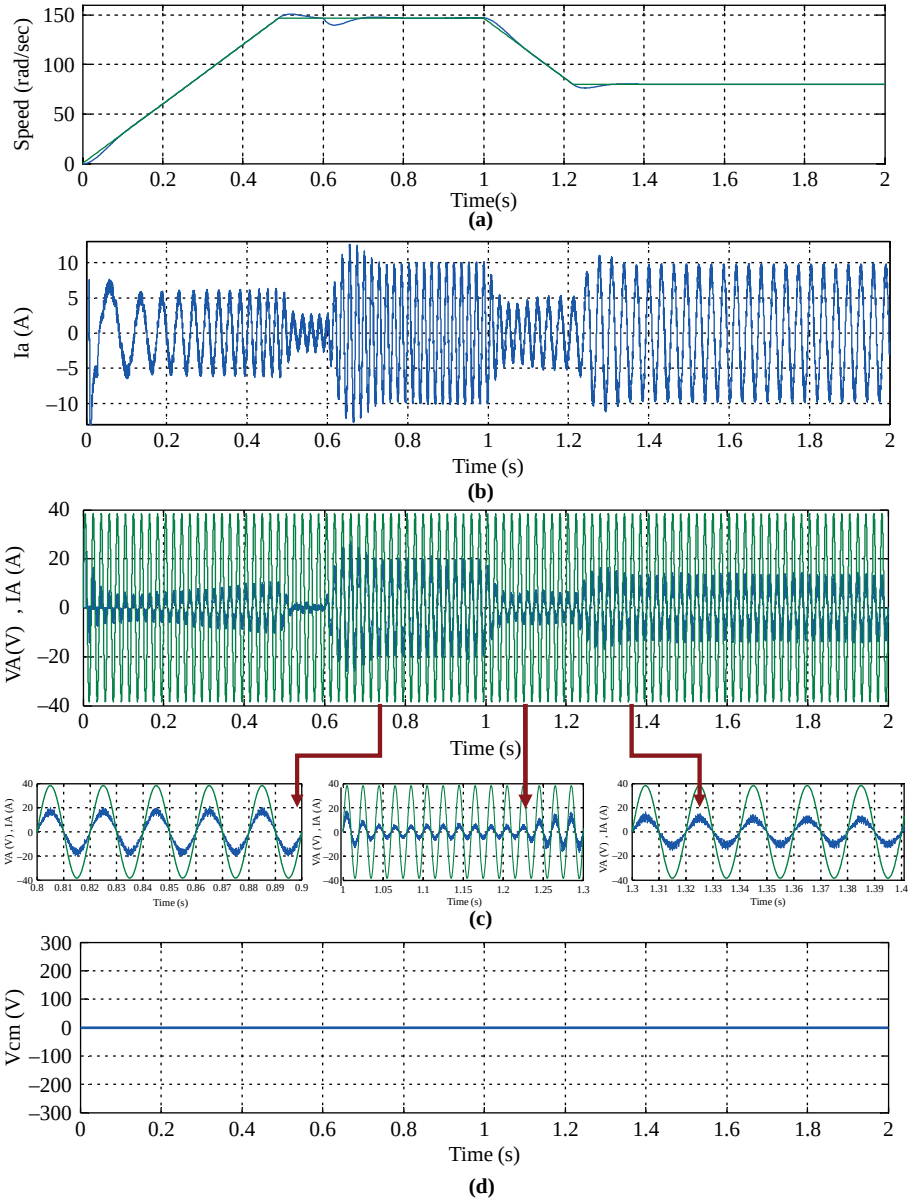


Figure 15.
(a) Speed of the induction motor, (b) input current to the induction motor, (c) input voltage and input current of the PDMC, (d) common mode voltage at the load

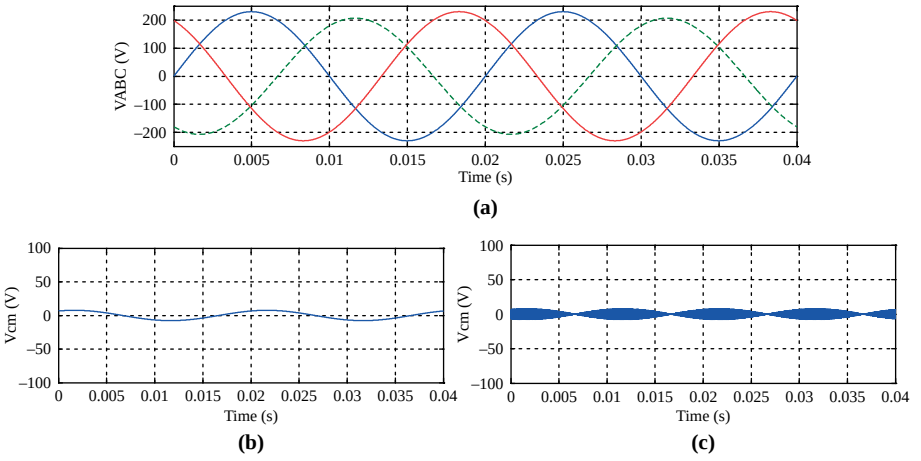


Figure 16.
(a) Unbalanced input voltage, (b) CMV of CMC and (c) CMV of PDMC

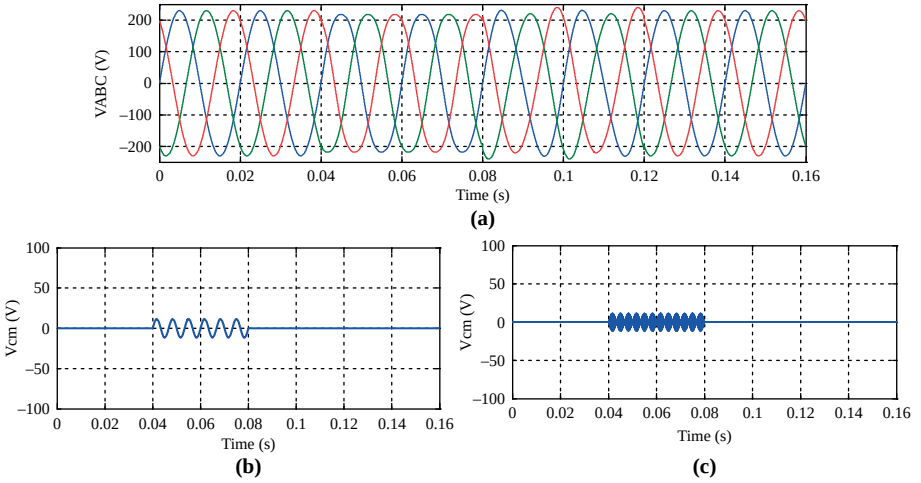


Figure 17.
(a) Non-sinusoidal input voltage, (b) CMV of CMC and (c) CMV of PDMC

CMC is limited between unity power factor and output power factor. In current controlled technique for PDMC and CMC, the modulation index reduces further. It is also found that the switching stresses of individual switches reduce in PDMC compared to CMC because of additional states introduced in the PDMC topology. Hence, the proposed PDMC modulated RSVM technique can be used for the elimination of common mode voltage with a higher modulation index.

Acknowledgements

The authors wish to thank the Centre for Wind Energy Technology (C-WET), Ministry of New and Renewable Energy, Government of India, for financial support of the project "Study and control of weak grid connected matrix converter based DFIG systems". The work carried out in this paper forms a part of the project.

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DIRECT POWER CONTROL OF A MATRIX CONVERTER BASED WIND ENERGY CONVERSION SYSTEM

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Abstract— **A conventional wind turbine uses the AC-DC-AC converter, which incorporates a bulky storage electrolytic capacitor, prone to poor performance at high temperatures and susceptible to failures. The storage capacitor not only increases the system weight and volume but also reduces the reliability of the system. In an effort to eliminate the storage capacitor, direct AC-AC power electronic converters are under investigation for implementation in wind energy conversion systems [1]−[3]. This paper attempts to incorporate a matrix converter as the power electronic converter for a doubly-fed induction generator (DFIG) wind turbine system, which controls the stator power using the rotor power electronic converter. Although the Direct Power Control (DPC) technique is widely used, the power ripple is prevalent and significantly large. The Direct Torque Control-Space Vector Modulation (DTC-SVM) technique was proposed as an alternative to minimize the torque ripple in induction motor drives. The DPC-Space Vector Modulation (DPC-SVM) is derived from the DTC-SVM technique, where the torque and real power are considered to be analogous. The control of stator power is carried out on a 50 Hz, 3 hp DFIG proto-type in the MATLAB / Simulink environment using DPC-SVM algorithm. The wind model is emulated with a Squirrel Cage Induction Motor (SCIM) v/f drive.**

Keywords—Matrix Converter, DFIG, DPC-SVM, DSVM, direct AC-AC, rotor side control.

I. INTRODUCTION

Today, most of the installed wind turbines are variable-speed wind turbines based on the doubly-fed Induction generators (DFIGs), wound rotor synchronous generators (WRSGs) and permanent magnet synchronous generators (PMSGs). All these generators allow variable-speed generation. The primary difference between the former, shown in Fig. 1, and the other two configurations arises due to the point of connection of the bidirectional converter required for power exchange between the generator and the grid.

The WRSG and the PMSG employ a full-converter with rating equal to that of the grid. The DFIG allows the use of a partial converter, almost 30% of the full converter rating, which gives a drastic reduction in the size of the components and cost involved. However, it also comes with the disadvantage of slip-rings that require constant maintenance and a limited operating speed range (~ -30% to +20%). The other two configurations provide full operating speed range. Nevertheless, due to the merits of the DFIG configuration, it is taken up in this work.

The bidirectional converter employed in most of the wind turbines is the AC-DC-AC converter shown in Fig. 1, due to its robust ride-through capability. However, the disadvantages of the oversized capacitor and its degradation over time are paving way for new topologies that are still under research, like the matrix converter, which converts AC-AC directly, eliminating the DC-link capacitor. Fig. 2 shows a matrix converter based variable-speed wind turbine configuration employing a DFIG.

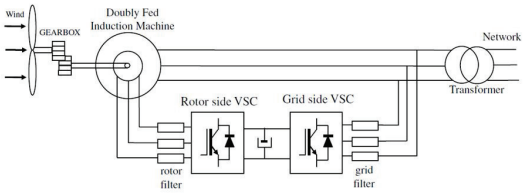

Fig. 1. DFIG-based variable wind-speed turbine

The matrix converter offers some significant advantages such as adjustable power factor, inherent four-quadrant operation, high quality sinusoidal input/output waveforms and high power density [4]. Hence, it has received extensive attention in research as a replacement for the traditional AC-DC-AC converter for variable-voltage and variable-frequency AC drive applications.

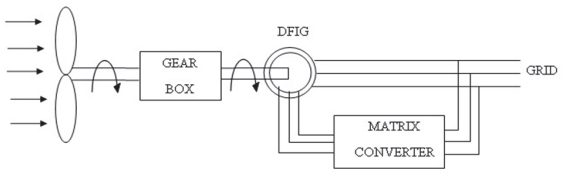

Fig. 2. Matrix converter based variable speed WECS

The purpose of the bidirectional converter is to control the power exchange between the wind turbine and the power grid, and to ensure the synchronization of the generated voltage with that of the grid. The generator and converter together inject real power and reactive power into the network in response to the power control commands P_{ref} and Q_{ref}.

Section II discusses the mathematical model of the doubly-fed induction motor (DFIM). The matrix converter and its modulation algorithm are discussed in Section III. The method of control of the stator power through the modulation of the matrix converter connected at the rotor side of the machine is discussed in Section IV. Simulation results are presented in Section V.

II. Mathematical Model of the DFIM

The commonly used induction machine model is based on the flux linkages as in [5]-[6]. The inductance of the windings varies with rotor position, and hence leads to a complex mathematical system. In order that the time-varying inductances appear constant, the stationary three-axis machine variables are transformed to a rotating two-axis frame, the d-q frame.

Machine parameters are usually represented in ohms or p.u. system. Hence, the inductances of the windings are represented as reactances. The voltage equations of the stator and rotor circuits in the dq-frame in terms of the flux linkages per second are given in Eqns. (1)-(4).

$$v_{qs}=r_s i_{qs}+\frac{\omega}{\omega_b}\psi_{ds}+\frac{p}{\omega_b}\psi_{qs} \quad (1)$$

$$v_{ds}=r_s i_{ds}-\frac{\omega}{\omega_b}\psi_{qs}+\frac{p}{\omega_b}\psi_{ds} \quad (2)$$

$$v'_{qr}=r'_r i'_{qr}+\left(\frac{\omega-\omega_r}{\omega_b}\right)\psi'_{dr}+\frac{p}{\omega_b}\psi'_{qr} \quad (3)$$

$$v'_{dr}=r'_r i'_{dr}-\left(\frac{\omega-\omega_r}{\omega_b}\right)\psi'_{qr}+\frac{p}{\omega_b}\psi'_{dr} \quad (4)$$

where, ω_b is the base angular velocity, and the flux linkages are given by Eqns. (5)-(8). The dq components of stator and rotor currents are given in Eqns. (9)-(12).

$$\psi_{qs}=X_{ls}i_{qs}+X_m(i_{qs}+i'_{qr}) \quad (5)$$

$$\psi_{ds}=X_{ls}i_{ds}+X_m(i_{ds}+i'_{dr}) \quad (6)$$

$$\psi'_{qr}=X'_{lr}i'_{qr}+X_m(i_{qs}+i'_{qr}) \quad (7)$$

$$\psi'_{dr}=X'_{lr}i'_{dr}+X_m(i_{ds}+i'_{dr}) \quad (8)$$

$$i_{qs}=\frac{1}{X_{ls}}(\psi_{qs}-\psi_{mq}) \quad (9)$$

$$i_{ds}=\frac{1}{X_{ls}}(\psi_{ds}-\psi_{mq}) \quad (10)$$

$$i'_{qr}=\frac{1}{X'_{lr}}(\psi'_{qr}-\psi_{mq}) \quad (11)$$

$$i'_{dr}=\frac{1}{X'_{lr}}(\psi'_{dr}-\psi_{md}) \quad (12)$$

The expressions for electromagnetic torque and speed are computed using Eqns. (13) and (14).

$$T_e=\frac{3}{2}\frac{P}{2}(\psi_{ds}i_{qs}-\psi_{qs}i_{ds}) \quad (13)$$

$$\omega_r=\frac{\omega_b}{2H}\int(T_e-T_L) \quad (14)$$

The dynamic behaviour of the DFIM are described by Eqns. (1)-(14). The parameters of the 50 Hz, 3 hp laboratory DFIM were obtained by conducting the DC test, the blocked rotor test and the no-load test on the machine [7], and are listed in Table I. The dynamic model of the DFIM was simulated in the synchronous reference frame and the characteristics were obtained. This model is used further in this work.

Table I. Parameters of the 415 V, 50 Hz DFIM

Supply	415 V, 3-Φ AC
f_s	50 Hz
R_s	4.608 Ω
R_r	6.576 Ω
L_{ls}	23 mH
L_{lr}	23 mH
L_m	442.5 mH
P	4

III. Matrix Converter

The matrix converter is the force-commutated version of the cyclo-converters, which overcomes the disadvantage of the conventional cyclo-converter such as the limitations in the frequency conversion, rich output voltage harmonics and increased number of switches. The direct matrix converter is an array of 3×3 bidirectional switches connected in common-emitter configuration as shown in Fig. 3. The topology directly interconnects two independent multi-phase voltage systems at different frequencies.

A control technique based on space vector theory was proposed for the matrix converter and this came to be popularly known as the Direct Space Vector Technique (DSVM) [8]. The idea of the 'fictitious DC Link' in the MC, decoupled the control into smaller independent units [9]. Though it is an easy method in comparison to the DSVM, the values of duty cycles obtained may be very small that result in very narrow pulses. There is always a chance that it may be missed by the digital controller [10]. Hence, the DSVM technique as in [11] is employed to trigger the bidirectional switches.

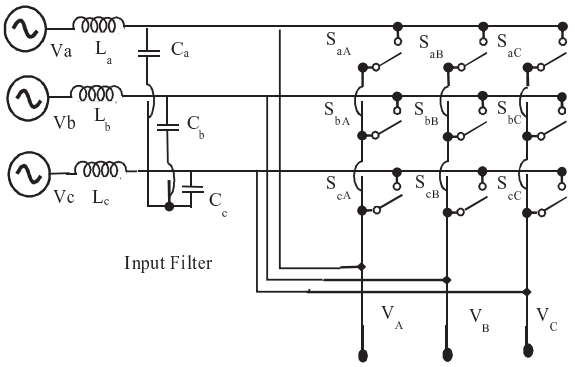

Fig. 3. Conventional matrix converter

In order that the current drawn by the matrix converter be in phase with the phase voltage, and hence achieve unity power factor operation, the phase voltage of the grid itself is given as the reference signal to the current space vector module. The three-phase voltage that is desired at the output terminals of the converter is taken as the reference signal of the voltage space vector module.

IV. DPC-SVM CONTROLLER

The DFIG is supplied by both the stator and rotor. By changing the stator and rotor voltages, the machine can operate at different points of torque, and hence, the stator and rotor active power and reactive power. In general, the stator of the machine will be connected directly to the grid, which means that the stator voltage is fixed. On the contrary, the rotor voltage is supplied by a bidirectional power electronic converter, allowing modulation of the rotor voltage amplitude, frequency and phase with respect to the stator voltage as required. In order to achieve a certain power exchange with the grid, the rotor voltage amplitude, frequency and phase shift must be selected accordingly.

This can be achieved by the means of the well-established Direct Power Control technique (DPC). The biggest disadvantages of direct power control are the variable switching frequency, the current and torque ripple as in [12]. The movement of reactive power vector during the changes of cyclic sectors is responsible for creating notable edge oscillations of electromagnetic torque. Another issue is the implementation of hysteresis controllers, which require a high sampling frequency.

Initially, the DTC-SVM technique was developed to reduce the torque ripple for direct torque controlled Induction motor drives [13]. The principle was then extended to the DPC technique. The DPC-SVM technique requires calculations in the control schemes of the voltage vectors that are to be modulated at the converter terminals. Since the power order to the turbine is known, it is easy to perform the modulation using the DSVM, and applying specific switching pattern to the converter. The block diagram of the scheme is shown in Figure 4.

The DPC is based on the direct control of stator active power and reactive power of the DFIM that can be calculated directly from the stator voltage and currents [13] as in Eqns. (15) and (16).

$$P_s = \frac{3}{2}\mathrm{Re}\left\{\vec{v_s}\cdot\vec{i_s}^{*}\right\} \quad (15)$$

$$Q_s = \frac{3}{2}\mathrm{Im}\left\{\vec{v_s}\cdot\vec{i_s}^{*}\right\} \quad (16)$$

where v_s is the stator voltage, and i_s is the stator current.

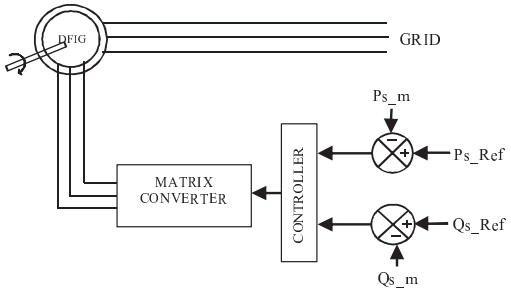

Fig. 4. Block diagram of the DPC for the MC-based DFIG system

The stator active power and reactive power are controlled by applying the reference voltage from the controller to the rotor windings of the machine. To do this, we first obtain the equations of the stator voltages in the synchronous reference frame as outlined in [14]. It should be noted that the 'd' component of the stator voltage space vector is aligned with the grid phase voltage V_{as}. The rotor voltages are computed from the stator voltage using Eqns. (17) and (18).

$$V_{dr} = s \cdot V_{ds} \quad (17)$$

$$V_{qr} = s \cdot V_{qs} \quad (18)$$

where slip $s = \frac{\omega_s - \omega_r}{\omega_s}$, V_{dr} and V_{qr} are the d and q components of the rotor voltage in the dq synchronous reference frame.

Fig. 5 shows the schematic block diagram of the DPC-SVM technique. The stator voltages and currents are measured and the d-q variables are calculated. The stator real power and reactive power are calculated. The reference voltages v_{ds}* and v_{qs}* are generated and the error is minimized using separate PI controllers. The actual voltage to be injected into the rotor circuit is obtained and transformed to the machine variables. This is the voltage reference signal for given to the Direct SVM (DSVM) algorithm.

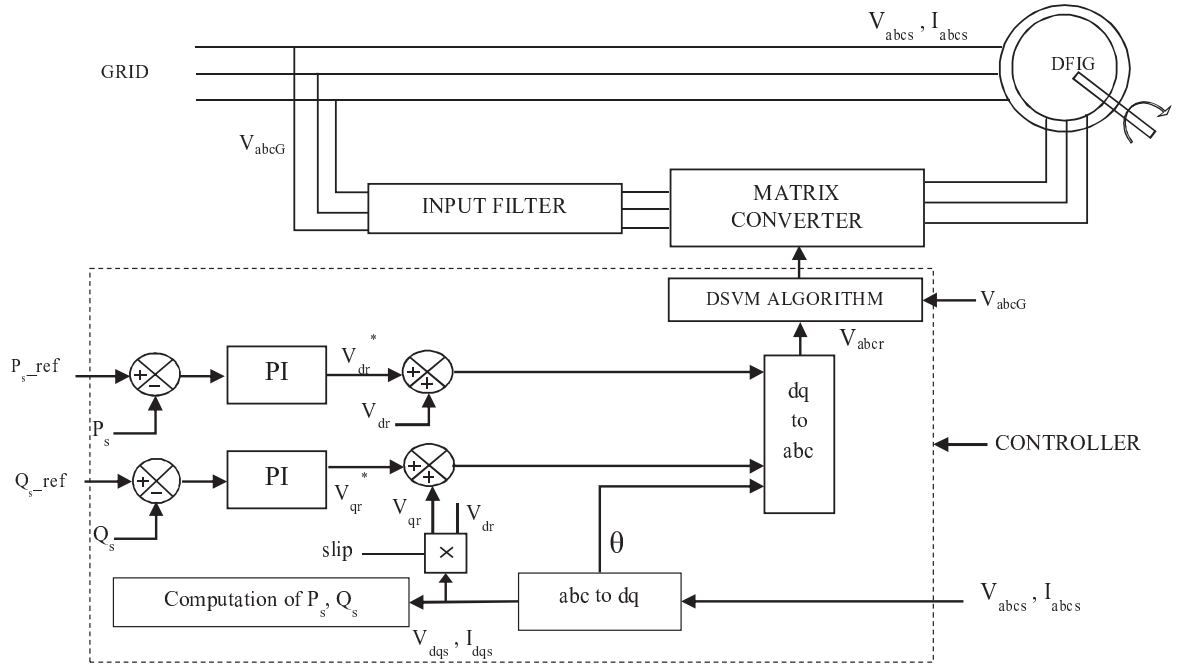

Fig. 5. Schematic of DPC-SVM algorithm

The rotor circuit rating is only 30% of the machine rating, as the rotor power is slip times the stator power. Hence, a step down transformer is required on the matrix converter input side.

The voltage at the converter side input transformer serves as the reference for the current space vector in the DSVM algorithm. This ensures that the current drawn from the grid is in phase with the grid phase voltage so that unity power factor operation is achieved. The switching pulses to the converter are obtained by synthesizing the reference rotor voltage obtained from the Controller, and input current waveforms using the DSVM algorithm block.

V. Simulation Results

Simulation of the proposed control strategy for a DFIG-based generation system was carried out using MATLAB/ Simulink. The DFIG is rated at 3 hp and its parameters are given in Table I. The values of the proportional and integral constants were obtained using trial and error method for the real and reactive power controllers. The switching frequency of the MC along with its filter circuit parameters are given in Table II.

Initially, the DFIG was operated in the generating mode with the speed input to the shaft set at 170 rad/s until 3 s. At 3 s, the speed was changed to 147 rad/s. The reference for the reactive power was set as 0 VAR, implying that the machine is not required for reactive power compensation, and also that it should absorb as minimum reactive power as possible from the grid for operation. The active power reference was step changed from 0 W to -1 kW at 2.5 s, and from -1kW to -2 kW at 4.5 s.

Table II Parameters of the Matrix Converter

PARAMETERS	VALUE
R_{fl} (Ω)	20
L_f (mH)	3
R_{fc} (Ω)	1000
C_f (μF)	10
Switching Frequency (kHz)	5
Input Voltage(L-L)	120 V

Fig. 6 shows the stator active and reactive powers. Fig. 7 shows that the input current drawn by the converter from the grid is sinusoidal. Fig. 8 shows the injected rotor voltage waveform, which is of interest. When the machine is operated at sub-synchronous speed, the magnitude of the rotor voltage does not increase to meet the generation demand. Only the magnitude of the current drawn by the rotor increases, whose amplitude is equal to the input current drawn by the converter. Also, the frequency of the

output voltage of the matrix converter varies corresponding to the speed of the machine, and is equal to the slip speed.

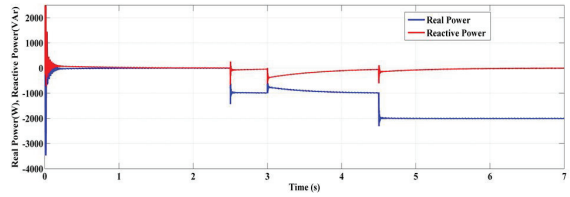

Fig. 6. Stator active and reactive powers

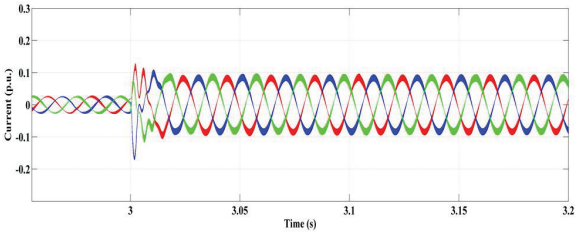

Fig. 7. Current drawn by the converter

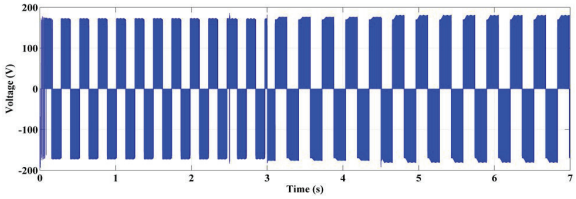

Fig. 8. Line-to-line voltage injected by the converter into the rotor of DFIG

Figs. 9 and 10 show the stator and rotor currents. The rotor current is at the slip frequency, while its magnitude varies according to the stator power requirement. It is to be noted that the rotor current is at slip frequency, while the input current of the MC is at grid frequency. This is achieved by setting the voltage at the input terminals of the converter, V_{abcG} as the reference for the input current of the SVM algorithm, and hence the input current frequency is the same as that of the grid voltage. The rotor voltage frequency is set by the controller, and hence the frequency of the rotor current is same as that of the rotor voltage. Hence, the voltage obtained at the output terminals of the MC has variable frequency and magnitude, while the input voltage and current are at fixed frequency. The magnitude of the input current to the converter alone varies with the reference power.

Fig. 11 shows the real power consumed by the rotor. When the machine operates in super-synchronism, the rotor power is negative, implying that the power is delivered from the rotor to the grid. Under low speed wind conditions, the machine runs at sub-synchronous speed. The stator will not be able to deliver the power that it is ordered to deliver to the grid. The rotor draws the percentage of power that is deficit from the grid through the converter. This additional power is added to the already available stator power to meet the demand. Hence, the rotor power is positive, i.e., the rotor draws power from the grid.

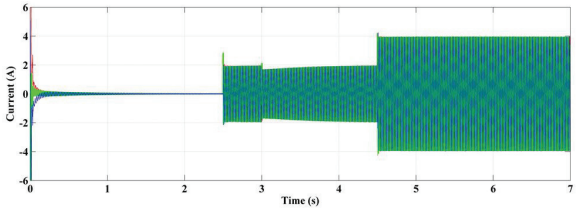

Fig. 9. Stator current

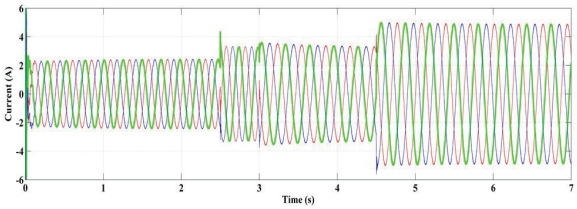

Fig. 10. Rotor current

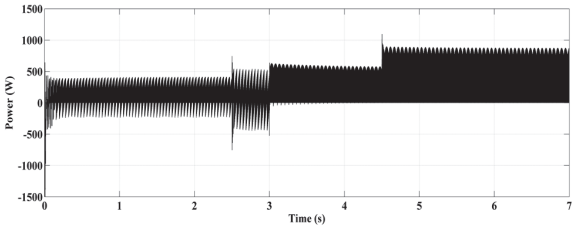

Fig. 11. Real power drawn by the rotor

The rotor power is less than half the stator power at any instant of time. Hence, the rating of the converter can be taken as half of that of the stator. From Fig. 6, it can be seen that the stator delivers power to the grid under both modes of operation, sub-synchronous and super-synchronous speeds.

VI. Conclusion

The DPC-SVM algorithm has been implemented for a MC-based DFIG system and the control of real and reactive powers of the machine was achieved. The bidirectional converter and its controller make it possible for the operation of the machine as a generator for a wide range of wind speed. The effectiveness of the controller can be clearly seen. The responses of both the active and the reactive powers during the step change in reference are within a few milliseconds. There is no overshoot of either the stator/rotor currents or the active/reactive power. As the converter switching frequency in the DPC-SVM strategy is fixed, the machine parameters such as

the rotor speed, the active and the reactive powers are not affected, which was the major problem with the DPC strategy. Stable operation of the system was possible without the two-stage power conversion. Hence, the problems that arose with the large DC-link capacitor are eliminated.

ACKNOWLEDGMENT

The authors would like to thank the Center for Wind Energy Technology (C-WET), Chennai for giving us the opportunity and support to carry out the proposed work.

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MODELING AND DIRECT POWER CONTROL OF DFIG FOR WIND ENERGY CONVERSION SYSTEM WITH A BACK TO BACK CONVERTER

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***Abstract*— The Variable-speed wind turbines are gaining more prominence due to their ability to generate power for a wide range of wind speeds. This class of turbines requires a fraction of the power be drawn from the grid in order to deliver the promised power when there is a deficiency in wind speed. For this purpose, a Doubly-Fed Induction Generator (DFIG) with a bidirectional converter (AC-DC-AC) on the rotor side is employed. The back-to-back converter controls the flow of energy from the machine to the grid and vice-versa. The Direct Power Control algorithm is used to control the power delivered by the stator to the grid. In this paper, the Space Vector Modulation (SVM) technique using the PI-controllers is used for controlling active and reactive powers. The SVM algorithm triggers the power electronic devices of the converter resulting in improved input current waveform. The paper discusses the simulation results of 1.5 MW DFIG machine connected to the grid via back–to–back converter.**

***Keywords*—DFIG, Back-to-Back Converter, Direct Power Control, Space Vector Modulation, PI controller.**

I. INTRODUCTION

The variable speed wind turbine generates power in the sub-synchronous speed and the super-synchronous speed [1]. The variable speed wind turbine uses the converter to convert the generated AC power into DC power and again the DC power to the AC power. The converter can be of fully rated or partially rated [10]. In addition, the generators used in the variable speed wind turbine type can be of the permanent magnet synchronous generator (PMSG) or the DFIG. If we use PMSG, the cost of the generator and converter are higher because of the permanent magnet and full converter. In this topology, the DFIG is used, which is cost wise effective. The converter used has reduced ratings and the power handled by it is ±30% of stator power. The power rating of the converter is less because the rotor injected voltage and frequency will be slip times the stator frequency. By controlling the frequency of the rotor-injected voltage, the DFIG can deliver power at both sub-synchronous speed and super-synchronous speed [8]. Fig. 1 shows the general block diagram of the DFIG with a back-to-back converter. The back-to-back converter consists of two voltage source converters, one called as the rotor side converter (RSC) and the other called as the grid side converter (GSC). The RSC generates a three-phase voltage with variable amplitude and variable frequency in order to control the generator torque and the power exchanged between the stator and the grid. The GSC exchanges the active power extracted or injected by the RSC with the grid. A DC-link maintained by the capacitor is connected between the two voltage source converters.

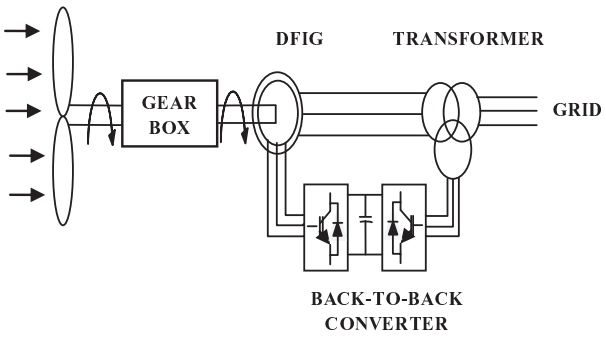

Fig. 1 Block diagram of the back-to-back converter based DFIG

A. wind turbine model

The wind turbine is described in terms of the power it generates, which depends on the wind velocity, air density, turbine radius and the power coefficient for the turbine. The turbine radius plays an important role in energy capture from the wind. If the radius of the turbine is large, then it will capture large amount of energy from the wind [4]. The power P_t that is produced by the wind turbine is given by Equation (1)

$$P_t = \frac{1}{2}\rho R^2 V^3 C_p(\lambda,\theta) \quad (1)$$

where, C_p is the power coefficient of the wind turbine, θ is the pitch angle of the turbine blade, ρ is the air density, R is the turbine radius, and V is the wind velocity. The turbine is normally coupled to shaft of the generator through a gearbox whose gear ratio G is chosen to maintain the speed of the generator shaft within a desired speed range. The turbine torque and the shaft speed are related as in Equations (2) and (3).

$$T_m=\frac{T_t}{G} \tag{2}$$

$$\omega_t=\frac{\Omega_m}{G} \tag{3}$$

where, T_m is the driving torque of the generator, Ω_m is the generator shaft speed and T_t is the turbine torque given by Equation (4).

$$T_t=\frac{P_t}{\omega_t} \tag{4}$$

C_p, which is a function of the wind speed, the turbine rotational speed and the pitch angle of the wind turbine blades, is given by Equation (5).

$$C_p(\lambda,\theta)=\sum_{i=0}^{4}\sum_{j=0}^{4}\alpha_{ij}\theta^i\lambda^j \tag{5}$$

Where λ is the ratio of the rotor blade tip speed, θ is blade pitch angle in degrees, α_{ij} is C_p power coefficient. C_p depends on the ratio between the shaft angular velocity ω_t and the wind velocity V. The ratio is called as tip-speed ratio and is given in Equation (6).

$$\lambda=\frac{\omega_t R}{V} \tag{6}$$

II. MODELING OF DFIG

In order to study the dynamic characteristics of induction generator it is modeled by using the mathematical equation [6]. The three-phase stator and rotor circuits are shown in Fig. 2 and the dynamic voltage equations are described using Eqns. (7) and (8)

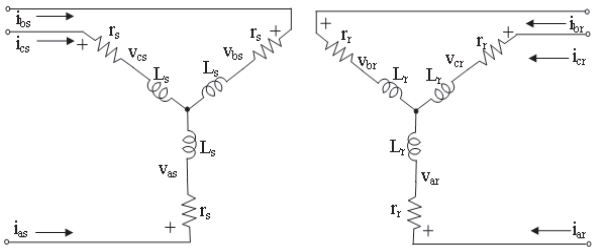

Fig. 2 Stator and rotor circuits of the induction machine

$$v_{abcs}=r_s i_{abcs}+p\lambda_{abcs} \tag{7}$$

$$v_{abcr}=r_r i_{abcr}+p\lambda_{abcr} \tag{8}$$

Where p is differential operator, v_{abcs} is stator voltage, r_s is stator resistance, λ_{abcs} is stator flux linkage of stator and v_{abcr} is rotor voltage, r_r rotor resistance, λ_{abcr} is rotor flux linkage. The mathematical modeling and simulation is done by using d-q reference frame theory. It is carried out by computing the flux linkages, voltage, current, torque, and rotor speed by using the Eqns. (9) to (14).

$$v_{qs}=r_s i_{qs}+\frac{\omega}{\omega_b}\psi_{ds}+\frac{p}{\omega_b}\psi_{qs} \tag{9}$$

$$v_{ds}=r_s i_{ds}-\frac{\omega}{\omega_b}\psi_{qs}+\frac{p}{\omega_b}\psi_{ds} \tag{10}$$

$$v_{0s}=r_s i_{0s}+\frac{p}{\omega_b}\psi_{0s} \tag{11}$$

$$v'_{qr}=r'_r i'_{qr}+\left(\frac{\omega-\omega_r}{\omega_b}\right)\psi'_{dr}+\frac{p}{\omega_b}\psi'_{qr} \tag{12}$$

$$v'_{dr}=r'_r i'_{dr}-\left(\frac{\omega-\omega_r}{\omega_b}\right)\psi'_{qr}+\frac{p}{\omega_b}\psi'_{dr} \tag{13}$$

$$v'_{0r}=r'_r i'_{0r}+\frac{p}{\omega_b}\psi'_{0r} \tag{14}$$

Where ω_b is the base angular velocity, ω_r is angular speed of the rotor and r_s is stator winding resistance. v_{qs}, v_{ds}, v_{os} are stator voltages in dq0 reference frame. v'_{qr}, v'_{dr}, v'_{0r} is rotor voltage in dq0 reference frame referred to stator. i_{qs}, i_{ds} are stator currents in dq0 reference frame and i'_{qr}, i'_{dr} are rotor currents refereed to stator in dq0 reference frame. X_{ls} is reactance of stator winding and X'_{lr} is reactance of rotor winding refereed to stator. ψ_{qs} , ψ_{ds}, ψ_{0s} are flux linkage per second in dq0 reference frame. ψ'_{dr}, ψ'_{qr}, ψ'_{0r} is flux linkage per second of rotor referred to stator in dq0 reference frame.

The flux linkages of the machine can be calculated by using the inductances of the machine and current. The expression for flux linkage is given in the Equation (15) to (20)

$$\lambda_{qs}=L_{ls}i_{qs}+L_m(i_{qs}+i'_{qr}) \tag{15}$$

$$\lambda_{ds}=L_{ls}i_{ds}+L_m(i_{ds}+i'_{dr}) \tag{16}$$

$$\lambda_{0s}=L_{ls}i_{0s} \tag{17}$$

$$\lambda'_{qr}=L'_{lr}i'_{qr}+L_m(i_{qs}+i'_{qr}) \tag{18}$$

$$\lambda'_{dr}=L'_{lr}i'_{dr}+L_m(i_{qs}+i'_{dr}) \tag{19}$$

$$\lambda'_{0r}=L'_{lr}i'_{0r} \tag{20}$$

Where λ_{qs} ,λ_{ds}, λ_{0s} stator flux linkage in dq0 reference frame, λ'_{qs}, λ'_{ds}, λ'_{0s} are rotor flux linkage referred to primary in the dq0 reference frame. L_{ls} is stator winding inductance, L'_{lr} is rotor winding inductance referred to stator. L_m is mutual inductance. The current and electromagnetic torque in the synchronously rotating frame can be calculated using the Equation (21) to (25)

$$i_{qs}=\frac{1}{X_{ls}}(\psi_{qs}-\psi_{mq}) \tag{21}$$

$$i_{ds}=\frac{1}{X_{ls}}(\psi_{ds}-\psi_{mq}) \tag{22}$$

$$i'_{qr}=\frac{1}{X'_{lr}}(\psi'_{qr}-\psi_{mq}) \tag{23}$$

$$i'_{dr}=\frac{1}{X'_{lr}}(\psi'_{dr}-\psi_{md}) \tag{24}$$

$$\begin{aligned}T_e&=\frac{3}{2}\frac{P}{2}L_m\left(i_{qs}i'_{dr}-i_{ds}i'_{qr}\right)\\&=\frac{3}{2}\frac{P}{2}(\lambda'_{qr}i'_{dr}-\lambda'_{dr}i'_{qr})\\&=\frac{3}{2}\frac{P}{2}(\lambda_{ds}i_{qs}-\lambda_{qs}i_{ds})\\&=\psi_{ds}i_{qs}-\psi_{qs}i_{ds}\end{aligned} \tag{25}$$

III. GRID SIDE CONVERTER CONTROL

A. Introduction

A grid side converter maintains the DC link voltage of the capacitor and controls the reactive power absorbed or delivered to the grid. This converter consists of three-phase two-leg voltage source inverter with six IGBTs with anti-parallel diodes. This converter is a forced commutated converter whose switching states are obtained by using space vector modulation technique (SVM) [3]. GSC provides bi-directional power flow [11]. It also maintains the power quality because it will not absorb or deliver any reactive power from the grid. The grid side converter is shown in fig.3. In this control strategy, the current control method is used to control the grid side converter. The converter draws a current from the grid to maintain DC-link voltage constant. This current is taken as the reference to maintain the DC-link voltage. The capacitor value should be chosen such the DC link voltage should be maintained constant [13].

Capacitor value can be calculated by using the Equation (26)

$$c=p_{out}\frac{\sqrt{2}\div\sqrt{3}\,V_{LLrms}/V_{DC}}{2\sqrt{2}f_s V_{LLrms}\Delta V_{DC}} \quad (26)$$

where, V_{LLrms} is the line-line rms voltage, V_{DC} is the DC-link voltage, ΔV_{DC} is ripple in the DC-link voltage and f_s is the sampling frequency.

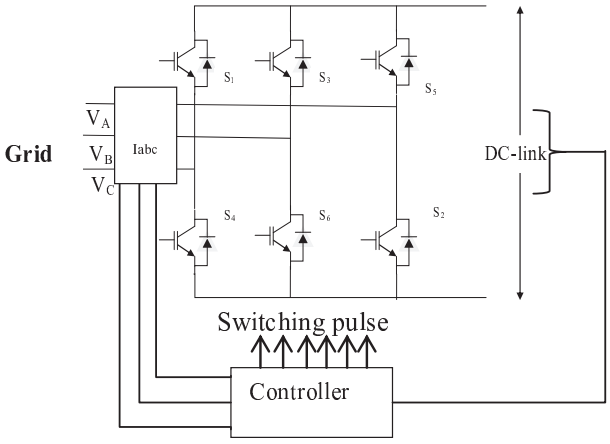

Fig. 3 Grid side converter

B. Current control scheme

The objective of the control scheme for the GSC is to keep the DC-link voltage constant regardless of the magnitude and direction of the rotor power. The control scheme is also responsible for controlling the reactive power flow between the grid and GSC. The control method used in this controller is the current control method. It consists of two control loops, the inner current loop and the outer current loop [2]. A simple proportional-Integral (PI) controller is used in th control algorithm. In this, the outer currents loop maintains the DC-link voltage constant and the inner current loop maintains the reactive power absorbed from the grid. The block diagram for the grid side control algorithm is shown in Fig. 4.

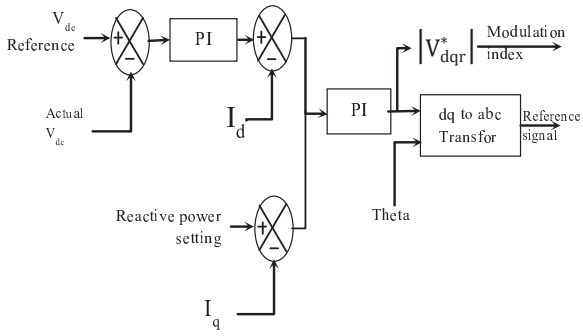

Fig. 4 Grid side converter control

In the above algorithm, the actual value of the DC-link voltage is compared with the reference DC-link voltage. The PI controller processes this error signal. The output from the PI controller is compared with the real current component of the converter. Similarly, actual reactive power of the grid is compared with the reactive current component of the converter and the error value is computed with PI controllers. However, there is a need of the reference signal in the three-phase signal so the d-q values are converted to abc values with a voltage reference vector where input A phase voltage is aligned with d frame. The modulation index is calculated from the output of PI controller. The generated reference signal from the controller is given as the reference signal to the space vector modulation algorithm (SVM), which produces the switching pulses to the grid side converter switches.

IV. ROTOR SIDE CONVERTER CONTROL

A. Introduction

The control of power in the stator can be done by the rotor side converter (RSC). Depending upon the stator actual power and power reference, the reference signal is generated and used for the control of stator power [8] [12]. The widely used control technique is the vector control technique, also known as the field-oriented control (FOC). Here we are using the Direct Power Control (DPC) technique, which is a modified form of FOC.

B. Direct power control

This control scheme requires he calculation of voltage vectors that are to be modulated at the converter terminals. Block diagram of the rotor side converter is shown in Fig. 5.

The DPC is based on the direct control of the stator active and reactive powers of the DFIG that can calculate directly by using the stator voltage and current in Equations (27) and (28)

$$P_s = \frac{3}{2}\mathrm{Re}\{\vec{v_s}\cdot\vec{i_s^*}\} \quad (27)$$

$$Q_s = \frac{3}{2} \mathrm{Im}\left\{\vec{v_s} \cdot \vec{i_s}^{*}\right\} \quad (28)$$

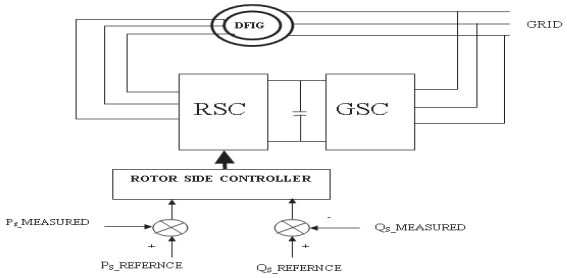

Fig. 5 Block diagram of the RSC

Where, P_s and Q_s are stator real and reactive powers, V_s and I_s are stator voltages and currents. Stator powers can also be calculated using the d-q voltage and currents of the stator as shown in the Equations (29) and (30)

$$P_s = \frac{3}{2}\left(v_{ds} \cdot i_{ds} + v_{qs} \cdot i_{qs}\right) \quad (29)$$

$$Q_s = \frac{3}{2}\left(v_{qs} \cdot i_{ds} - v_{ds} \cdot i_{qs}\right) \quad (30)$$

Where, V_{ds} and V_{qs} are the voltages of the stator and I_{ds} and I_{qs} are stator currents in the d-q reference frame. The actual real and reactive powers calculated from the Equations (27) and (28) is compared with reference power P_{ref} and Q_{ref} at any instant and the error is processed using a PI controller to generate the d-q component of the reference grid voltage. This reference voltage is transformed into three-phase voltage in the abc reference frame. This is the voltage reference signal given to the SVM algorithm of the RSC.

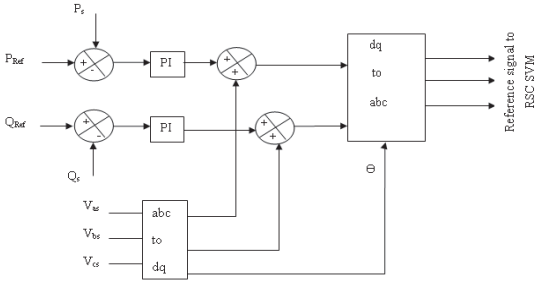

Fig. 6 Rotor side controller

Conversion of the d-q variable into abc is calculated using the slip speed of the DFIG. The rotor injected voltage and frequency is slip times the stator voltage and frequency and is calculated using Equations (31) to (33)

$$v_{dr} = s \cdot v_{ds} \quad (31)$$

$$v_{qr} = s \cdot v_{qs} \quad (32)$$

$$s = \frac{\omega_s - \omega_r}{\omega_s} \quad (33)$$

V. SIMULATION RESULTS

The simulation for the 1.5 MW DFIG is done using the MATLAB/SIMULINK model. The parameter of the machine is given in Appendix I. The fig. 7 shows the speed of the DFIG that operates at sub-synchronous (0 s to 4 s) and super-synchronous speeds (4 s to 10 s).

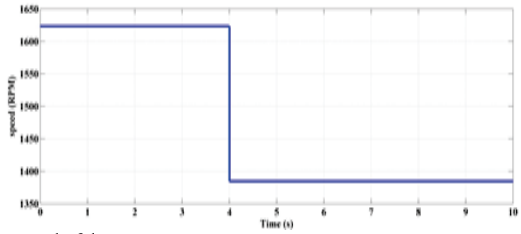

Fig. 7 Speed of the DFIG

The fig. 8 shows the reference stator real and reactive powers. Where the real power delivered is zero up to 2sec and 1MW above 2sec. Reactive power is zero at all the instants.

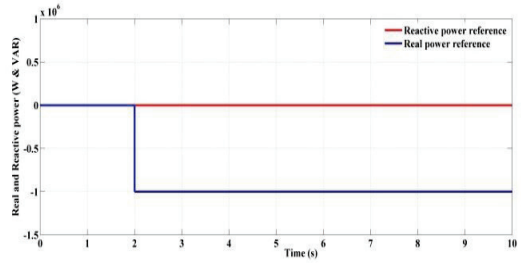

Fig. 8 Reference stator real and reactive power

The fig. 9 shows the actual real and reactive powers of the DFIG. Initially, the oscillation is more and after 1 s it delivers the real power to the grid at both sub-synchronous speeds (0 s to 4 s) and super-synchronous speeds (4 s to 10 s). Also the reactive power is zero at all the instants.

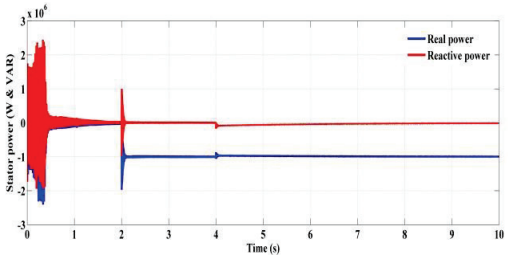

Fig. 9 Stator real and reactive power delivered to the grid

The fig. 10 shows the voltage and current of the DC bus. The initial capacitor voltage is set to be 2500 V and the reference capacitor voltage is 2000 V. When the machine is running at the sub-synchronous speed, the rotor will absorb the power from the DC bus so there will be a voltage drop. When it operates at super-synchronous speeds, the rotor delivers power to the DC bus.

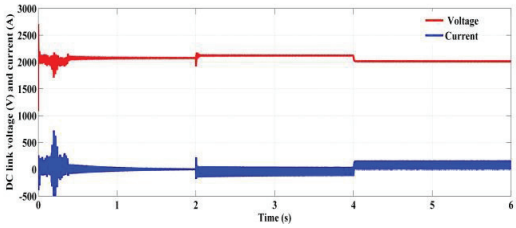

Fig. 10 DC link voltage and current

The fig. 11 shows the voltage reference generated by the controller, which given as the reference to the SVM algorithm.

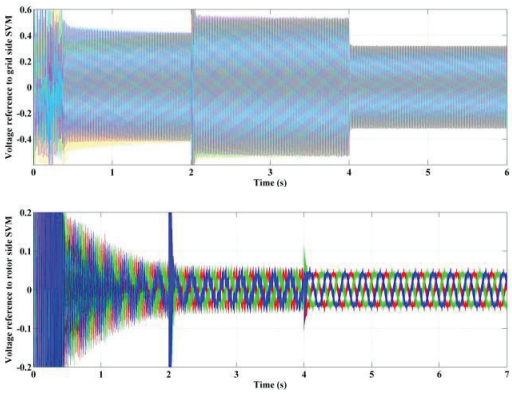

Fig. 11 Reference voltage to grid and rotor side Converters

The fig. 12 shows the input current of the GSC and fig. 13 shows the line-line output voltage of the RSC, which is injected to the rotor of the DFIG at the variable frequency depending upon the speed of the rotor.

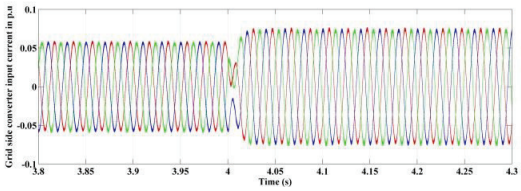

Fig. 12 Input current of Grid side converter

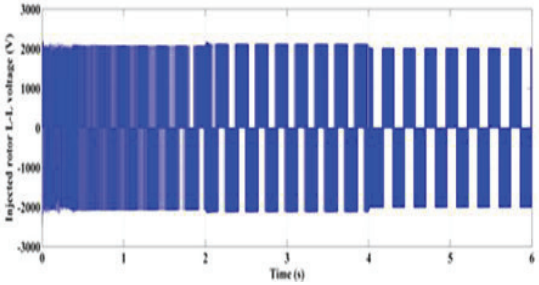

Fig. 13 Injected rotor voltage to DFIG

VI. Conclusion

This paper represents the co-ordinate control of the GSC and the RSC tied with the DFIG wind energy conversion system. The DFIG can operate at ±30% of slip speed and deliver the desired power and the algorithm used is space vector pulse width modulation (SVM). The RSC regulates the DC link voltage constant by delivering or absorbing power from the grid. By using the SVM algorithm, the input current of the GSC is sinusoidal such that the harmonics injected into the grid will be reduced. Due to the capacitor in DC link, the need of reactive power to DFIG is supplied through the capacitor by absorbing the real power from the grid. The RSC controls the power delivered from the stator of DFIG to the grid. This method provides effective voltage support under varying wind speed conditions.

APPENDIX I

Machine parameters	**Values**
DFIG rating	1.5MW
Stator voltage (L-L)	690V
Frequency	50Hz
R_s	0.00265Ω
R_r	0.00265Ω
L_s	0.1687mH
L_r	0.1337mH
Switching frequency	5kHz
Base power	1.5MW/0.95
Base voltage	690V

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